FAIRCHILD SEMICONDUCTOR®

March 2013

FDD1600N10ALZ

N-Channel PowerTrench® MOSFET

100 V, 6.8 A, 160 mΩ

Features

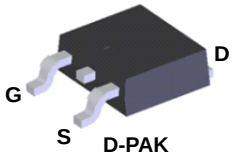
- $R_{DS(on)}$ = 124 mΩ (Typ.)@ V_{GS} = 10 V, I_D = 3.4 A
- $R_{DS(on)}$ = 175 mΩ (Typ.)@ V_{GS} = 5.0 V, I_D = 2.1 A
- Low Gate Charge (Typ.2.78 nC)
- Low C_{rss} (Typ. 2.04 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

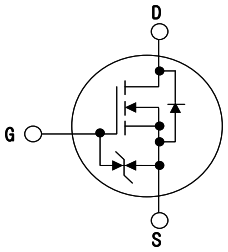
Description

This N-Channel MOSFET is produced using Fairchld Semiconductor®'s PowerTrench® process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

Applications

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter





MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter			FDD1600N10ALZ	Unit
V_{DSS}	Drain to Source Voltage			100	V
V_{GSS}	Gate to Source Voltage			±20	V
I_D	Drain Current	- Continuous (T_C = 25°C)		6.8	A
		- Continuous (T_C = 100°C)		4.3	
I_{DM}	Drain Current	- Pulsed	(Note 1)	13.6	A
E_{AS}	Single Pulsed Avalanche Energy		(Note 2)	5.08	mJ
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)		14.9	W
		- Derate above 25°C		0.12	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	°C

Thermal Characteristics

Symbol	Parameter	FDD1600N10ALZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	8.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max	87	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
1600N10ALZ	FDD1600N10ALZ	D-PAK	380mm	16mm	2500

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.1	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 80V, V_{GS} = 0V, T_C = 125°C	-	-	500	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	1.4	-	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 3.4A	-	124	160	mΩ
		V_{GS} = 5V, I_D = 2.1A	-	175	375	
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 6.8A	-	19.6	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50V, V_{GS} = 0V, f = 1MHz	-	169	225	pF
C_{oss}	Output Capacitance		-	43	55	pF
C_{rss}	Reverse Transfer Capacitance		-	2.04	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 50V, V_{GS} = 0V		85	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{GS} = 10 V; V_{DD} = 50 V, I_D = 6.8 A	-	2.78	3.61	nC
$Q_{g(tot)}$	Total Gate Charge at 5V	V_{GS} = 5 V; V_{DD} = 50 V, I_D = 6.8 A		1.5	1.95	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 50 V, I_D = 6.8 A	-	0.72	-	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 6.8 A	-	0.56	-	nC
$V_{plateau}$	Gate Plateau Volatge	V_{DD} = 50 V, I_D = 6.8 A (Note 4)	-	4.02	-	V
Q_{sync}	Total Gate Charge Sync.	V_{DS} = 0V, I_D = 3.4A (Note 5)	-	2.5	-	nC
Q_{oss}	Output Charge	V_{DS} = 50V, V_{GS} = 0V	-	5.2	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50V, I_D = 6.8A, V_{GS} = 10V, R_{GEN} = 4.7Ω	-	7	24	ns
t_r	Turn-On Rise Time		-	2	14	ns
$t_{d(off)}$	Turn-Off Delay Time		-	13	36	ns
t_f	Turn-Off Fall Time	(Note 4)	-	2	14	ns
ESR	Equivalent Series Resistance (G-S)	f = 1MHz	-	2.1	-	Ω
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.8	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	13.6	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 6.8A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 6.8A, V_{DS} = 50V, dI_F/dt = 100A/μs	-	37	-	ns
Q_{rr}	Reverse Recovery Charge		-	42	-	nC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 1mH, I_{AS} =3.18A, R_G = 25Ω, Starting T_J = 25°C
3. $I_{SD} \le$ 6.8A, di/dt ≤ 200A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
4. Essentially Independent of Operating Temperature Typical Characteristics
5. See the test circuit in page 8

Typical Performance Characteristics

Figure 1. On-Region Characteristics

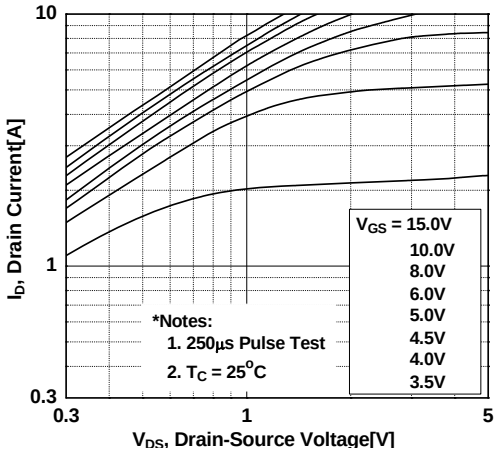


Figure 2. Transfer Characteristics

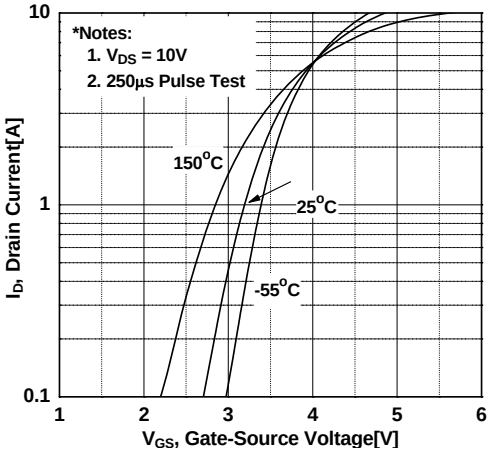


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

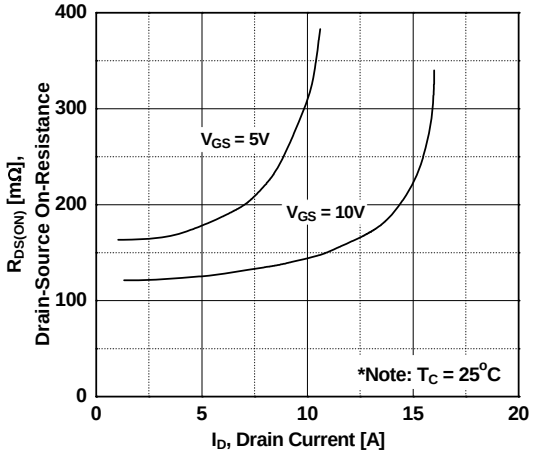


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

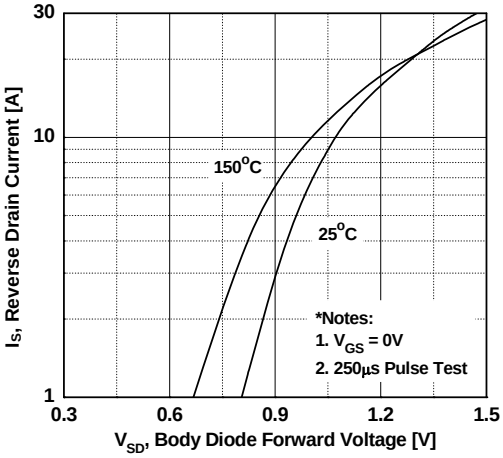


Figure 5. Capacitance Characteristics

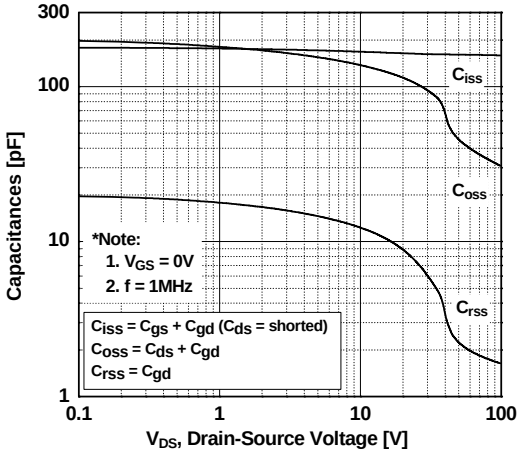
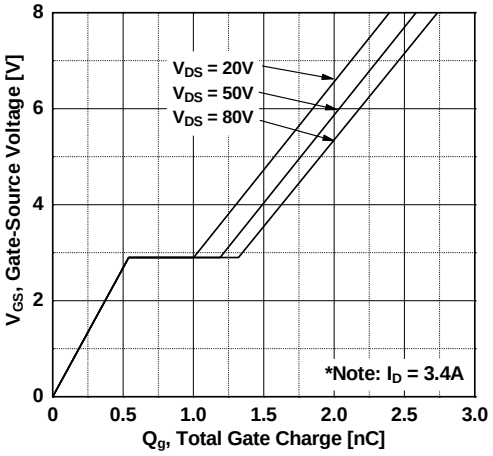


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

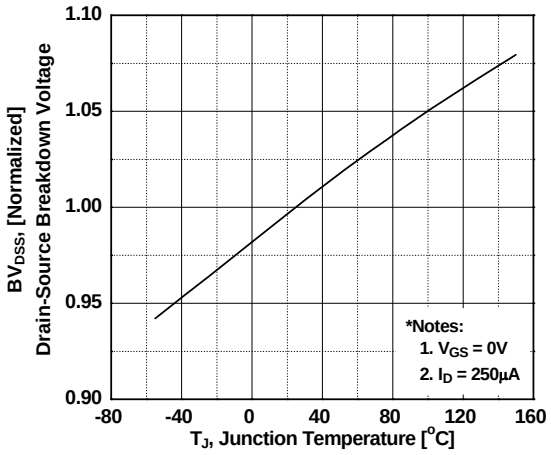


Figure 8. On-Resistance Variation vs. Temperature

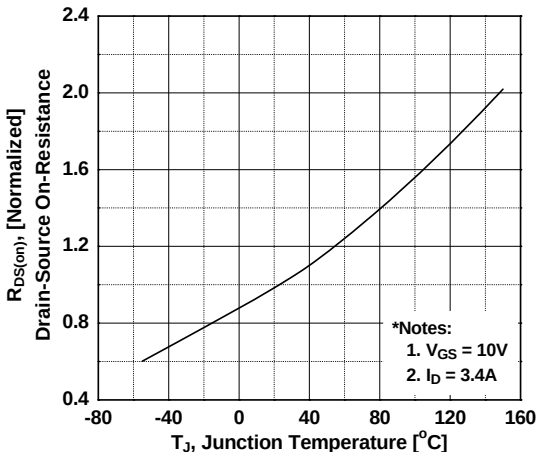


Figure 9. Maximum Safe Operating Area vs. Case Temperature

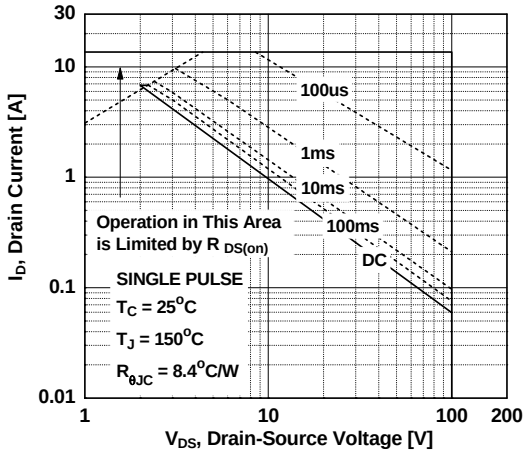


Figure 10. Maximum Drain Current

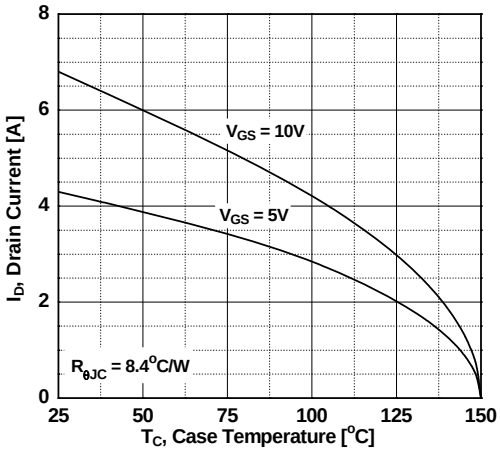


Figure 11. Eoss vs. Drain to Source Voltage

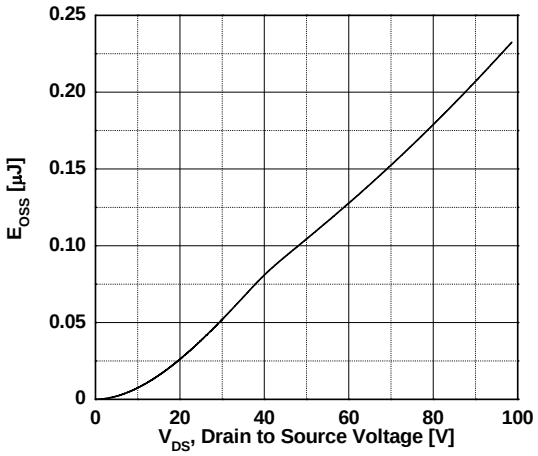
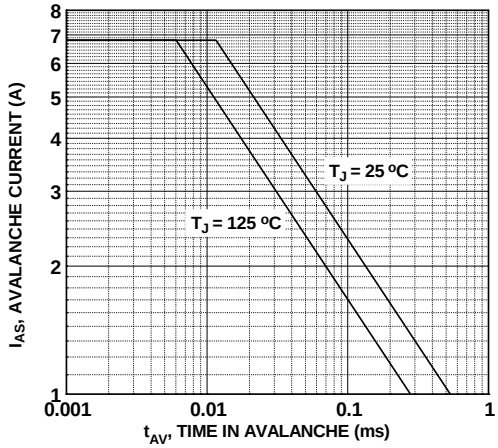
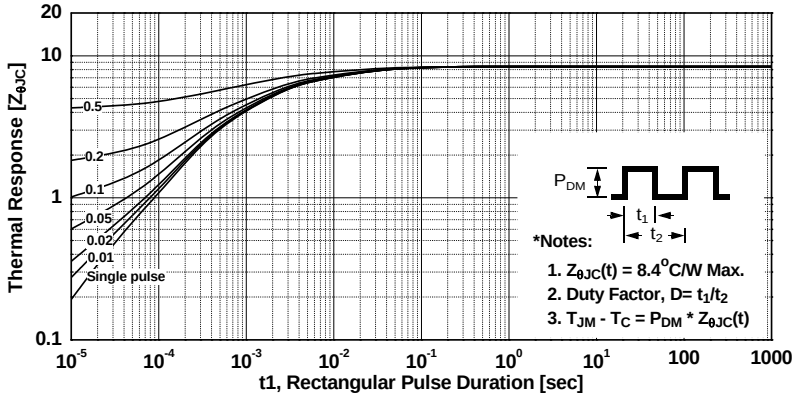


Figure 12. Unclamped Inductive Switching Capability

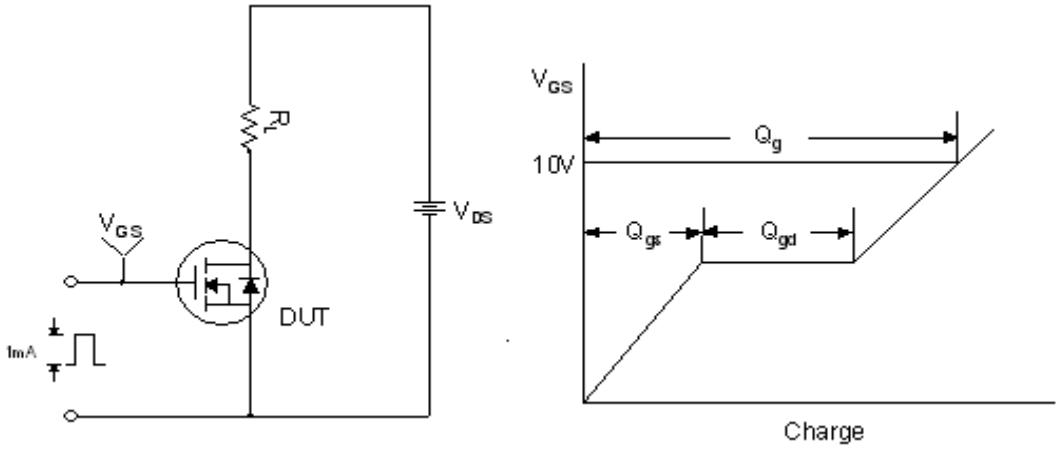


Typical Performance Characteristics (Continued)

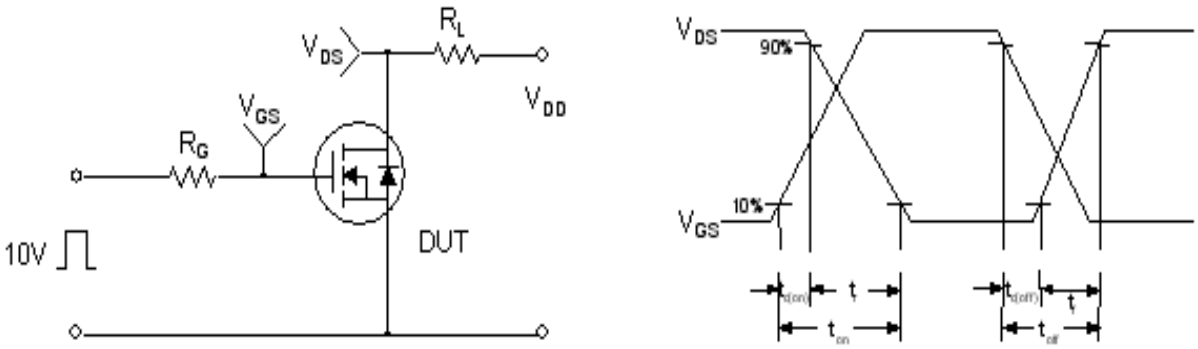
Figure 13. Transient Thermal Response Curve



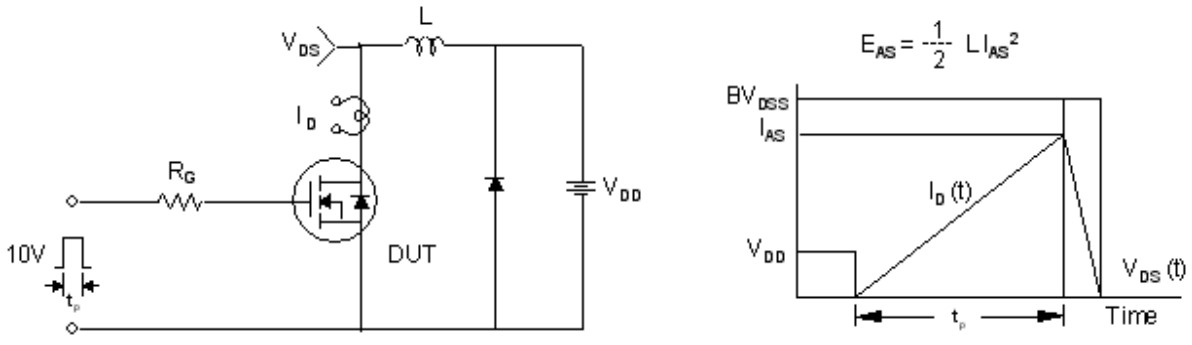
Gate Charge Test Circuit & Waveform



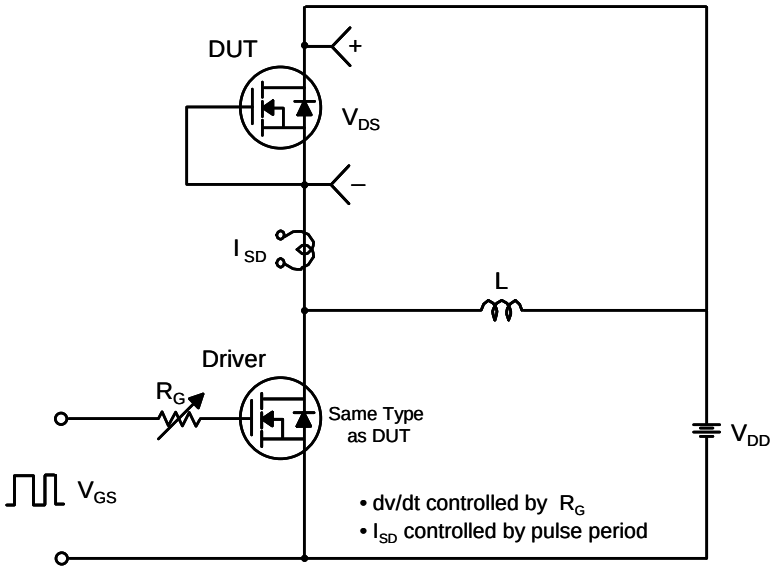
Resistive Switching Test Circuit & Waveforms

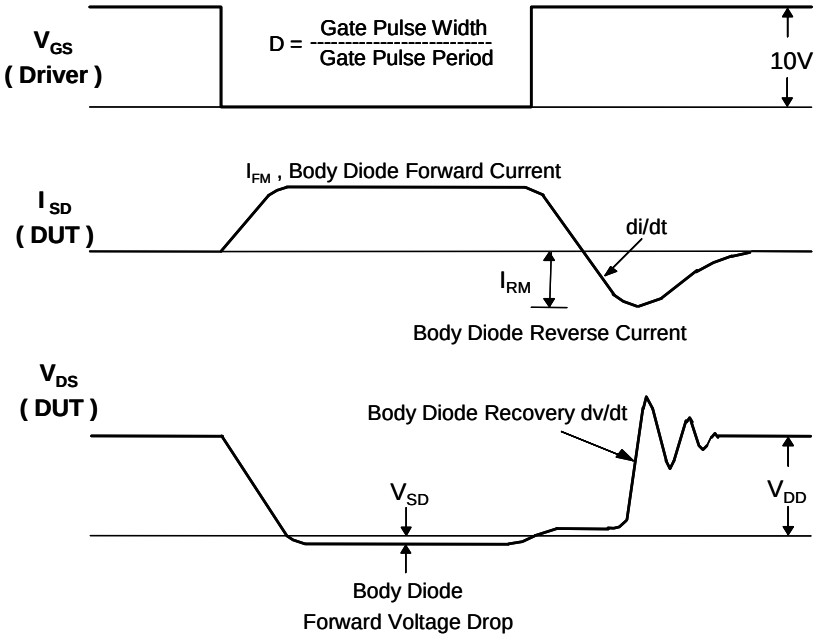


Unclamped Inductive Switching Test Circuit & Waveforms

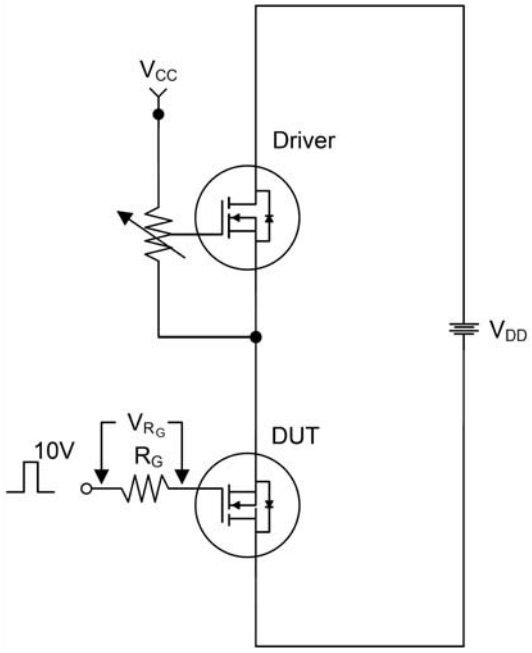


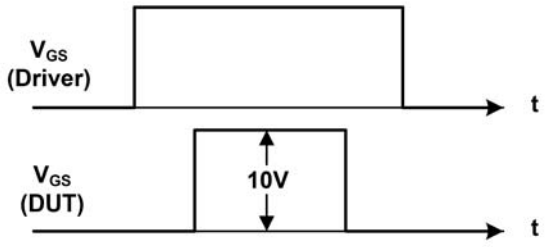
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Total Gate Charge Qsync. Test Circuit & Waveforms

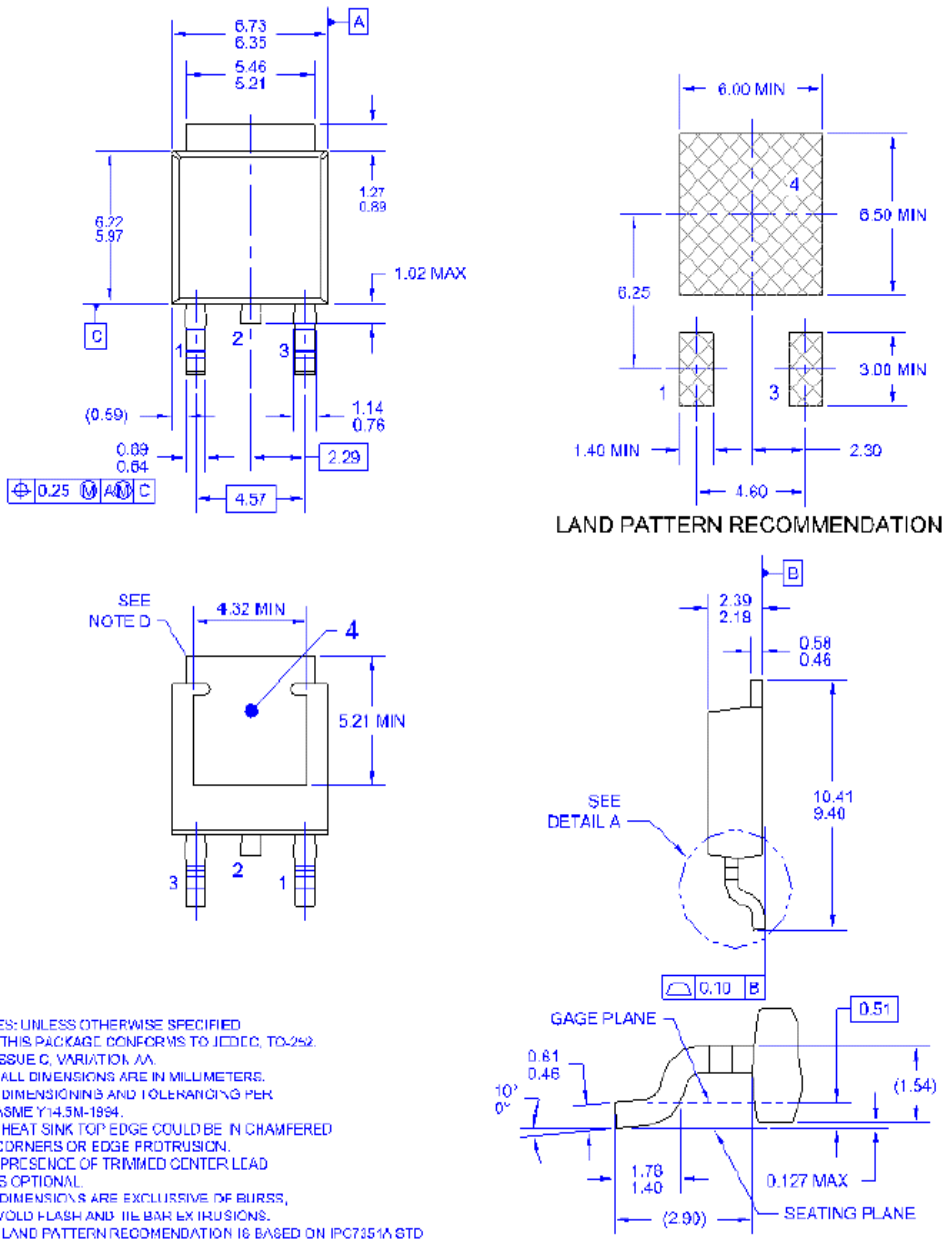




$$Qsync = \frac{1}{R_G} \cdot \int V_{R_G}(t)\ dt$$

Mechanical Dimensions

D-PAK



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.
F) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMENDATION IS BASED ON IPC7351A STD TO220P1003X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REVB

Dimensions in Millimeters

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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