

# BLF8G24L-200P; BLF8G24LS-200P

Power LDMOS transistor

Rev. 3 — 12 July 2013

Product data sheet

## 1. Product profile

### 1.1 General description

200 W LDMOS power transistor for base station applications at frequencies from 2300 MHz to 2400 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.

Test signal	f (MHz)	$I_{Dq}$ (mA)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)	ACPR <sub>5M</sub> (dBc)
1-carrier W-CDMA	2300 to 2400	1740	28	60	17.2	32	-37 <a href="#">[1]</a>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low  $R_{th}$  providing excellent thermal stability
- Designed for broadband operation (2300 MHz to 2400 MHz)
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

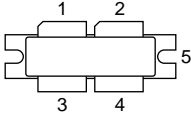
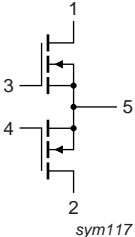
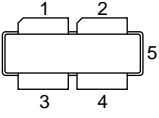
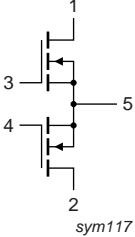
### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 2300 MHz to 2400 MHz frequency range



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF8G24L-200P (SOT539A)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
<b>BLF8G24LS-200P (SOT539B)</b>			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF8G24L-200P	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF8G24LS-200P	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	200	°C
$T_{case}$	case temperature		[1]	150	°C

[1] Continuous use at maximum temperature will affect the MTTF.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 60\text{ W}$	0.217	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  per section, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 100\text{ mA}$	1.5	1.9	2.3	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	26.8	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 5.1\text{ A}$	-	1.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5.04\text{ A}$	-	0.1	-	$\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA, PAR = 7.2 dB at 0.01 % probability on the CCDF, 3GPP test model 1; 64 DPCH;  $f_1 = 2300\text{ MHz}; f_2 = 2400\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 1740\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(AV)}$	average output power		-	60	-	W
$G_p$	power gain		15.8	17.2	-	dB
$RL_{in}$	input return loss		-	-11	-8	dB
$\eta_D$	drain efficiency		27	32	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)		-	-37	-33	dBc

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF8G24L-200P and BLF8G24LS-200P are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}; I_{Dq} = 1740\text{ mA}; P_L = 200\text{ W (CW)}; f = 2300\text{ MHz}$ .

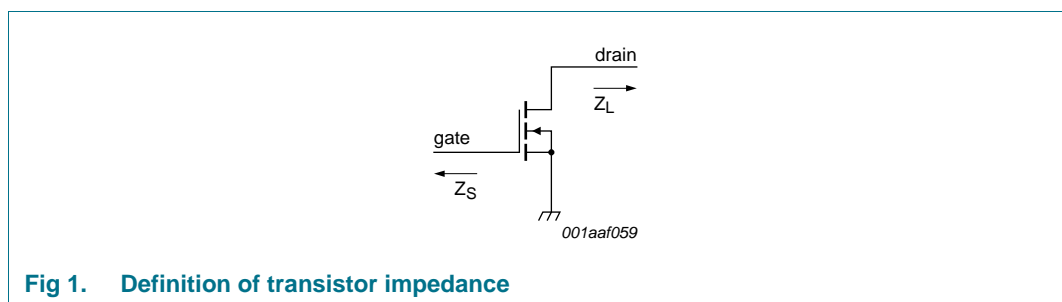
## 7.2 Impedance information

**Table 8. Typical impedance**

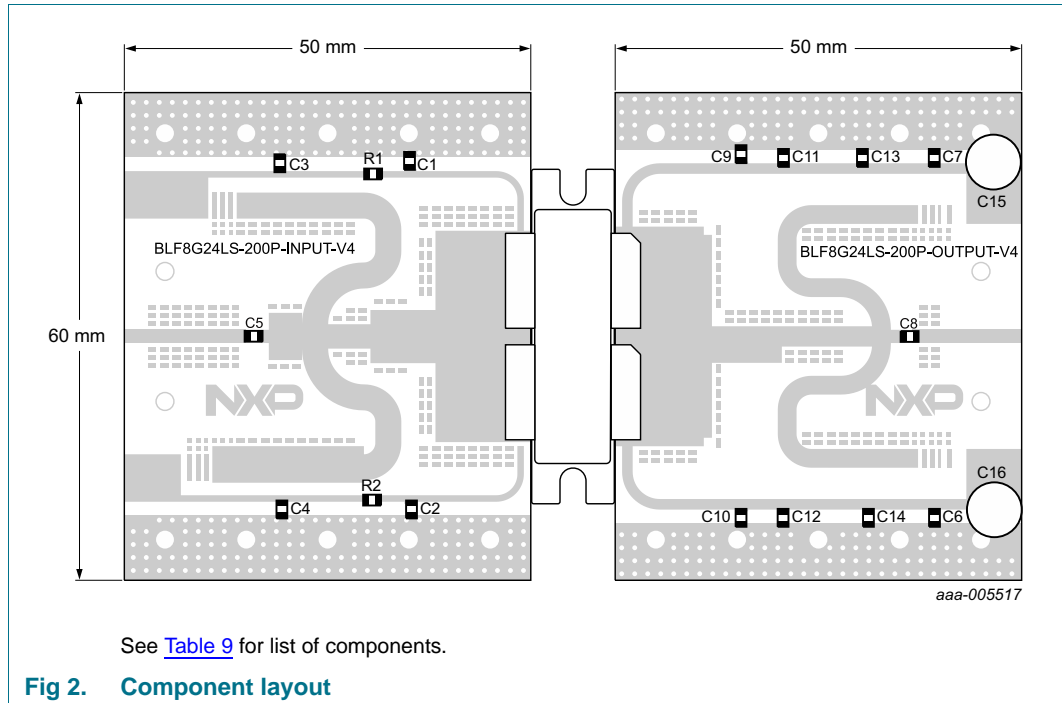
Measured load-pull data half section;  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 860\text{ mA}$ ; typical values unless otherwise specified.

f (MHz)	$Z_S$ <sup>[1]</sup> ( $\Omega$ )	$Z_L$ <sup>[1]</sup> ( $\Omega$ )
2300	4.24 – j6.5	1.5 – j5.4
2400	7.47 – j6.07	1.5 – j5.5

[1]  $Z_S$  and  $Z_L$  defined in [Figure 1](#).



## 7.3 Test circuit



**Table 9. List of components**

See [Figure 2](#) for component layout.

The used PCB material is Rogers RO4350B with a thickness of 0.76 mm.

Component	Description	Value	Remarks
C1, C2, C9, C10	multilayer ceramic chip capacitor	6.8 $\mu$ F	[1]
C3, C4, C6, C7	multilayer ceramic chip capacitor	1 $\mu$ F	[2]
C5, C8	multilayer ceramic chip capacitor	33 pF	[1]
C11, C12, C13, C14	multilayer ceramic chip capacitor	0.1 $\mu$ F	[2]
C15, C16	electrolytic capacitor	1000 $\mu$ F; 50 V	
R1, R2	chip resistor	5.1 $\Omega$	[3]

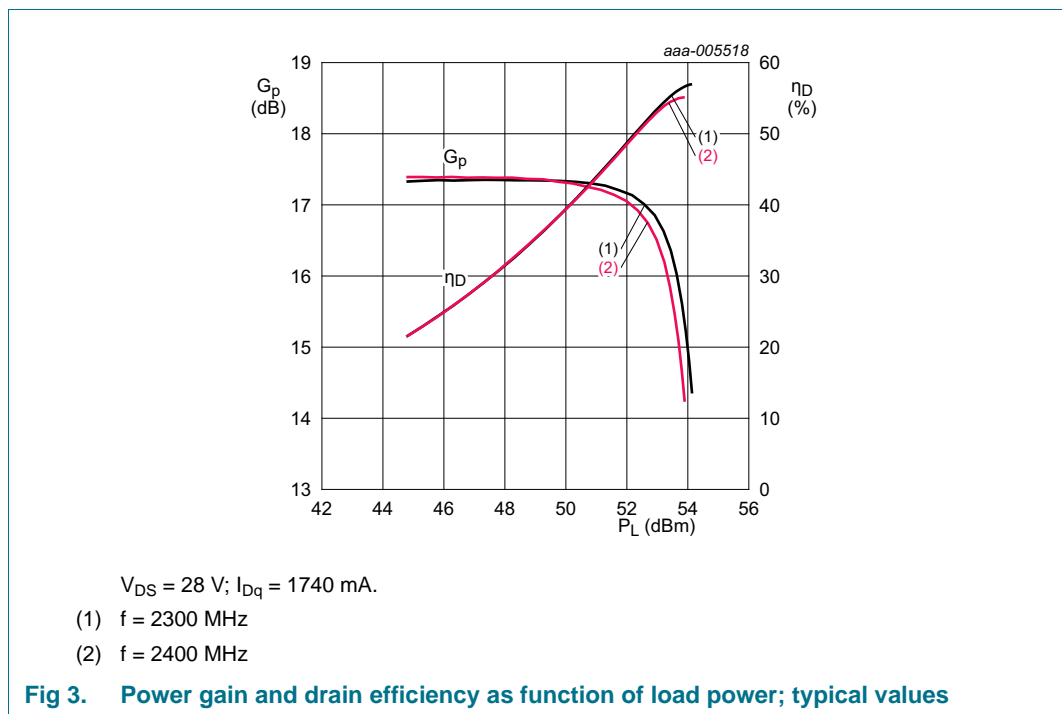
[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] Murata or capacitor of same quality.

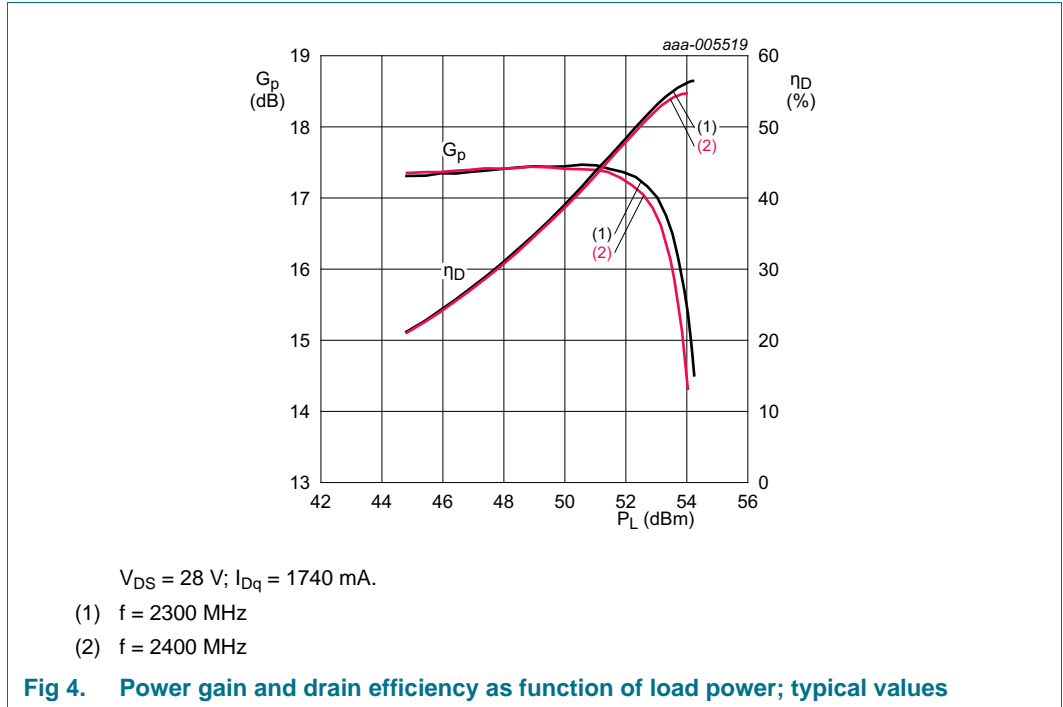
[3] Vishay Dale or resistor of same quality.

## 7.4 Graphical data

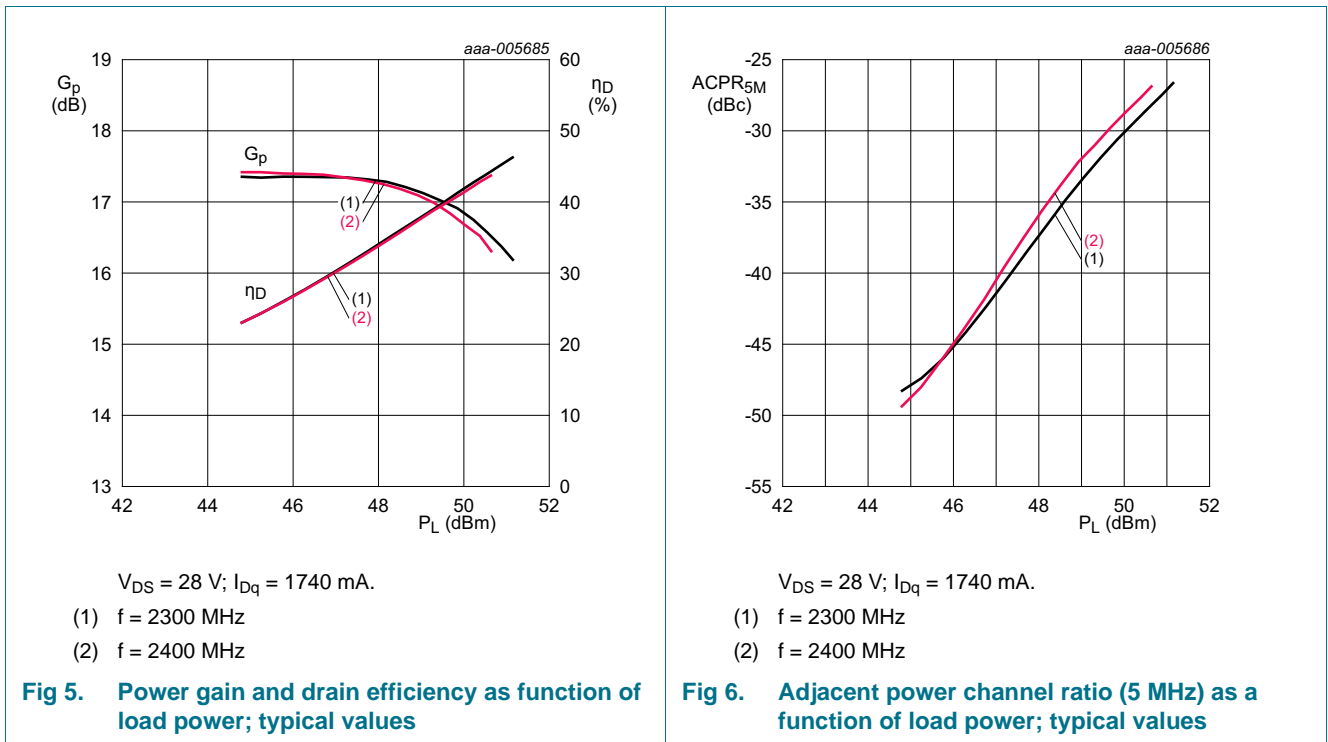
### 7.4.1 1-Tone CW

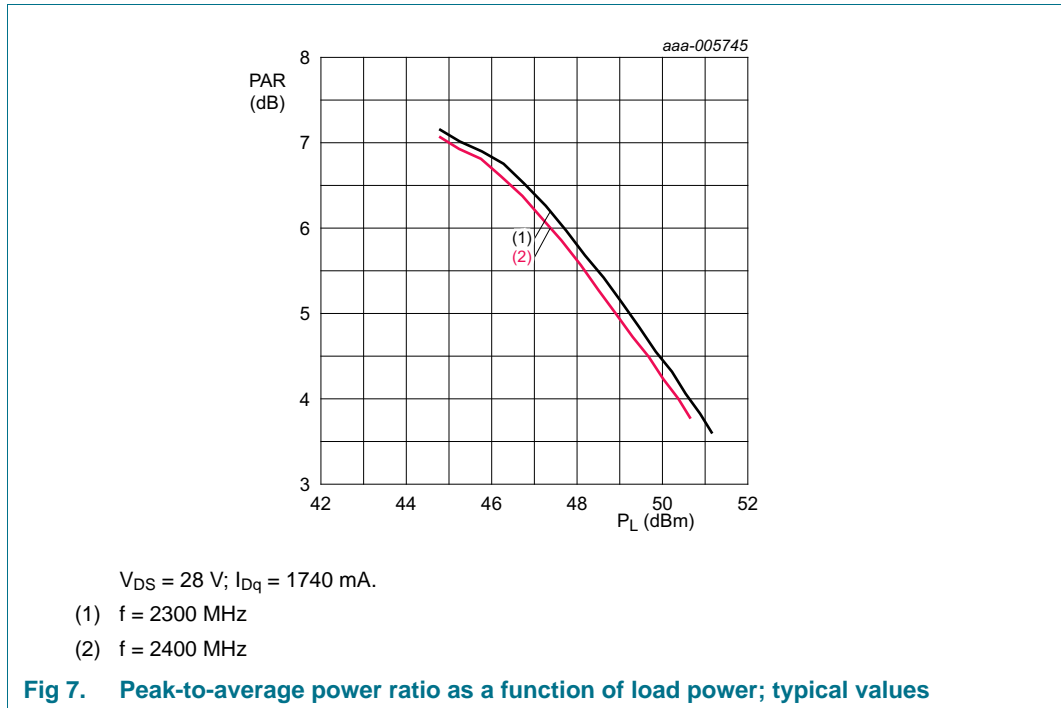


7.4.2 1-Tone CW pulsed



7.4.3 1-Carrier W-CDMA





8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

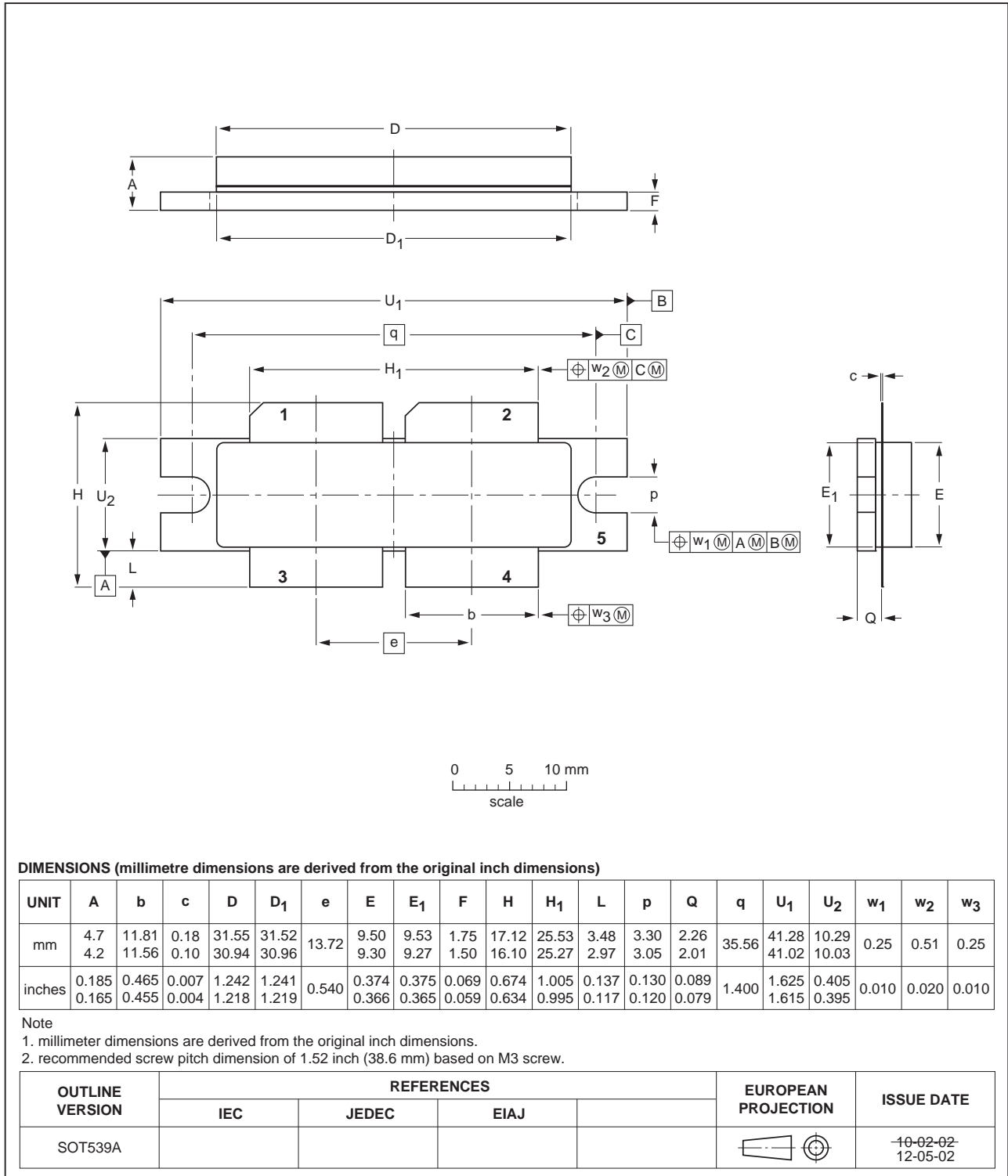


Fig 8. Package outline SOT539A



Earless flanged balanced ceramic package; 4 leads

SOT539B

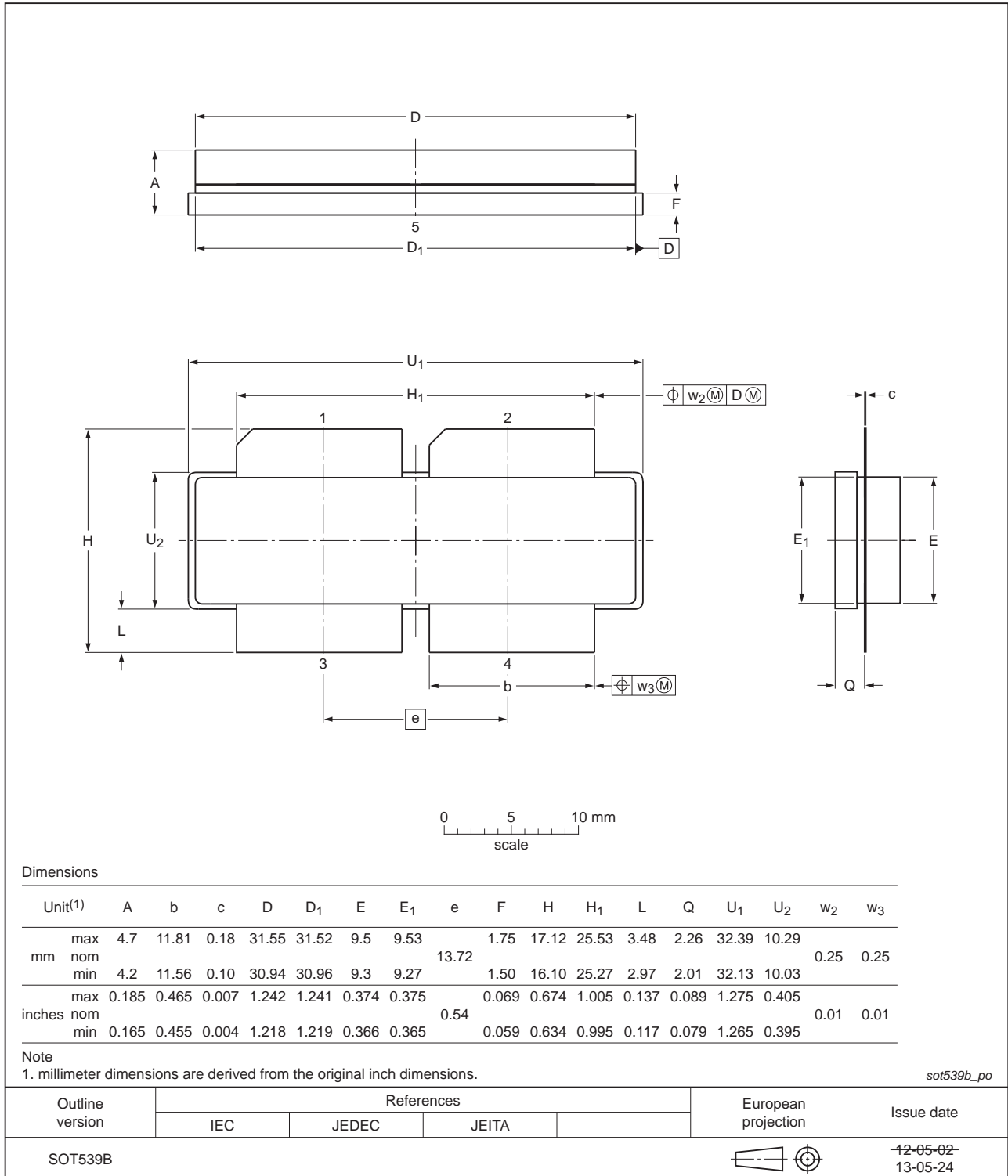


Fig 9. Package outline SOT539B

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
DPCH	Dedicated Physical Channel
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal Oxide Semiconductor
MTTF	Mean Time To Failure
PAR	Peak-to-Average Ratio
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G24L-200P_LS-200P v.3	20130712	Product data sheet	-	BLF8G24L-200P_LS-200P v.2
Modifications:	<ul style="list-style-type: none"> <li>The package outline <a href="#">Figure 9</a> is updated.</li> </ul>			
BLF8G24L-200P_LS-200P v.2	20121203	Product data sheet	-	BLF8G24L-200P_LS-200P v.1.1
Modifications:	<ul style="list-style-type: none"> <li>Table 1 on page 1: several changes.</li> <li>Table 4 on page 2: several changes.</li> <li>Table 5 on page 3: added typical value.</li> <li>Table 6 on page 3: changed several values.</li> <li>Table 7 on page 3: several changes.</li> <li>Table 7 on page 3: table moved to Section 6</li> <li>Section 7.1 on page 3: changed the value of <math>I_{Dq}</math>.</li> <li>Section 7.2 on page 4: added section.</li> <li>Section 7.3 on page 4: added section.</li> <li>Section 7.4 on page 5: added section.</li> <li>Section 9 on page 10: added section.</li> </ul>			
BLF8G24L-200P_LS-200P v.1.1	20120220	Objective data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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## 14. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>3</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>3</b>
<b>7</b>	<b>Test information</b> . . . . .	<b>3</b>
7.1	Ruggedness in class-AB operation . . . . .	3
7.2	Impedance information . . . . .	4
7.3	Test circuit . . . . .	4
7.4	Graphical data . . . . .	5
7.4.1	1-Tone CW . . . . .	5
7.4.2	1-Tone CW pulsed . . . . .	6
7.4.3	1-Carrier W-CDMA . . . . .	6
<b>8</b>	<b>Package outline</b> . . . . .	<b>8</b>
<b>9</b>	<b>Handling information</b> . . . . .	<b>10</b>
<b>10</b>	<b>Abbreviations</b> . . . . .	<b>10</b>
<b>11</b>	<b>Revision history</b> . . . . .	<b>10</b>
<b>12</b>	<b>Legal information</b> . . . . .	<b>11</b>
12.1	Data sheet status . . . . .	11
12.2	Definitions . . . . .	11
12.3	Disclaimers . . . . .	11
12.4	Trademarks . . . . .	12
<b>13</b>	<b>Contact information</b> . . . . .	<b>12</b>
<b>14</b>	<b>Contents</b> . . . . .	<b>13</b>

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