

# 74VHC123AFT,74VHC221AFT

## 1. Functional Description

- Dual Monostable Multivibrator  
74VHC123AFT: Retriggerable  
74VHC221AFT: Non-Retriggerable

## 2. General

The 74VHC123A/221AFT are high speed CMOS MONOSTABLE MULTIVIBRATOR fabricated with silicon gate C<sup>2</sup>MOS technology.

There are two trigger inputs,  $\bar{A}$  input (negative edge), and B input (positive edge). These inputs are valid for a slow rise/fall time signal ( $t_r = t_f = 1$  s) as they are schmitt trigger inputs. This device may also be triggered by using  $\bar{CLR}$  input (positive edge).

After triggering, the output stays in a MONOSTABLE state for a time period determined by the external resistor and capacitor ( $R_X, C_X$ ). A low level at the  $\bar{CLR}$  input breaks this state.

Limits for  $C_X$  and  $R_X$  are:

External capacitor,  $C_X$ : No limit

External resistor,  $R_X$ :  $V_{CC} = 2.0$  V more than 5 k $\Omega$

$V_{CC} \geq 3.0$  V more than 1 k $\Omega$

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

## 3. Features (Note)

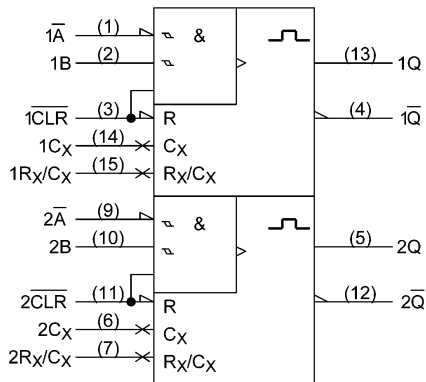
- (1) High speed: Propagation delay time = 8.1 ns (typ.) at  $V_{CC} = 5$  V
- (2) Low power dissipation:
  - Standby state: 4  $\mu$ A (max) at  $T_a = 25$  °C
  - Active state: 750  $\mu$ A (max) at  $T_a = 25$  °C
- (3) High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- (4) Power-down protection is provided on all inputs.
- (5) Balanced propagation delays:  $t_{PLH} \approx t_{PHL}$
- (6) Wide operating voltage range:  $V_{CC(opr)} = 2$  V to 5.5 V
- (7) Pin and function compatible with 74HC123,74HC221 type.

Note: In the case of using only one circuit,  $\bar{CLR}$  should be tied to GND,  $R_X/C_X \cdot C_X \cdot Q \cdot$  should be tied to OPEN, the other inputs should be tied to  $V_{CC}$  or GND.

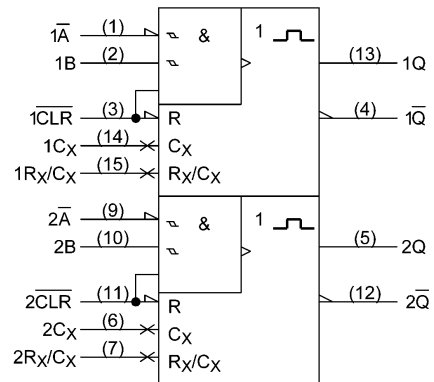


**7. IEC Logic Symbol**

74VHC123AFT



74VHC221AFT



**8. Truth Table**

Inputs			Outputs		Function
$\bar{A}$	B	$\bar{CLR}$	Q	$\bar{Q}$	
	H	H			Output Enable
X	L	H	L	H	Inhibit
H	X	H	L	H	Inhibit
L		H			Output Enable
L	H				Output Enable
X	X	L	L	H	Reset

X: Don't care

**9. Block Diagram**

- (1)  $C_X$ ,  $R_X$ ,  $D_X$  are external  
Capacitor, resistor, and diode, respectively.
- (2) External clamping diode,  $D_X$ ;

The external capacitor is charged to  $V_{CC}$  level in the wait state, i.e. when no trigger is applied. If the supply voltage is turned off,  $C_X$  is discharged mainly through the internal (parasitic) diode. If  $C_X$  is sufficiently large and  $V_{CC}$  drops rapidly, there will be some possibility of damaging the IC through inrush current or latch-up. If the capacitance of the supply voltage filter is large enough and  $V_{CC}$  drops slowly, the inrush current is automatically limited and damage to the IC is avoided.

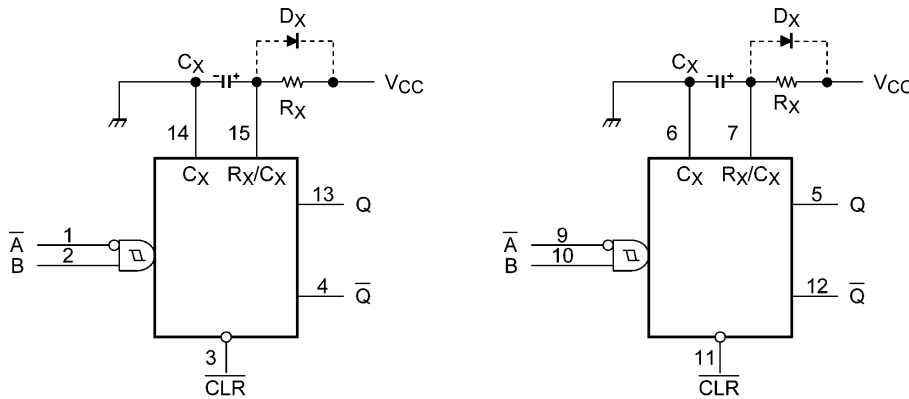
The maximum value of forward current through the parasitic diode is  $\pm 20$  mA.

In the case of a large  $C_X$ , the limit of fall time of the supply voltage is determined as follows:

$$t_f \geq (V_{CC} - 0.7) C_X / 20 \text{ mA}$$

( $t_f$  is the time between the supply voltage turn off and the supply voltage reaching  $0.4 V_{CC}$ .)

In the even a system does not satisfy the above condition, an external clamping diode ( $D_X$ ) is needed to protect the IC from inrush current.



10. System Diagram

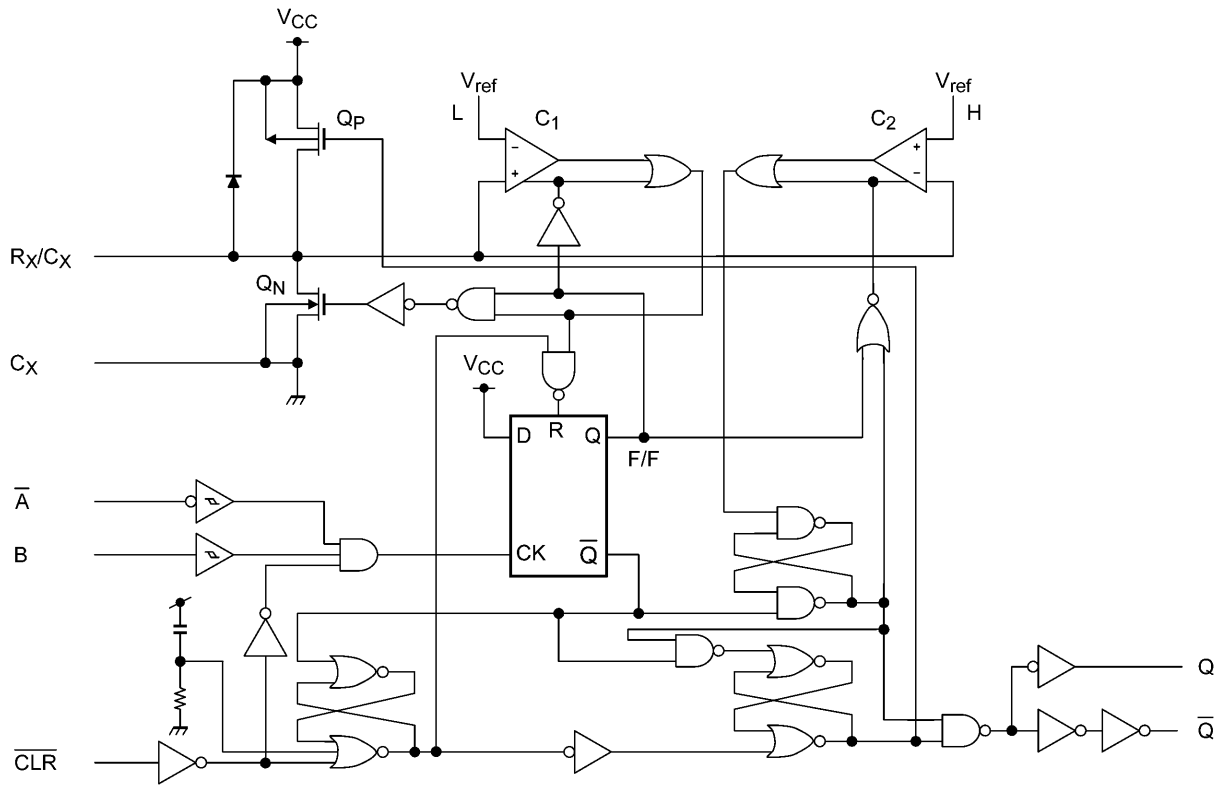


Fig. 10.1 74VHC123AFT

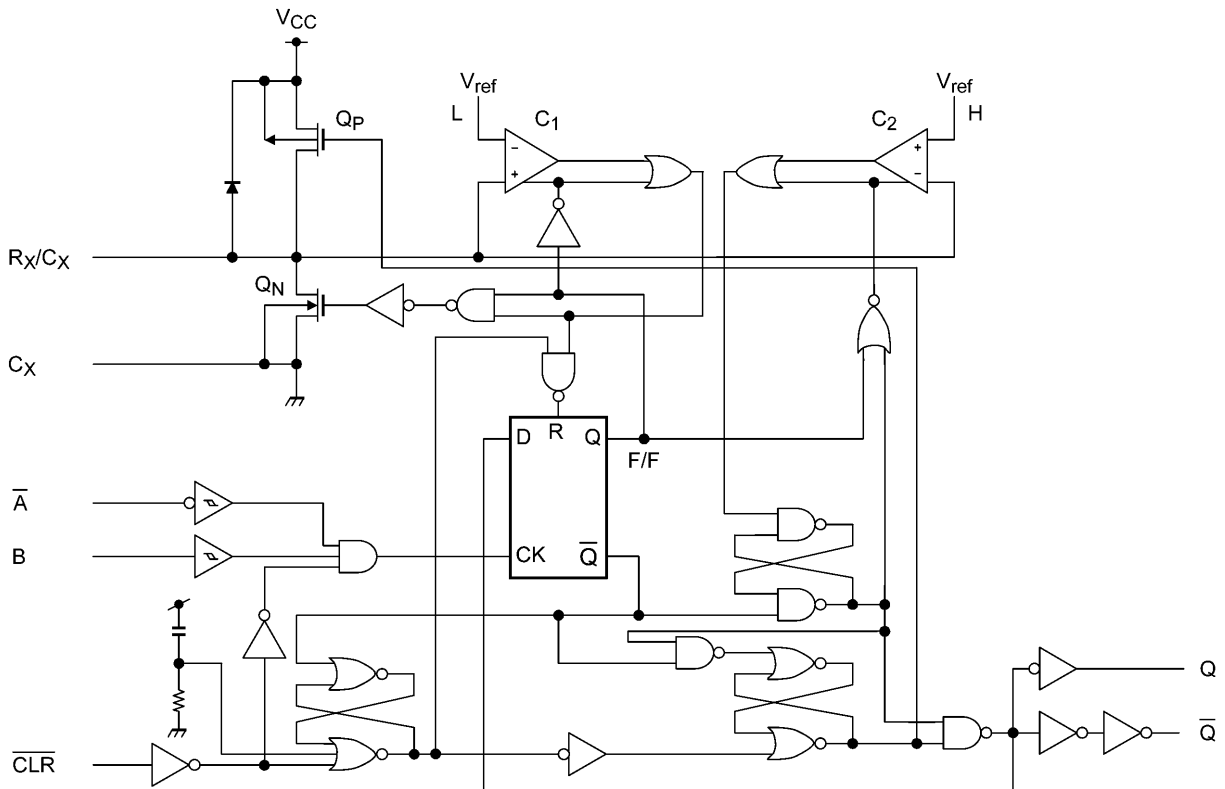


Fig. 10.2 74VHC221AFT

11. Timing Chart

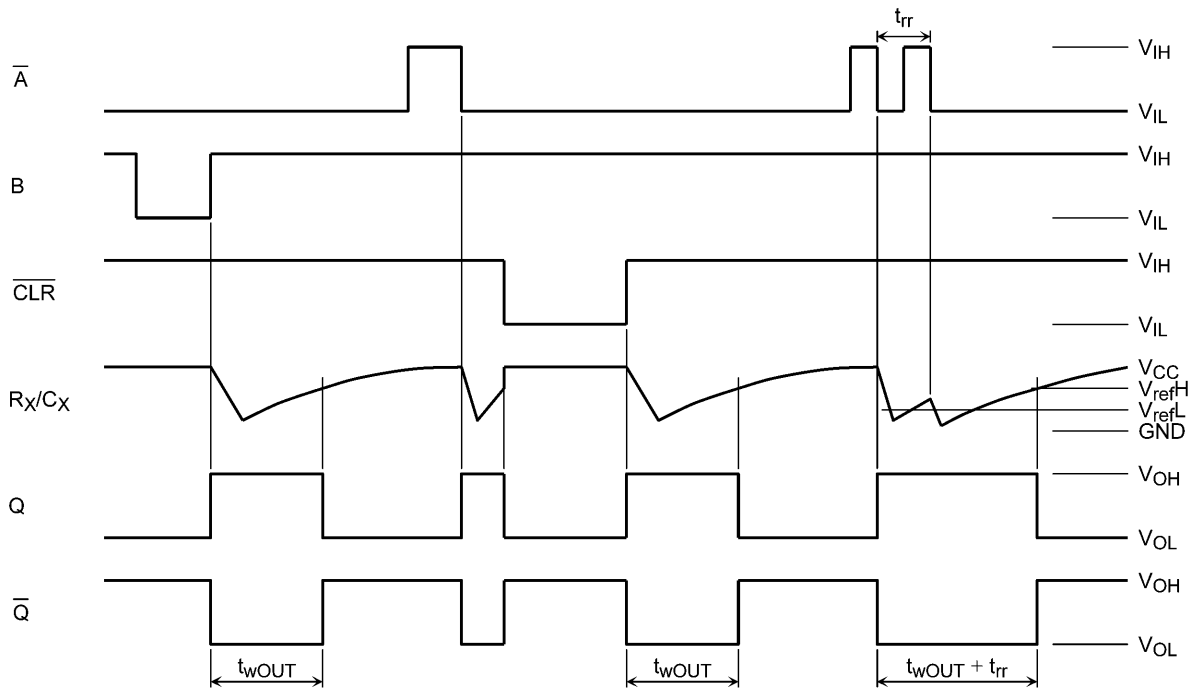


Fig. 11.1 74VHC123AFT

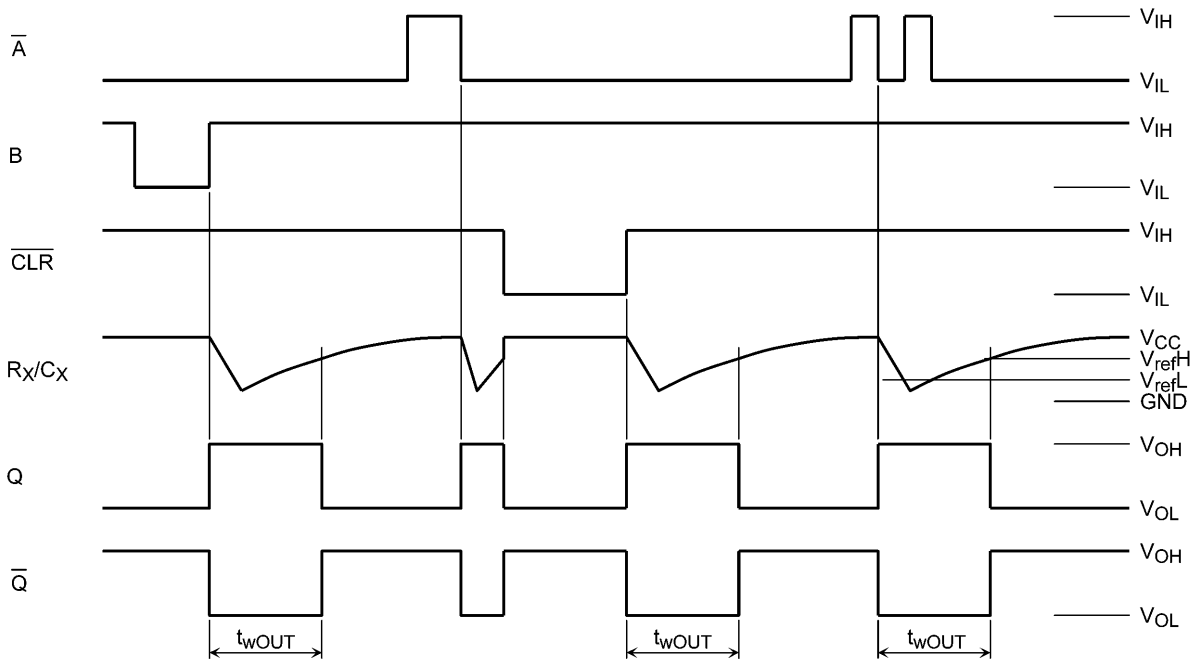


Fig. 11.2 74VHC221AFT

## 12. Functional Description

### (1) Standby state

The external capacitor ( $C_X$ ) is fully charged to  $V_{CC}$  in the stand-by state. That means, before triggering, the  $Q_P$  and  $Q_N$  transistors which are connected to the  $R_X/C_X$  node are in the off state. Two comparators that relate to the timing of the output pulse, and two reference voltage supplies turn off. The total supply current is only leakage current.

### (2) Trigger operation

Trigger operation is effective in any of the following three cases. First, the condition where the  $\bar{A}$  input is low, and the B input has a rising signal; second, where the B input is high, and the  $\bar{A}$  input has a falling signal; and third, where the  $\bar{A}$  input is low and the B input is high, and the  $\overline{CLR}$  input has a rising signal. After a trigger becomes effective, comparators  $C_1$  and  $C_2$  start operating, and  $Q_N$  is turned on. The external capacitor discharges through  $Q_N$ . The voltage level at the  $R_X/C_X$  node drops. If the  $R_X/C_X$  voltage level falls to the internal reference voltage  $V_{refL}$ , the output of  $C_1$  becomes low. The flip-flop is then reset and  $Q_N$  turns off. At that moment  $C_1$  stops but  $C_2$  continues operating.

After  $Q_N$  turns off, the voltage at the  $R_X/C_X$  node starts rising at a rate determined by the time constant of external capacitor  $C_X$  and resistor  $R_X$ .

Upon triggering, output Q becomes high, following some delay time of the internal F/F and gates. It stays high even if the voltage of  $R_X/C_X$  changes from falling to rising. When  $R_X/C_X$  reaches the internal reference voltage  $V_{refH}$ , the output of  $C_2$  becomes low, the output Q goes low and  $C_2$  stops its operation. That means, after triggering, when the voltage level of the  $R_X/C_X$  node reaches  $V_{refH}$ , the IC returns to its MONOSTABLE state.

With large values of  $C_X$  and  $R_X$ , and ignoring the discharge time of the capacitor and internal delays of the IC, the width of the output pulse,  $t_{wOUT}$ , is as follows:

$$t_{wOUT} = 1.0 \times C_X \times R_X$$

### (3) Retrigger operation

When a new trigger is applied to either input  $\bar{A}$  or B while in the MONOSTABLE state, it is effective only if the IC is charging  $C_X$ . The voltage level of the  $R_X/C_X$  node then falls to  $V_{refL}$  level again. Therefore the Q output stays high if the next trigger comes in before the time period set by  $C_X$  and  $R_X$ .

If the new trigger is very close to previous trigger, such as an occurrence during the discharge cycle, it will have no effect.

The minimum time for a trigger to be effective 2 nd trigger,  $t_{tr}$  (min), depends on  $V_{CC}$  and  $C_X$ .(74VHC123AFT)

### (4) Reset operation

In normal operation, the  $\overline{CLR}$  input is held high. If  $\overline{CLR}$  is low, a trigger has no effect because the Q output is held low and the trigger control F/F is reset. Also,  $Q_P$  turns on and  $C_X$  is charged rapidly to  $V_{CC}$ . This means if  $\overline{CLR}$  is set low, the IC goes into a wait state.

**13. Absolute Maximum Ratings (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	-0.5 to 7.0	V
Input voltage	$V_{IN}$	-0.5 to 7.0	V
Output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
Output current	$I_{OUT}$	$\pm 25$	mA
$V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

**14. Operating Ranges (Note)**

Characteristics	Symbol	Note	Test Condition	Rating	Unit
Supply voltage	$V_{CC}$		—	2.0 to 5.5	V
Input voltage	$V_{IN}$		—	0 to 5.5	V
Output voltage	$V_{OUT}$		—	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$		—	-40 to 85	$^{\circ}C$
Input rise and fall times	$dt/dv$		$V_{CC} = 3.3 \pm 0.3 V$	0 to 100	ns/V
			$V_{CC} = 5 \pm 0.5 V$	0 to 20	
External capacitor	$C_X$	(Note 1)	—	No limitation	F
External resistor	$R_X$	(Note 1)	$V_{CC} = 2.0 V$	$\geq 5 k$	$\Omega$
			$V_{CC} \geq 3.0 V$	$\geq 1 k$	

Note: The operating ranges must be maintained to ensure the normal operation of the device.

Unused inputs and bus inputs must be tied to either  $V_{CC}$  or GND.

Note 1: The maximum allowable values of  $C_X$  and  $R_X$  are a function of leakage of capacitor  $C_X$ , the leakage of 74VHC123A/221AFT, and leakage due to board layout and surface resistance.

Susceptibility to externally induced noise signals may occur for  $R_X > 1 M\Omega$ .



**15. Electrical Characteristics**

**15.1. DC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Typ.	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
$I_{OH} = -8\text{ mA}$	4.5	3.94		—	—			
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
				$I_{OL} = 8\text{ mA}$	4.5	—	—	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	$\mu\text{A}$	
$R_X/C_X$ terminal OFF-state current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	$\pm 0.25$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	$\mu\text{A}$	
Active-state supply current (per circuit)	$I_{CC(opr)}$	$V_{IN} = V_{CC}$ or GND $R_X/C_X = 0.5 V_{CC}$	3.0	—	160	250	$\mu\text{A}$	
			4.5	—	380	500		
			5.5	—	560	750		

**15.2. DC Characteristics (Unless otherwise specified,  $T_a = -40$  to  $85\text{ }^\circ\text{C}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Min	Max	Unit	
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	0.50	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
$I_{OH} = -8\text{ mA}$	4.5	3.80		—			
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
				$I_{OL} = 8\text{ mA}$	4.5	—	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	$\pm 1.0$	$\mu\text{A}$	
$R_X/C_X$ terminal OFF-state current	$I_{IN}$	$V_{IN} = V_{CC}$ or GND	5.5	—	$\pm 2.5$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	40.0	$\mu\text{A}$	
Active-state supply current (per circuit)	$I_{CC(opr)}$	$V_{IN} = V_{CC}$ or GND $R_X/C_X = 0.5 V_{CC}$	3.0	—	280	$\mu\text{A}$	
			4.5	—	650		
			5.5	—	975		

**15.3. Timing Requirements (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Part Number	Symbol	Test Condition	$V_{CC}$ (V)	Typ.	Limit	Unit
Minimum pulse width		$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	—	5.0	ns
				$5.0 \pm 0.5$	—	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ )		$t_{w(L)}$	—	$3.3 \pm 0.3$	—	5.0	ns
				$5.0 \pm 0.5$	—	5.0	
Minimum retrigger time	74VHC123AFT	$t_{rr}$	$R_X = 1\text{ k}\Omega, C_X = 100\text{ pF}$	$3.3 \pm 0.3$	60	—	ns
				$5.0 \pm 0.5$	39	—	
			$R_X = 1\text{ k}\Omega, C_X = 0.01\text{ }\mu\text{F}$	$3.3 \pm 0.3$	1.5	—	$\mu\text{s}$
				$5.0 \pm 0.5$	1.2	—	

**15.4. Timing Requirements (Unless otherwise specified,  $T_a = -40\text{ to }85\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	Limit	Unit
Minimum pulse width	$t_{w(L)}, t_{w(H)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	
Minimum pulse width ( $\overline{\text{CLR}}$ )	$t_{w(L)}$	—	$3.3 \pm 0.3$	5.0	ns
			$5.0 \pm 0.5$	5.0	

**15.5. AC Characteristics (Unless otherwise specified,  $T_a = 25\text{ }^\circ\text{C}$ , Input:  $t_r = t_f = 3\text{ ns}$ )**

Characteristics	Symbol	Note	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Typ.	Max	Unit
Propagation delay time (A, B-Q, $\overline{Q}$ )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	13.4	20.6	ns
					50	—	15.9	24.1	
				$5.0 \pm 0.5$	15	—	8.1	12.0	
					50	—	9.6	14.0	
Propagation delay time (CLR trigger-Q, $\overline{Q}$ )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	14.5	22.4	ns
					50	—	17.0	25.9	
				$5.0 \pm 0.5$	15	—	8.7	12.9	
					50	—	10.2	14.9	
Propagation delay time (CLR-Q, $\overline{Q}$ )	$t_{PLH}, t_{PHL}$		—	$3.3 \pm 0.3$	15	—	10.3	15.8	ns
					50	—	12.8	19.3	
				$5.0 \pm 0.5$	15	—	6.3	9.4	
					50	—	7.8	11.4	
Output pulse width	$t_{wOUT}$		$C_X = 28\text{ pF}, R_X = 2\text{ k}\Omega$	$3.3 \pm 0.3$	50	—	160	240	ns
						—	133	200	
			$C_X = 0.01\text{ }\mu\text{F}, R_X = 10\text{ k}\Omega$	$3.3 \pm 0.3$	50	90	100	110	$\mu\text{s}$
						90	100	110	
			$C_X = 0.1\text{ }\mu\text{F}, R_X = 10\text{ k}\Omega$	$3.3 \pm 0.3$	50	0.9	1.0	1.1	ms
						0.9	1.0	1.1	
Output pulse width error between circuits (in same package)	$\Delta t_{wOUT}$		—			—	$\pm 1$	—	%
Input capacitance	$C_{IN}$		—			—	4	10	pF
Power dissipation capacitance	$C_{PD}$	(Note 1)	—			—	73	—	

Note 1:  $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC'} \times \text{Duty}/100 + I_{CC}/2 \text{ (per circuit),}$$

( $I_{CC}$ : Active supply current),

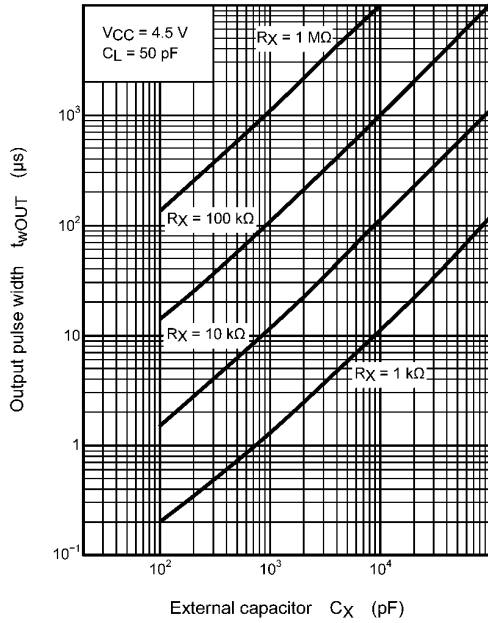
(Duty: %)

**15.6. AC Characteristics**

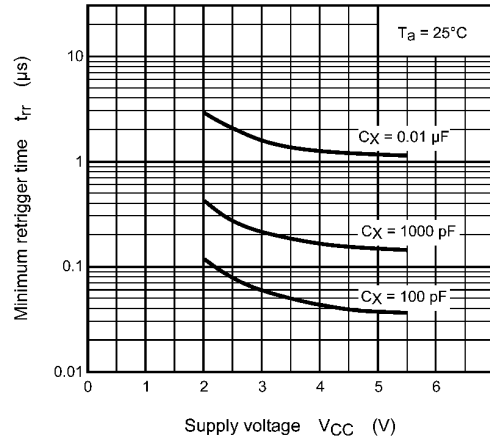
(Unless otherwise specified,  $T_a = -40$  to  $85$  °C, Input:  $t_r = t_f = 3$  ns)

Characteristics	Symbol	Test Condition	$V_{CC}$ (V)	$C_L$ (pF)	Min	Max	Unit		
Propagation delay time (A, B-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	24.0	ns		
				50	1.0	27.5			
			$5.0 \pm 0.5$	15	1.0	14.0			
				50	1.0	16.0			
Propagation delay time (CLR trigger-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	26.0	ns		
				50	1.0	29.5			
			$5.0 \pm 0.5$	15	1.0	15.0			
				50	1.0	17.0			
Propagation delay time (CLR-Q, $\bar{Q}$ )	$t_{PLH}, t_{PHL}$	—	$3.3 \pm 0.3$	15	1.0	18.5	ns		
				50	1.0	22.0			
			$5.0 \pm 0.5$	15	1.0	11.0			
				50	1.0	13.0			
Output pulse width	$t_{WOUT}$	$C_X = 28$ pF, $R_X = 2$ k $\Omega$	$3.3 \pm 0.3$	50	—	300	ns		
					5.0 $\pm$ 0.5	—		240	
			$C_X = 0.01$ $\mu$ F, $R_X = 10$ k $\Omega$	$3.3 \pm 0.3$	50	90		110	$\mu$ s
						5.0 $\pm$ 0.5		90	
		$C_X = 0.1$ $\mu$ F, $R_X = 10$ k $\Omega$	$3.3 \pm 0.3$	50	0.9	1.1	ms		
					5.0 $\pm$ 0.5	0.9		1.1	
		Input capacitance	$C_{IN}$	—			—	10	pF

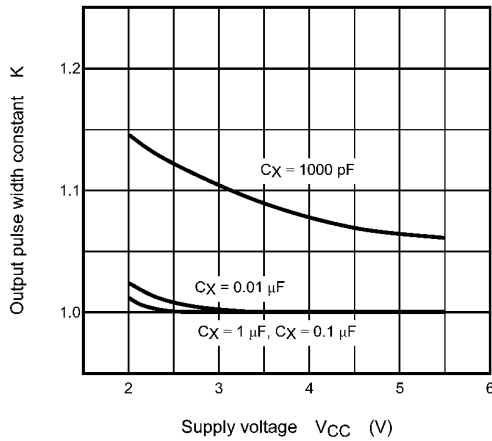
**16. Characteristics Curves (Note)**



**Fig. 16.1  $t_{wOUT}$  -  $C_X$  (typ.)**



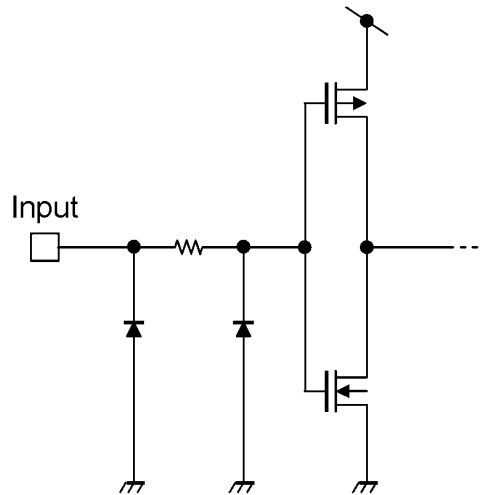
**Fig. 16.2  $t_r$  -  $V_{CC}$  (typ.) (74VHC123AFT)**



**Fig. 16.3 Output Pulse Width Constant K - Supply Voltage (typ.)**

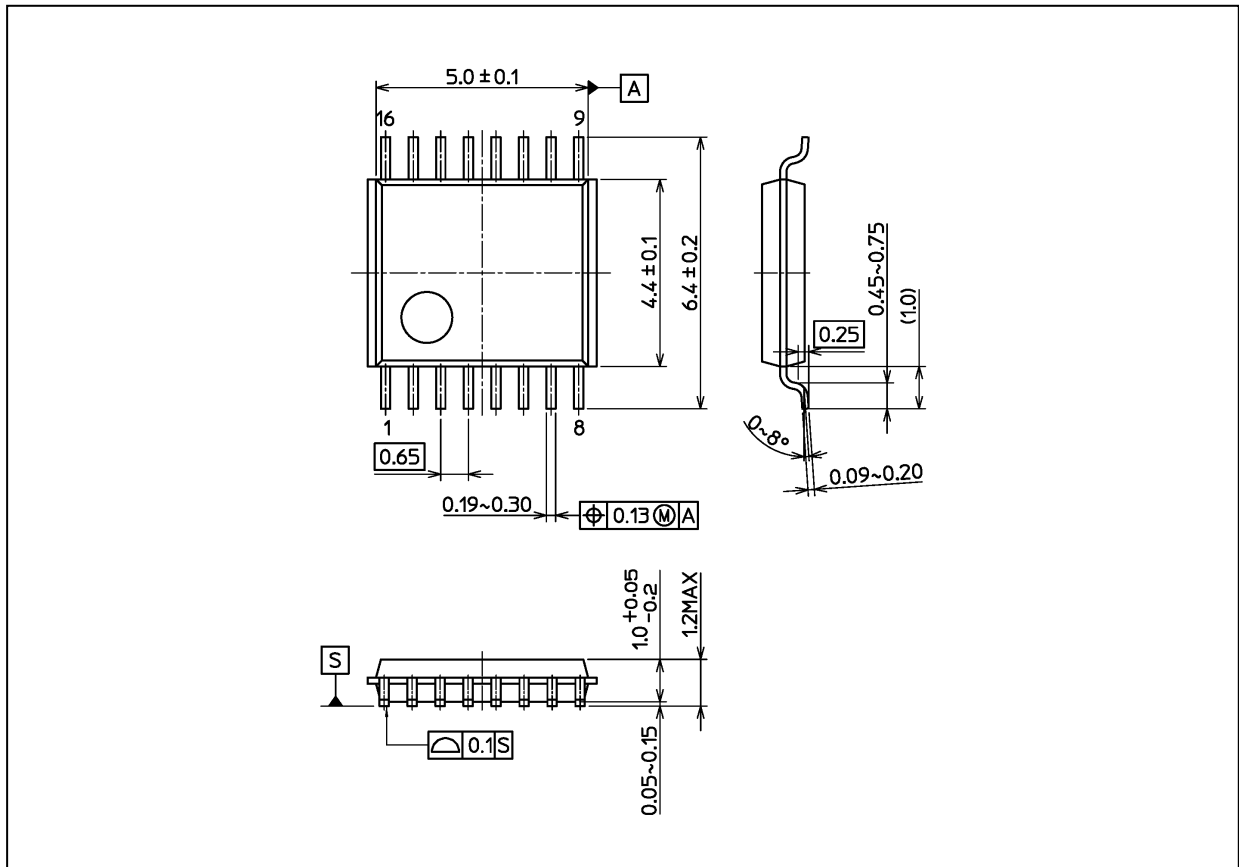
Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

17. Internal Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.055 g (typ.)

Package Name(s)
Nickname: TSSOP16B

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