Power supply IC series for TFT-LCD panels

12V Input Multi-Channel System Power Supply IC

BM81004MUV

General Description

BM81004MUV is a system power supply for TFT-LCD panels used for liquid crystal TVs. This IC is incorporated with Negative and Positive charge pump controller and Gate Pulse Modulation (GPM) function. It also features built-in EEPROM to contain each setting voltage, soft start time etc.

Features

- Step-up DC/DC converter (AVDD).
  (Synchronous rectification, Built-in load switch).
- Step-down DC/DC converter 1(VIO).
  (Non-synchronous rectification).
- Step-down DC/DC converter 2(VCORE).
- Step-down DC/DC converter 3(HAVDD).
  (Synchronous rectification).
- Positive charge pump controller (VGH).
- Negative charge pump controller (VGL).
- Gate Pulse Modulation (GPM) function.
- High Voltage LDO (50mA)
- 10 bit DAC-controlled Gamma Amplifier 4ch
- 8 bit DAC-controlled VCOM Amplifier
- Output voltage control by I2C.
- Built-in EEPROM.
- Switching Frequency 750kHz (AVDD, VIO).
- Switching Frequency 1MHz (VCORE, HAVDD).

Applications

- TFT-LCD panel

Key Specifications

Input voltage range :	8.6V to 14.0V
AVDD Output voltage range :	11.7V to 18.0V
VIO Output voltage range :	2.2V to 3.7V
HAVDD Output voltage range :	4.8V to 11.1V
VGH Output voltage range :	25V to 40.5V
VGL Output voltage range :	-10.2V to -4.0V
Switching Frequency :	750kHz(Typ) 1MHz(Typ)
Operating temperature range :	-40℃ to +105℃

Package

	W(Typ) x D(Typ) x H(Max)
VQFN48V7070A	7.00mm x 7.00mm x 1.0mm

Typical Application Circuit 1

(TOP VIEW)

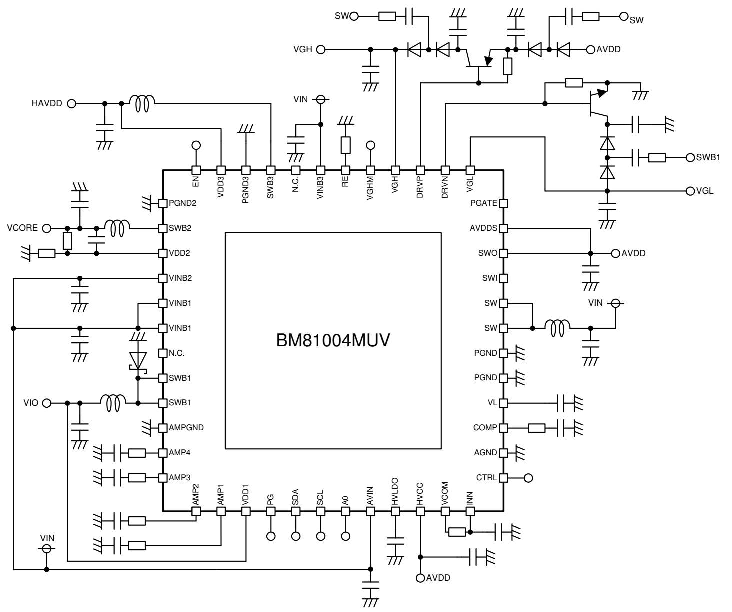


Figure 1. Application Circuit 1

○Product structure : Silicon monolithic chip ○This chip is not designed for protection against ratio active rays.

Typical Application Circuit 2
(TOP VIEW)

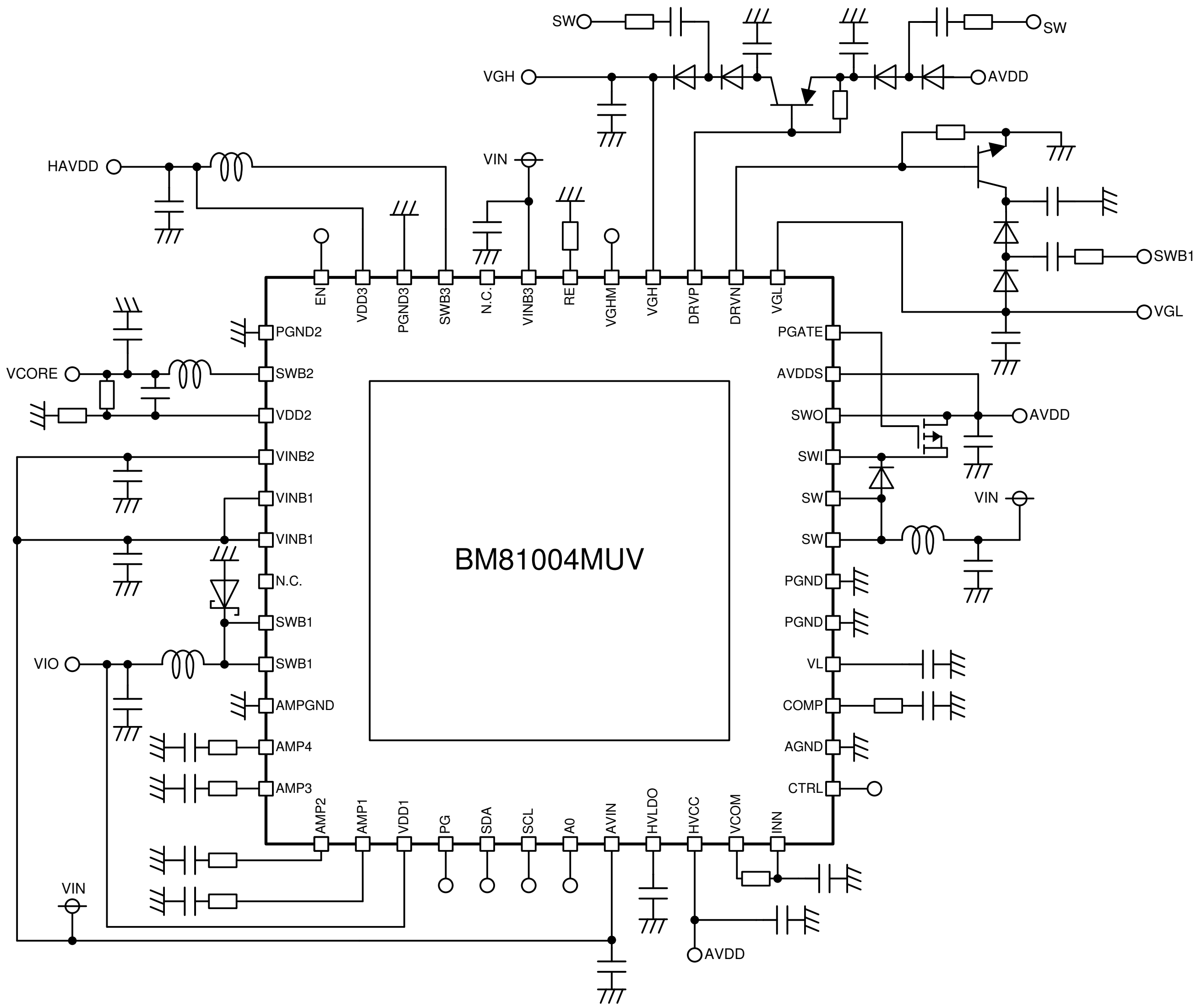


Figure 2. Application Circuit 2

Contents

Pin Configuration
(TOP VIEW)

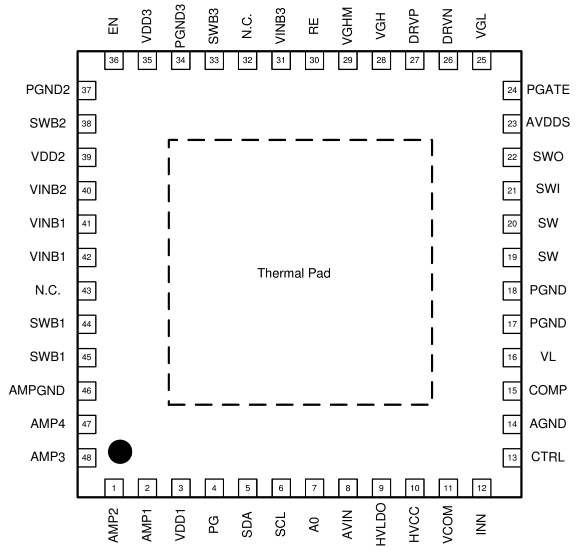


Figure 3. Pin Configuration

Pin Description

PIN No.	SYMBOL	FUNCTION	PIN No.	SYMBOL	FUNCTION
1	AMP2	Gamma amplifier output pin 2	25	VGL	Negative charge pump output pin
2	AMP1	Gamma amplifier output pin 1	26	DRVN	Negative charge pump drive pin
3	VDD1	Step-down DC/DC output pin 1	27	DRVP	Positive charge pump drive pin
4	PG	Power GOOD signal output pin	28	VGH	Positive charge pump output pin
5	SDA	Serial data input pin	29	VGHM	GPM output pin
6	SCL	Serial clock input pin	30	RE	GPM Slope adjustment pin
7	A0	I2C address selected pin	31	VINB3	Power supply pin for Step-down DC/DC 3
8	AVIN	Power supply input pin	32	N.C.	—
9	HVLDO	High Voltage LDO output pin	33	SWB3	Step-down DC/DC switching pin 3
10	HVCC	VCOM and Gamma power supply pin	34	PGND3	Step-down DC/DC GND pin 3
11	VCOM	VCOM amplifier output pin	35	VDD3	Step-down DC/DC output pin 3
12	INN	VCOM amplifier feedback pin	36	EN	Enable pin
13	CTRL	GPM control pin	37	PGND2	Step-down DC/DC GND pin 2
14	AGND	Analog GND pin	38	SWB2	Step-down DC/DC switching pin 2
15	COMP	Error amplifier output pin	39	VDD2	Step-down DC/DC output pin 2
16	VL	Internal REG output pin	40	VINB2	Power supply pin for Step-down DC/DC 2
17	PGND	Step-up DC/DC GND pin	41	VINB1	Power supply pin for Step-down DC/DC 1
18	PGND	Step-up DC/DC GND pin	42	VINB1	Power supply pin for Step-down DC/DC 1
19	SW	Step-up DC/DC switching pin	43	N.C.	—
20	SW	Step-up DC/DC switching pin	44	SWB1	Step-down DC/DC switching pin 1
21	SWI	Load switch input pin	45	SWB1	Step-down DC/DC switching pin 1
22	SWO	Load switch output pin	46	AMPGND	Gamma amplifier GND pin
23	AVDDS	Step-up DC/DC feedback pin	47	AMP4	Gamma amplifier output pin 4
24	PGATE	Load switch gate drive pin	48	AMP3	Gamma amplifier output pin 3

Block Diagram

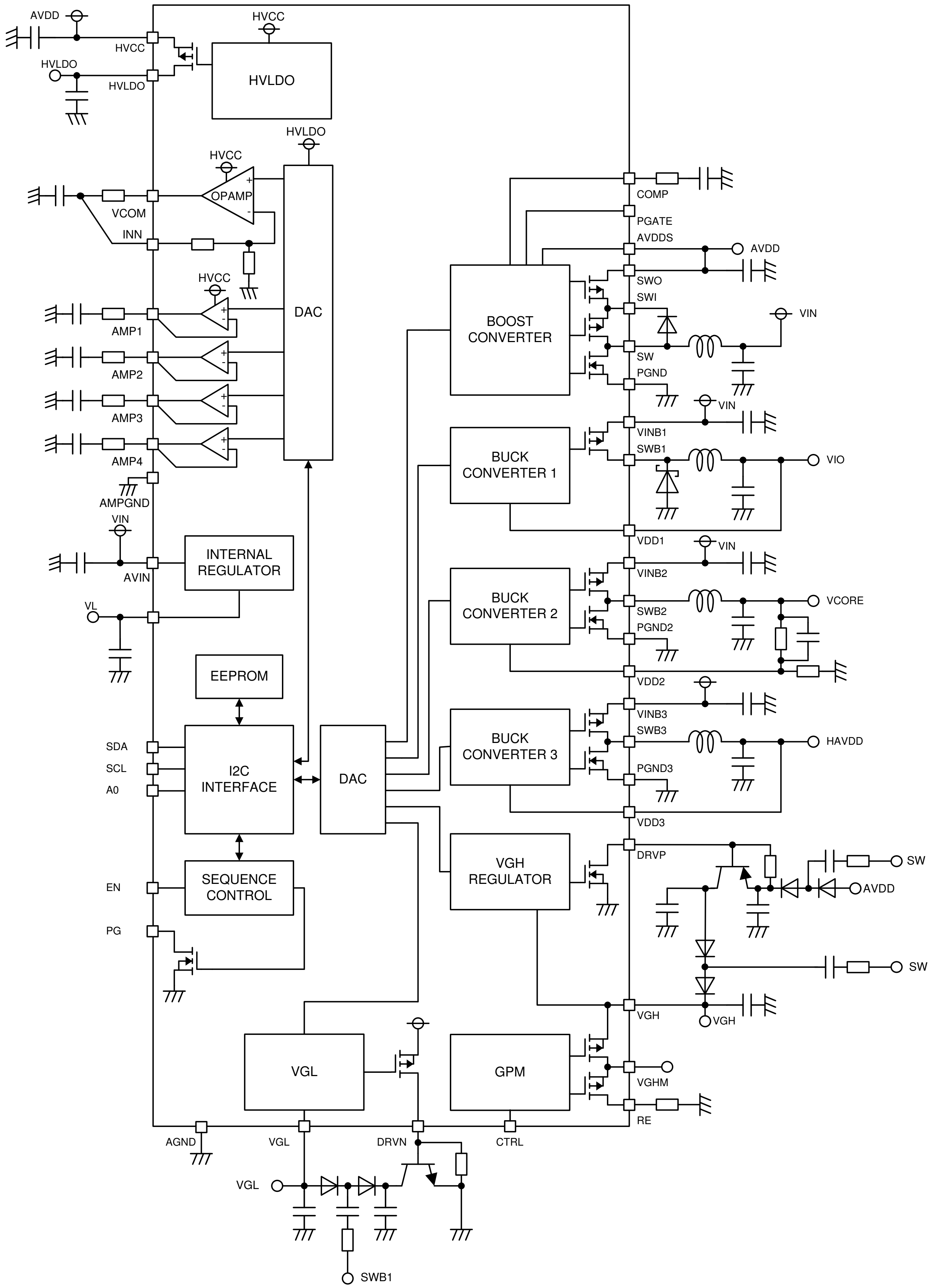


Figure 4. Block Diagram

Description of each Block

① BUCK CONVERTER BLOCK 2

This block generates VCORE (VDD2) voltage from Power supply voltage.
After releasing UVLO of VIN, VL starts activating. After Auto Read is operated to EEPROM, VCORE will be activated.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

② BUCK CONVERTER BLOCK 1

This block generates VIO (VDD1) voltage from Power supply voltage of VIO.
After completing VCORE start-up, VIO starts activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

③ VGL REGULATOR BLOCK

This block generates VGL voltage.
After completing VCORE start-up, VGL starts activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by UVP and OCP protection function.

④ BOOST CONVERTER BLOCK

This block generates AVDD (SWO) voltage from Power supply voltage.
It activates when EN=H, and under condition where VIO and VGL are activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

⑤ BUCK CONVERTER BLOCK 3

This block generates HAVDD (VDD3) voltage from Power supply voltage.
HAVDD starts up following AVDD output voltage.
The setting voltage range of the HAVDD voltage depends on the AVDD setting voltage, and the lower limit level of the HAVDD voltage is limited in AVDD × 0.4.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

⑥ HIGH VOLTAGE LDO BLOCK

This block generates HVLDO voltage from Power supply voltage of AVDD (HVCC).
HVLDO starts up following AVDD output voltage.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by UVP and OCP protection function.

⑦ VCOM AMPLIFIER BLOCK

This block generates VCOM voltage from Power supply voltage of AVDD (HVCC). VCOM calibrator function is built-in.
VCOM starts up following AVDD output voltage.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.

⑧ GAMMA AMPLIFIER BLOCK

This block generates AMP1 to 4 voltages from Power supply voltage of AVDD (HVCC).
AMP1 to 4 startup following AVDD output voltage.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.

⑨ VGH REGULATOR BLOCK

This block generates VGH voltage from AVDD voltage.
After completing AVDD start-up, VGH starts activating.
Power on Reset works at the time of VIN startup and the setting that is written to EEPROM will be reflected in Register.
During operations, it is possible to prevent destruction of IC by OVP, UVP and OCP protection function.

⑩ GPM BLOCK

This is a switching circuit to drive a gate voltage for TFT that consist of PMOS FET.
VGHM output synchronizes with CTRL input and outputs High voltage = VGH at CTRL=H.
GPM Falling Limit voltage can be controlled by EEPROM.

※ Caution

・EN Input tolerant function is built in this IC. No need to be always EN < VIN.
・When PG pin is not used, PG pin must be connected to GND, or it should be open.

Absolute Maximum Ratings

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN, VINB1, VINB2, VINB3	-0.3	-	24	V
	HVCC	-0.3	-	20	V
Input Voltage	SDA, SCL, A0, EN, CTRL	-0.3	-	7	V
Output Voltage	VL	-0.3	-	6.5	V
	COMP, PG	-0.3	-	7	V
	SW, SWI, SWO, PGATE, AVDDS, VDD1, SWB1, VDD2, SWB2, VDD3, SWB3	-0.3	-	24	V
	HVLDO, VCOM, INN AMP1, AMP2, AMP3, AMP4	-0.3	-	20	V
	VGL, DRVN	-15	-	7	V
	DRVP, VGH, VGHM, RE	-0.3	-	48	V
Operating Ambient Temperature Range	Ta	-40	-	105	℃
Storage Temperature Range	Tstg	-55	-	150	℃
Maximum Continuous Junction Temperature	Tjmax (*1)	-	-	150	℃
Power Dissipation (*2)	Pd	5.08			W
	Θja	24.6			degC/W

*1 It shows junction temperature when stores.
*2 Derate by 40.6mW/℃ at Ta>25℃(on 4-layer 76.2mm×114.3mm×1.6mm glass epoxy board).

Recommended Operating Ranges
(Ta=-40℃～105℃)

Parameter	Symbol	Limits			Unit
		MIN	TYP	MAX	
Supply Voltage	AVIN	8.6	-	14	V
Functional pin voltage	EN, A0, CTRL	-0.1	-	5.5	V
2 wire serial pin voltage	SDA, SCL	-0.1	-	5.5	V
2 wire serial frequency	FCLK	-	-	400	kHz

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 GENERAL 】						
VIN Under Voltage Lockout Threshold	VIN_UVLO	8.0	8.3	8.6	V	VIN rising
		7.25	7.55	7.85	V	VIN falling
Thermal shutdown	TSD	155	175	195	℃	Design guarantee
Internal Oscillator Frequency 1	FOSC1	600	750	900	kHz	AVDD, VIO, 0 < Ta < 50℃
Internal Oscillator Frequency 2	FOSC2	800	1000	1200	kHz	VCORE, HAVDD, 0 < Ta < 50℃
VL Voltage	VL	4.9	5	5.1	V	
Consumption Current	ICC	-	5.4	-	mA	Not Switching
【 LOGIC SIGNALS SDA, SCL, EN, A0, CTRL 】						
High Level Input Voltage	VIH	2	-	-	V	
Low Level Input Voltage	VIL	-	-	0.5	V	
Minimum Output Voltage	VSDA	-	-	0.4	V	SDA, ISDA=3mA
Pull-Down Resistance	RLOGIC	140	200	260	kΩ	EN, A0, CTRL
【 BOOST CONVERTER (AVDD) 】						
Output Voltage Range	AVDD	11.7	-	18.0	V	0.1V step
Regulation Voltage	AVDD_R	15.444	15.6	15.756	V	27h, 1%, 0 < Ta < 50℃
Hi-Side Leakage Current	ILK_SWH	-	0	10	uA	SWI=18V, SW=0V
Hi-Side SW ON-Resistance	RON_SWH	-	100	200	mΩ	ISW=-500mA
Lo-Side SW Leakage Current	ILK_SWL	-	0	10	uA	SW=18V
Lo-Side SW ON-Resistance	RON_SWL	-	100	200	mΩ	ISW=500mA
Load SW ON-Resistance	RON_LS	-	100	200	mΩ	ILS=500mA
SW Current Limit	ILIM_SW	4.25	5	5.75	A	5.0A – Offset(0.0A) setting L=6.8uH, 0 < Ta < 50℃
SW Current Limit Offset	ILIM_SET	0	-	2.8	A	0.4A step
Over-Voltage Protection Rise	VOVP_AVDD_RISE	18	19.5	21	V	
Over-Voltage Protection Fall	VOVP_AVDD_FALL	-	18	-	V	
AVDD UVP Detecting Voltage	VUVP_AVDD	-	AVDD x 0.8	-	V	
Soft Start Time	TSS_AVDD	10	-	20	msec	
Load Switch Current Limit	ILIM_LSW	-	7	-	A	
External Load Switch Current Limit	ILIM_EXT	450	540	630	mV	
PGATE Drive Capability	PGATE_DRV	-	10	-	uA	

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 BUCK CONVERTER 1 (VIO) 】						
Output Voltage Range	VIO	2.2	-	3.7	V	0.1V step
Regulation Voltage	VIO_R	3.234	3.3	3.366	V	0Bh, 2%, 0 < Ta < 50℃
Hi-Side SWB1 Leak Current	ILK_SWB1H	-	0	10	uA	VINB1=18V, SWB1=0V
Hi-Side SWB1 ON-Resistance	RON_SWB1H	-	200	300	mΩ	SWB1=-500mA
SWB1 Current Limit	ILIM_SWB1	2.8	3.5	4.2	A	L=6.8uH, 0 < Ta < 50℃
VIO Over-Voltage Protection	VOVP_VIO	VIO x 1.03	VIO x 1.1	VIO x 1.17	V	
VIO UVP Detecting Voltage	VUVP_VIO	-	VIO x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VIO	-	3.3	-	msec	VIO=3.3V
【 BUCK CONVERTER 2 (VCORE) 】						
VCORE Reference Voltage	VCORE_REF	0.396	0.400	0.404	V	1%, Ta=25℃
		0.394	0.400	0.406	V	1.5%, 0 < Ta < 50℃
Hi-Side SWB2 Leak Current	ILK_SWB2H	-	0	10	uA	VINB2=18V, SWB2=0V
Hi-Side SWB2 ON-Resistance	RON_SWB2H	-	175	300	mΩ	SWB2=-500mA
Lo-Side SWB2 Leak Current	ILK_SWB2L	-	0	10	uA	SWB2=18V
Lo-Side SWB2 ON-Resistance	RON_SWB2L	-	175	300	mΩ	SWB2=500mA
SWB2 Current Limit	ILIM_SWB2	2.4	3.0	3.6	A	L=6.8uH, 0 < Ta < 50℃
VCORE Over-Voltage Protection	VOVP_VCORE	VCORE x 1.03	VCORE x 1.1	VCORE x 1.17	V	
VCORE UVP Detecting Voltage	VUVP_VCORE	-	VCORE x 0.8	-	V	Frequency 1/4
Soft Start Time	TSS_VCORE	-	3	-	msec	
【 BUCK CONVERTER 3 (HAVDD) 】						
Output Voltage Range	HAVDD	4.8	-	11.1	V	0.1V step
Regulation Voltage	HAVDD_R	7.68	7.8	7.92	V	1Eh, 1.5%, 0 < Ta < 50℃
Hi-Side SWB3 Leak Current	ILK_SWB3H	-	0	10	uA	VINB3=18V, SWB3=0V
Hi-Side SWB3 ON-Resistance	RON_SWB3H	-	300	500	mΩ	SWB3=-500mA
Lo-Side SWB3 Leak Current	ILK_SWB3L	-	0	10	uA	SWB3=18V
Lo-Side SWB3 ON-Resistance	RON_SWB3L	-	300	500	mΩ	SWB3=500mA
SWB3 Current Limit	ILIM_SWB3	1.2	1.8	2.4	A	L=6.8uH, 0 < Ta < 50℃
HAVDD Over-Voltage Protection	VOVP_HAVDD	HAVDD x 1.03	HAVDD x 1.1	HAVDD x 1.17	V	
HAVDD UVP Detecting Voltage	VUVP_HAVDD	-	HAVDD x 0.8	-	V	Frequency 1/4

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 VGH REGULATOR 】						
Output Voltage Range	VGH	25	-	40.5	V	0.5V step
Regulation Voltage	VGH_R	34.47	35	35.53	V	14h, 1.5%, 0 < Ta < 50℃ Io=5mA
Over-Current Protection	ILIM_DRVP	5	-	-	mA	
VGH Over-Voltage Protection	VOVP_VGH	42	45	48	V	
VGH UVP Detecting Voltage	VUVP_VGH	-	VGH x 0.8	-	V	
Soft Start Time	TSS_VGH	-	7	-	msec	VGH=35V
【 VGL REGULATOR 】						
Output Voltage Range	VGL	-10.2	-	-4.0	V	0.2V step
Regulation Voltage	VGL_R	-6.09	-6	-5.91	V	0Ah, 1.5%, Ta=25℃ Io=5mA
		-6.12	-6	-5.88	V	0Ah, 2.0%, 0 < Ta < 50℃ Io=5mA
Over-Current Protection	ILIM_DRVN	5	-	-	mA	
VGL UVP Detecting Voltage	VUVP_VGL	-	VGL×0.8	-	V	
Delay Time	TDLY_VGL	-	2.5	-	msec	
【 GATE PULSE MODULATION (GPM) 】						
VGH-VGHM ON-Resistance	RGHH	-	3	5	Ω	
RE-VGHM ON-Resistance	RGHL	-	3	-	Ω	
Propagation Delay	TGPM	150	250	350	nsec	

Electrical Characteristics

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V)

Parameter	Symbol	Limits			Unit	Condition
		MIN	TYP	MAX		
【 HIGH VOLTAGE LDO 】						
Output Voltage Range	LDO	11.7	—	18.0	V	0.1V step
Regulation Voltage	LDO_R	15.12	15.2	15.28	V	23h, 0.5%
	LDO_R	15.09	15.2	15.31	V	23h, 0.7%, 0 < Ta < 50℃
Over-Current Protection	ILIM_ LDO	-	100	-	mA	
HVLDO UVP Detecting Voltage	LDO_UVP	-	LDOx0.8	-	V	
【 VCOM AMPLIFIER 】						
Output Voltage Range	VCOM_R	HVLDO X0.36	—	HVLDO X0.54	V	
Slew Rate	SR	-	30	-	V/usec	No external components
Output Current Capability	I_VCOM	-	±200	-	mA	C2h
Load Stability	ΔVO1	-	±15	-	mV	Io=-50mA～50mA
DAC Resolution	RES1		8		Bit	
DAC Integral Non-linearity Error (INL)	LE1	-1	-	+1	LSB	02～FD is the allowable margin of error against the ideal linear.
DAC Differential Non-linearity Error (DNL)	DLE1	-1	-	+1	LSB	02～FD is the allowable margin of error against the ideal increase of 1LSB.
【 GAMMA AMPLIFIER 】						
Output Current Capability	I_AMP	30	-	-	mA	
Load Stability	ΔVO2	-	±15	-	mV	Io=-5mA～5mA
DAC Resolution	RES2		10		Bit	
DAC Integral Non-linearity Error (INL)	LE2	-2	-	+2	LSB	00F ～ 3F0 is the allowable margin of error against the ideal linear.
DAC Differential Non-linearity Error (DNL)	DLE2	-2	-	+2	LSB	00F ～ 3F0 is the allowable margin of error against the ideal increase of 1LSB.

○This product has no designed for protection against radioactive rays.

Typical Performance Curves
(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

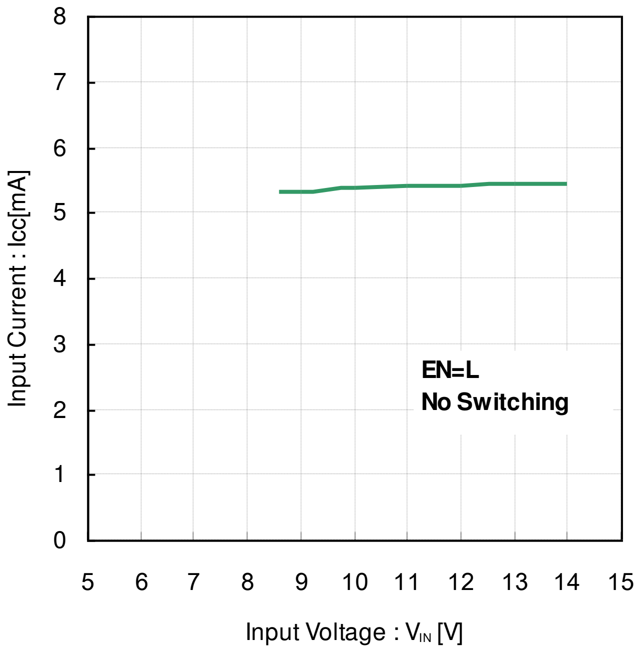


Figure 5. Input Current vs Input Voltage
(EN=L, no switching)

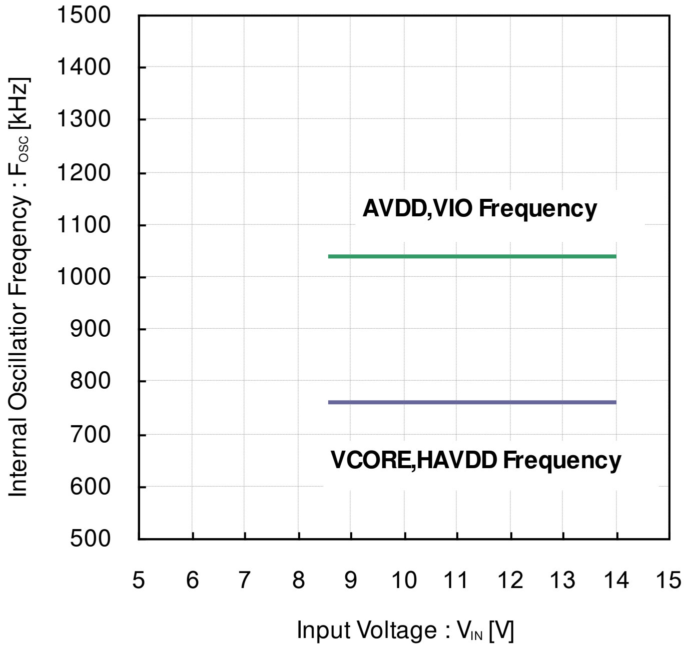


Figure 6. Internal Oscillator Frequency vs Input Voltage

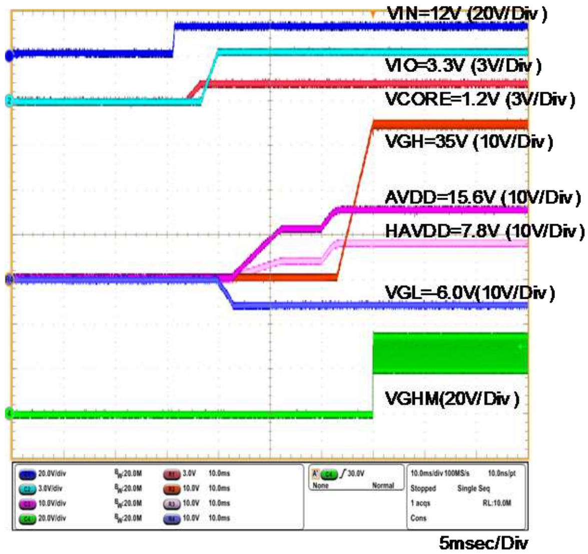


Figure 7. Power-on (till AVDD and VGH on)

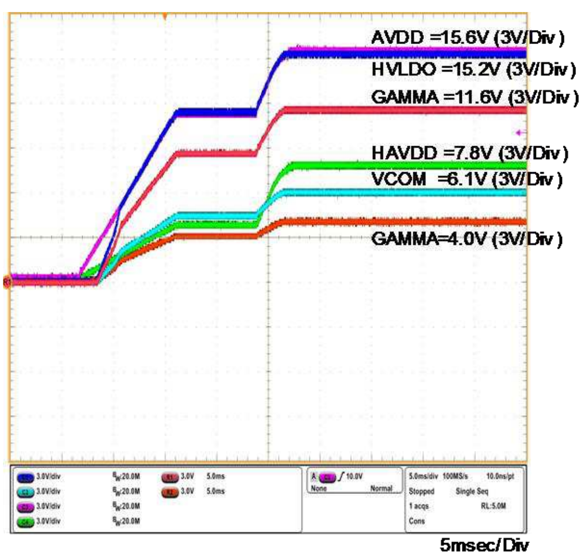


Figure 8. Power-on (after AVDD on)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

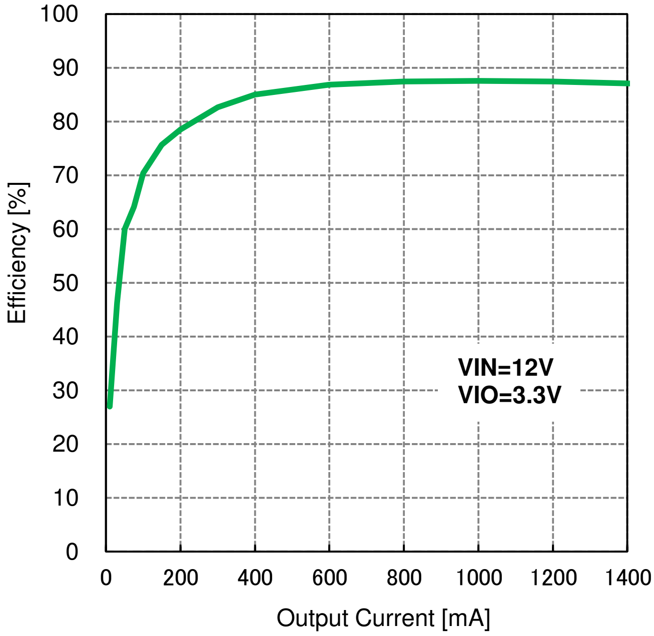


Figure 9. VIO Efficiency vs Output Current

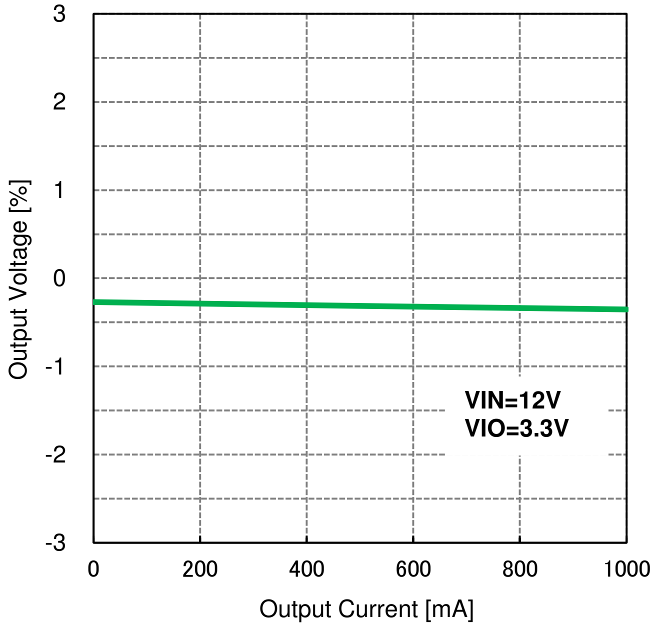


Figure 10. VIO Output Voltage vs Output Current

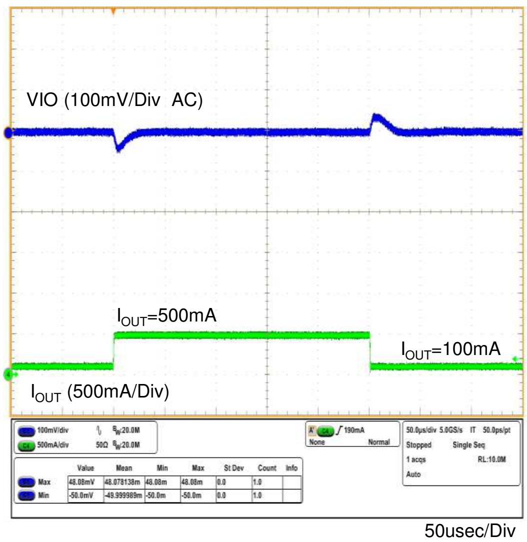


Figure 11. VIO Load Transient

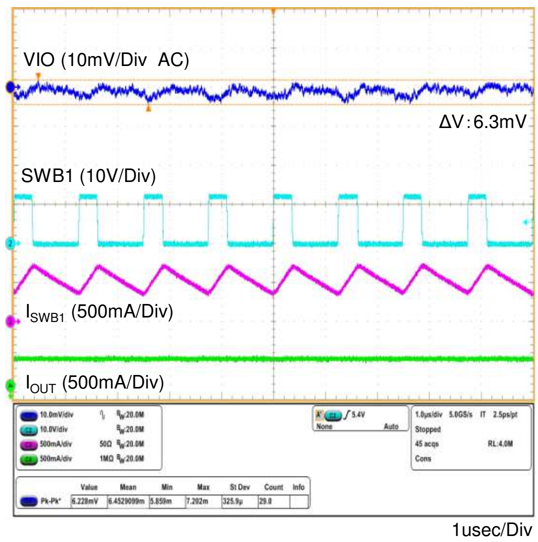


Figure 12. VIO Switching
(Output Current=500mA)

Typical Performance Curves
(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

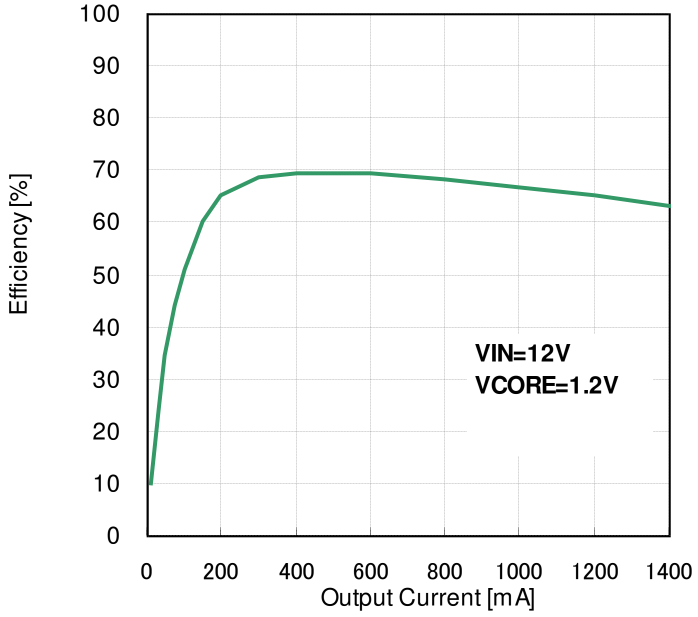


Figure 13. VCORE Efficiency vs Output Current

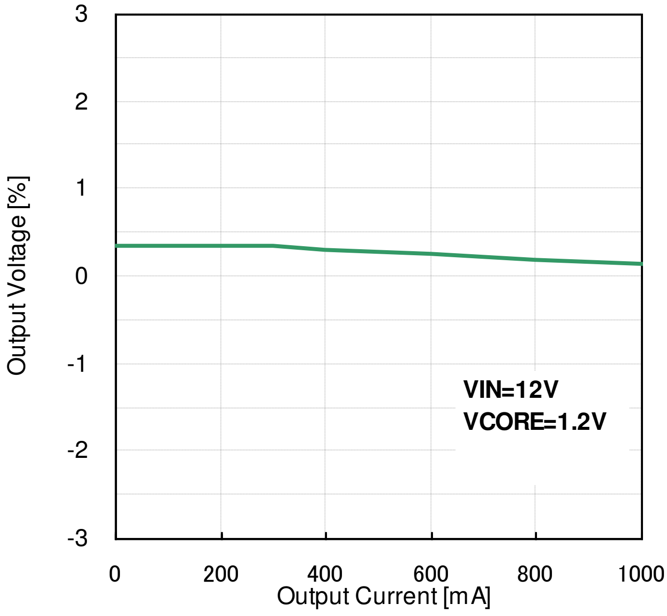


Figure 14. VCORE Output Voltage vs Output Current

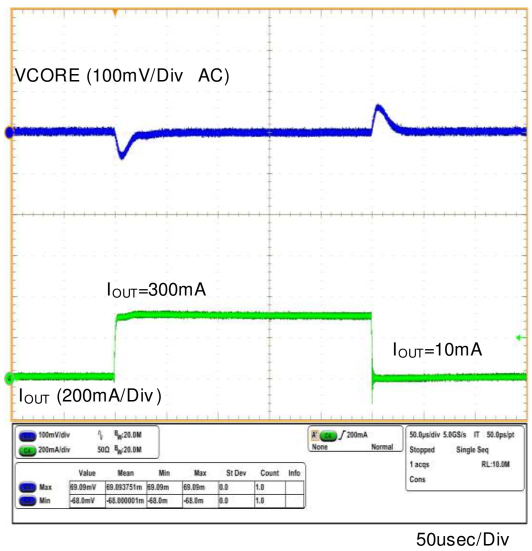


Figure 15. VCORE Load Transient

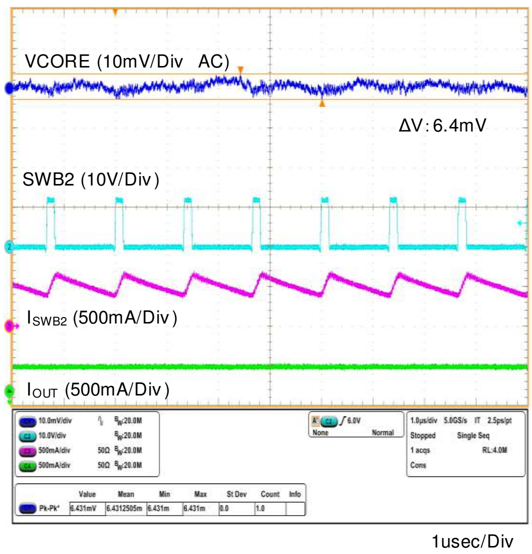


Figure 16. VCORE Switching
(Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

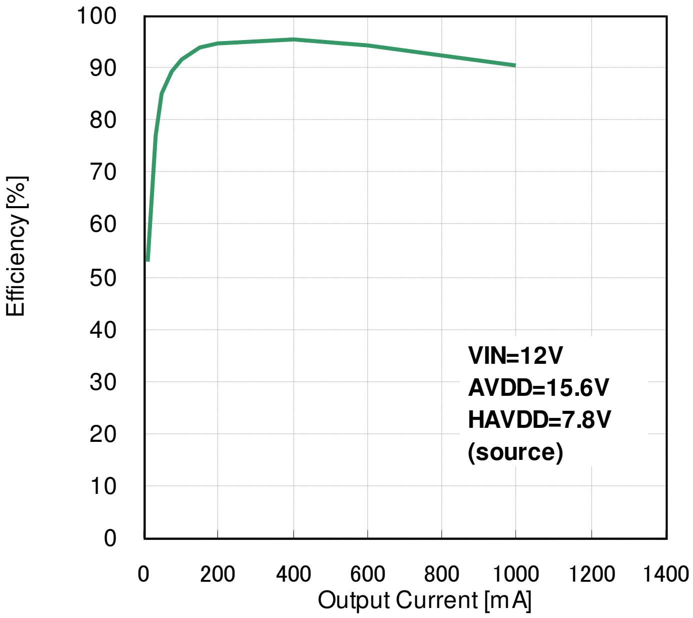


Figure 17. HAVDD Efficiency vs Output Current (source)

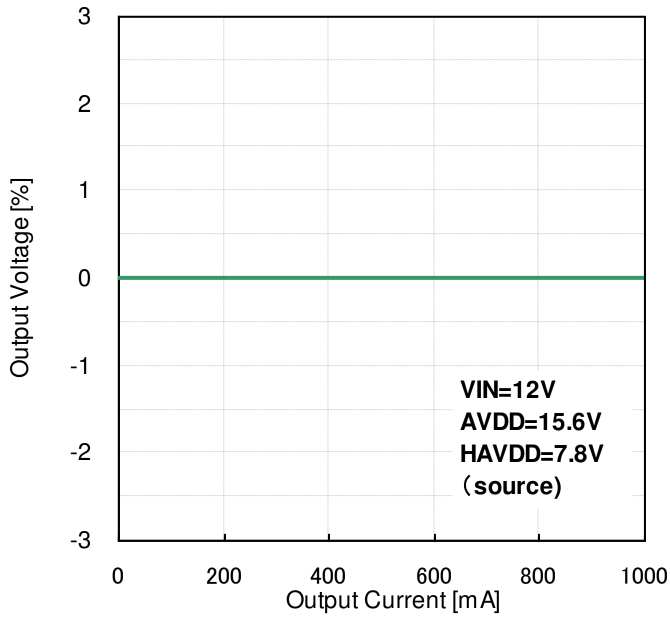


Figure 18. HAVDD Output Voltage vs Output Current (source)

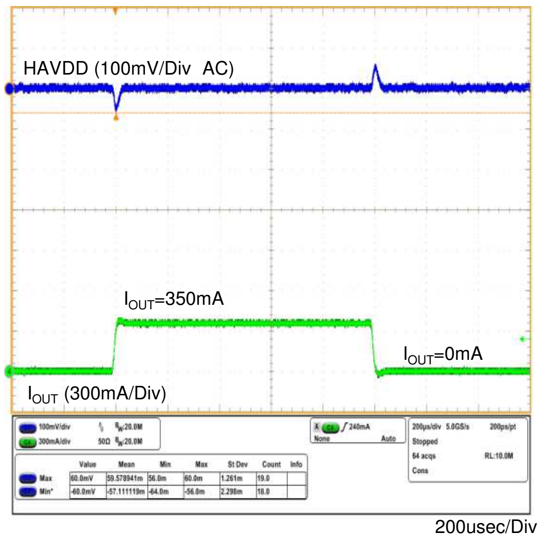


Figure 19. HAVDD Load Transient (source)

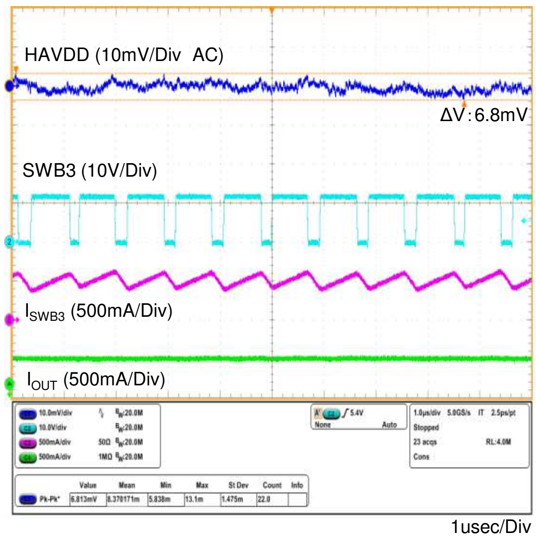


Figure 20. HAVDD Switching (source)
(Output Current=500mA)

Typical Performance Curves
(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

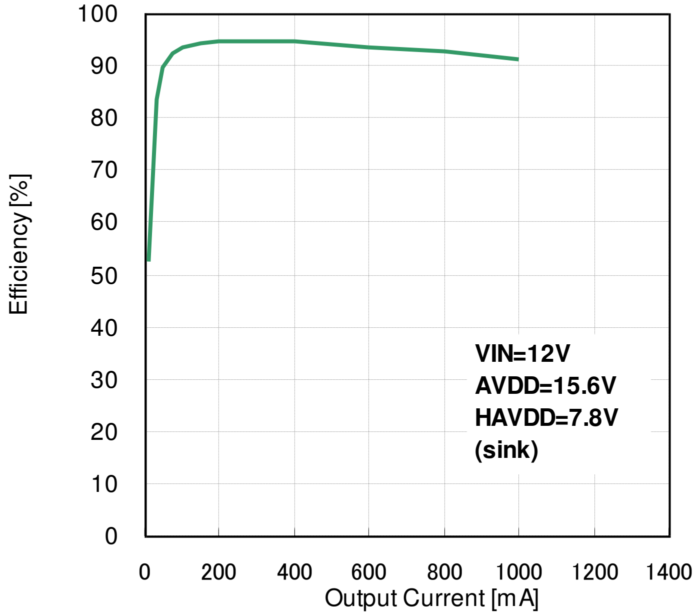


Figure 21. HAVDD Efficiency vs Output Current (sink)

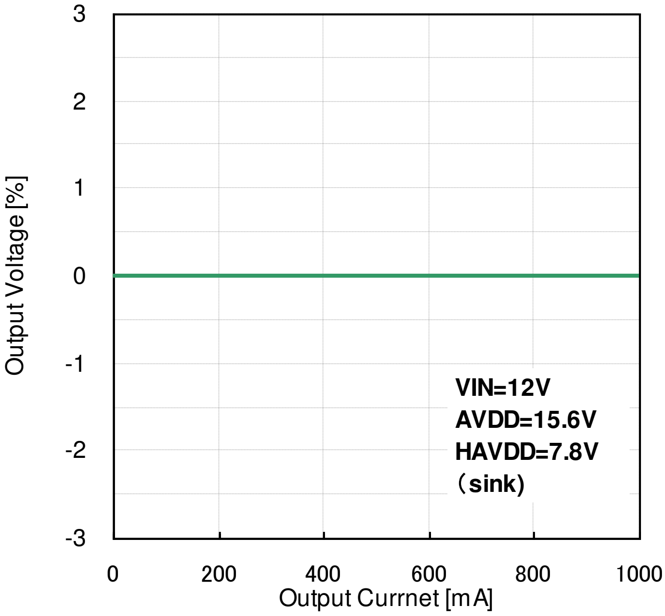


Figure 22. HAVDD Output Voltage vs Output Current (sink)

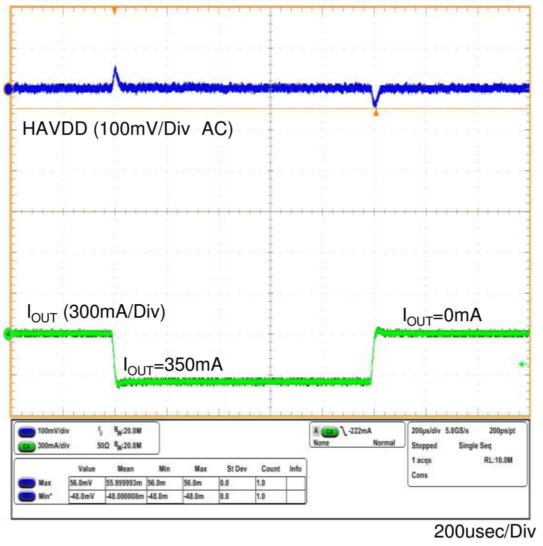


Figure 23. HAVDD Load Transient (sink)

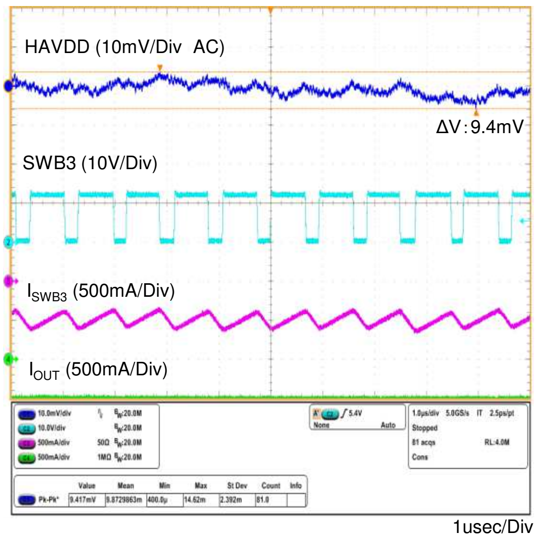


Figure 24. HAVDD Switching (sink)
(Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

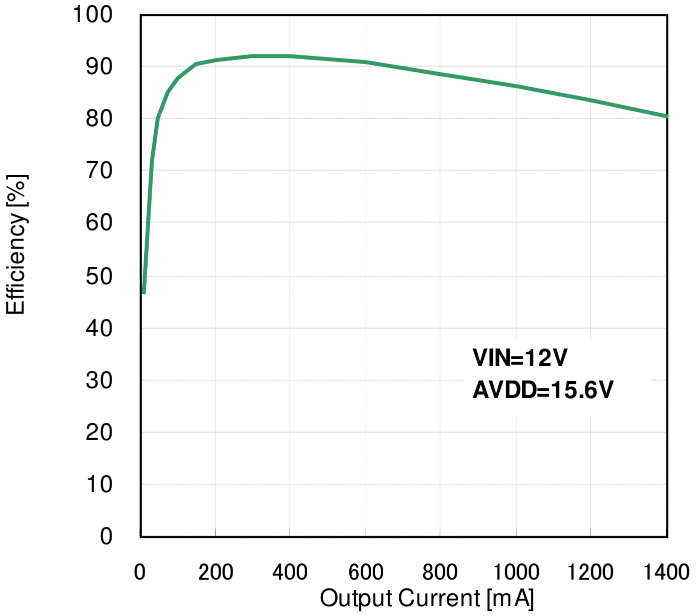


Figure 25. AVDD Efficiency vs Output Current

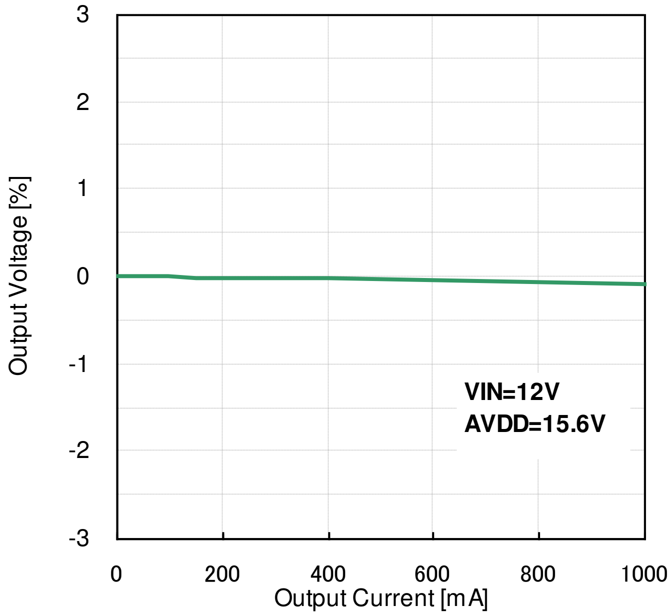


Figure 26. AVDD Output Voltage vs Output Current

Figure 27. AVDD Load Transient

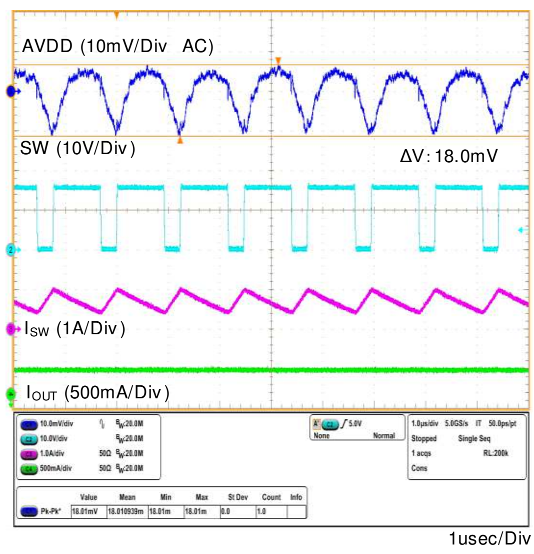


Figure 28. AVDD Switching
(Output Current=500mA)

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

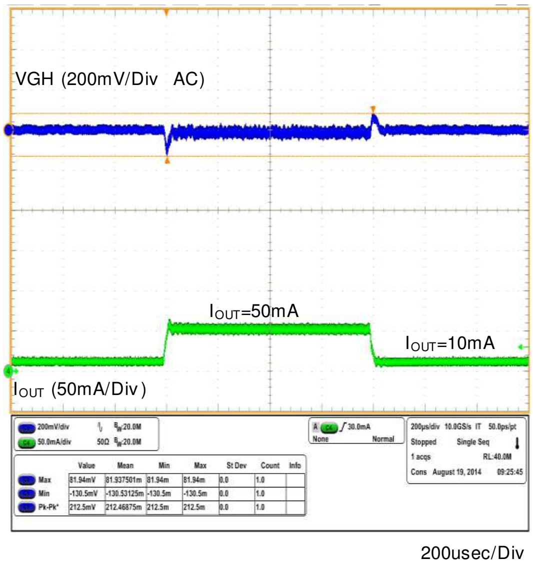


Figure 29. VGH Load Transient

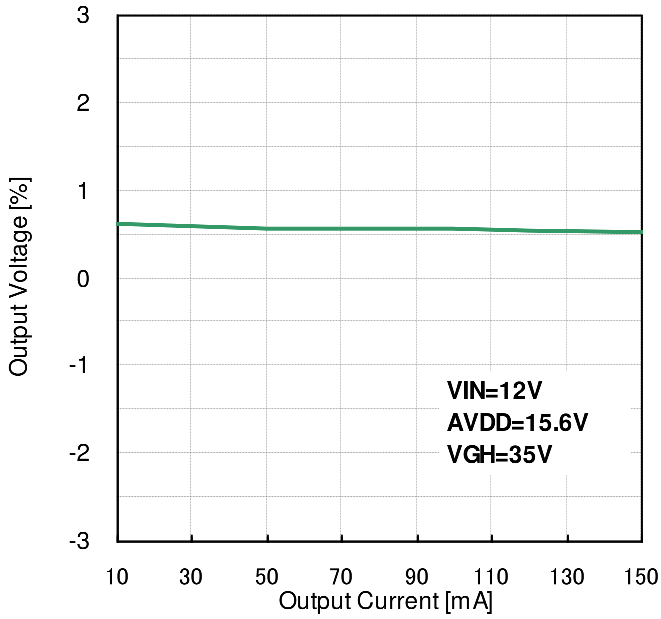


Figure 30. VGH Output Voltage vs Output Current

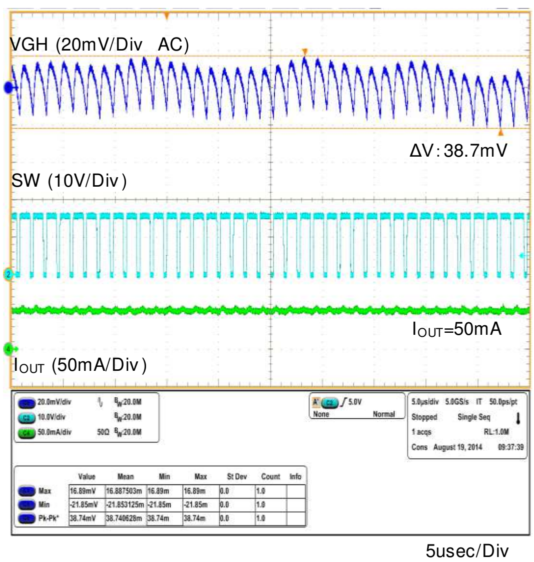


Figure 31. VGH Ripple Voltage

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

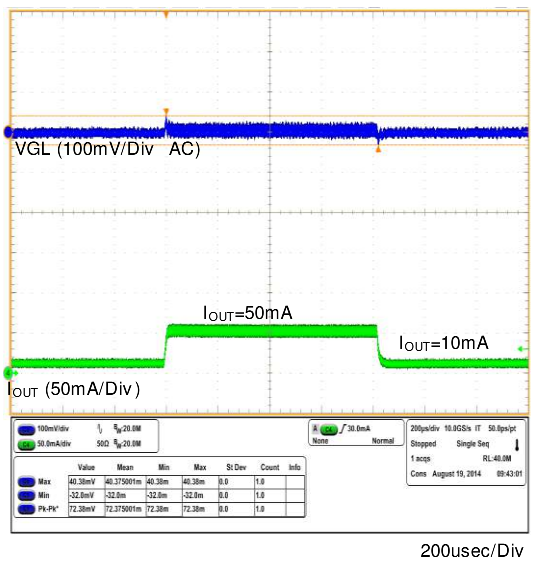


Figure 32. VGL Load Transient

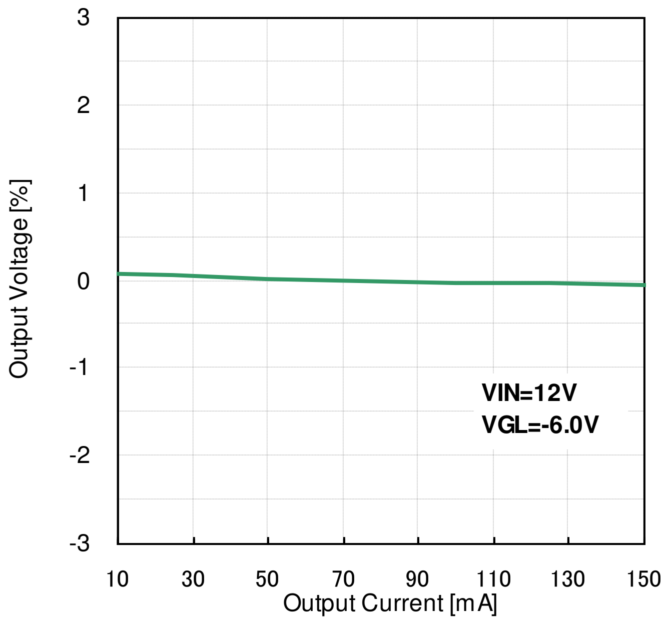


Figure 33. VGL Output Voltage vs Output Current

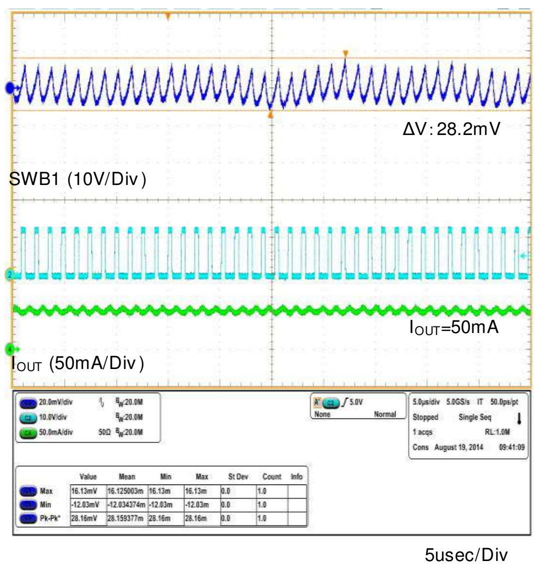


Figure 34. VGL Ripple Voltage

Typical Performance Curves

(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

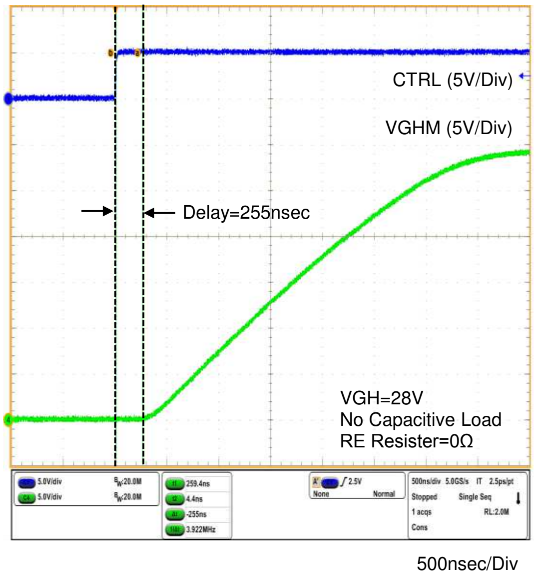


Figure 35. GPM Propagation Delay (rise)

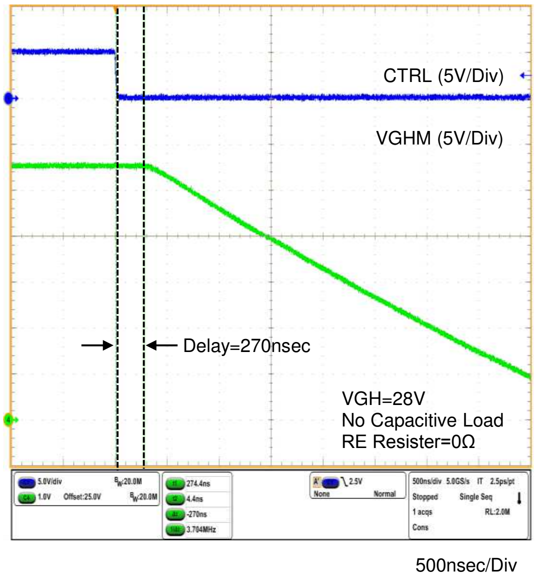


Figure 36. GPM Propagation Delay (fall)

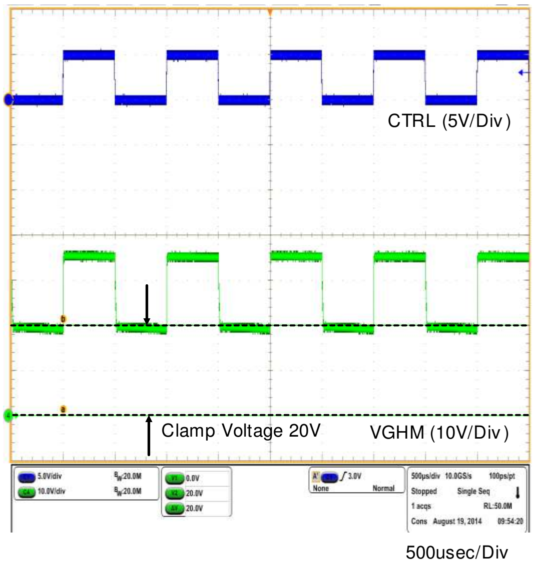


Figure 37. GPM Clamp Voltage (20V Clamp)

Typical Performance Curves
(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

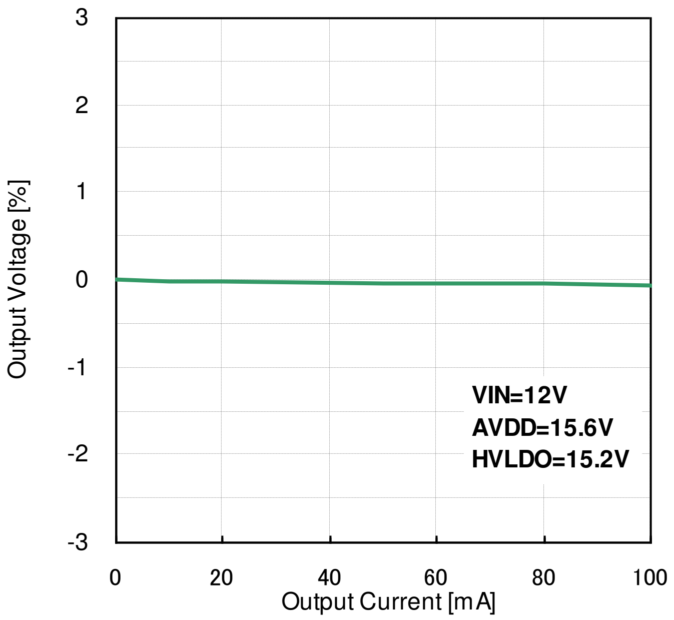


Figure 38. HVLDO Output Voltage vs Output Current

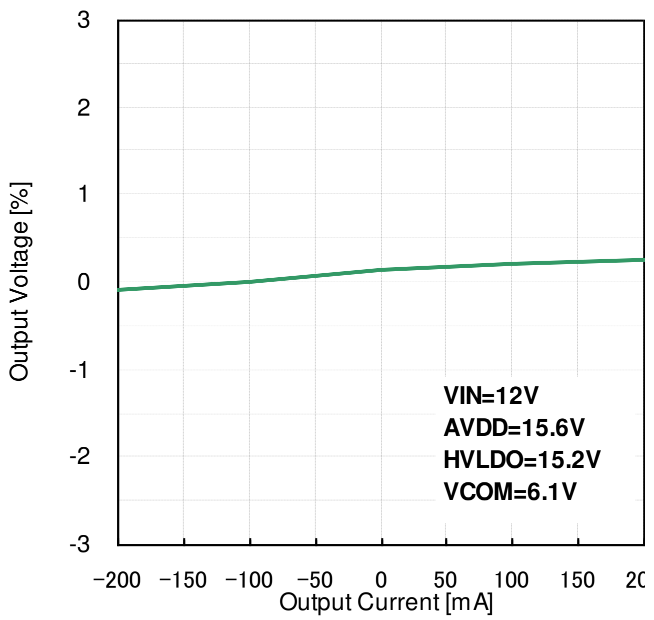


Figure 39. VCOM Output Voltage vs Output Current

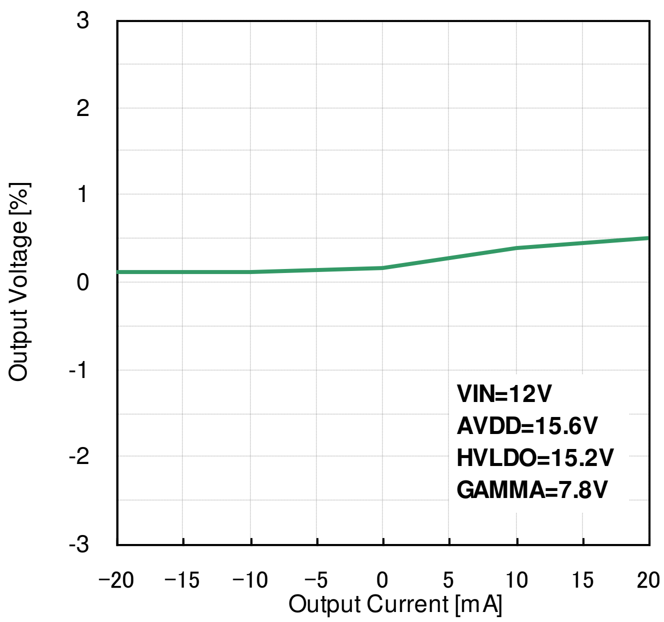


Figure 40. GAMMA Output Voltage vs Output Current

Typical Performance Curves
(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

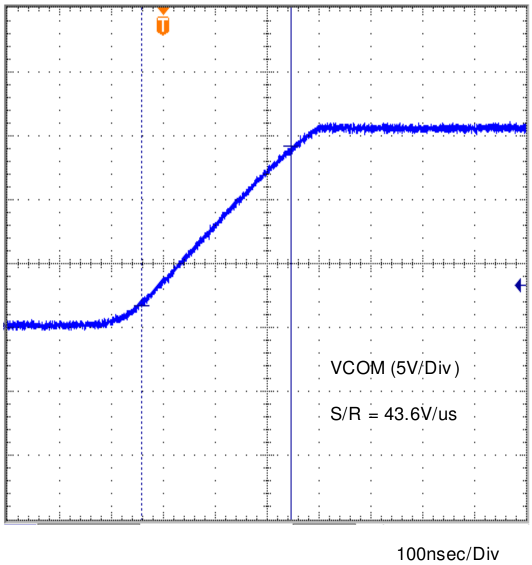


Figure 41. VCOM Slew Rate（Rise）

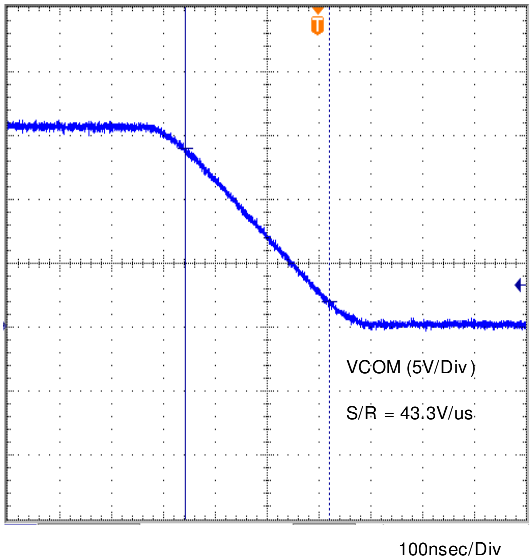


Figure 42. VCOM Slew Rate（Fall）

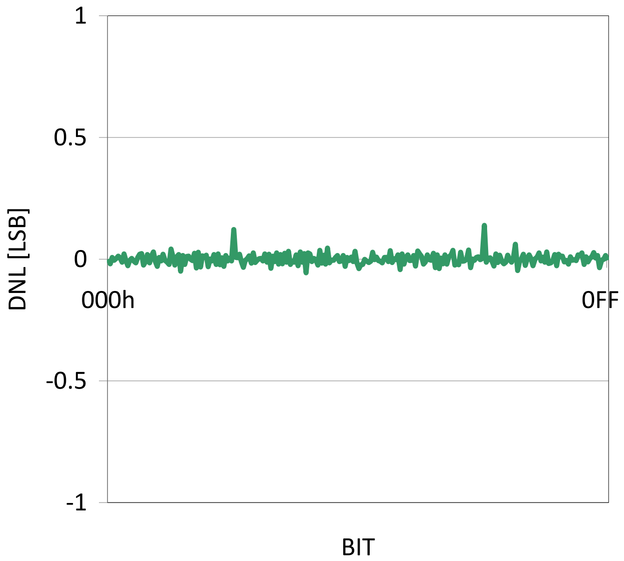


Figure 43. VCOM DNL vs BIT

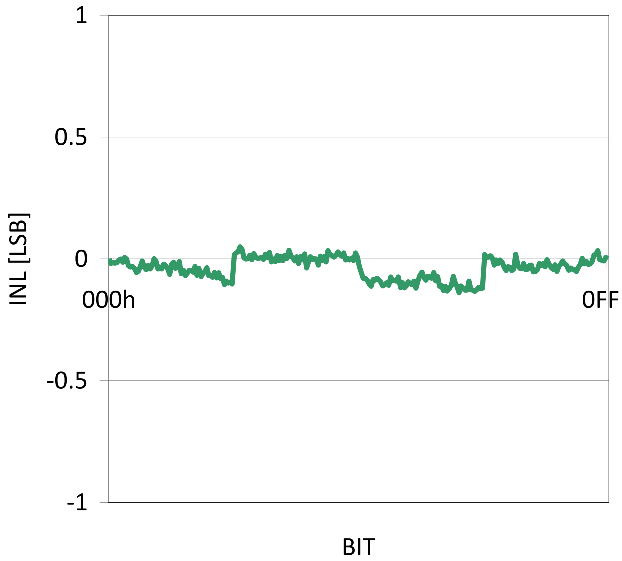


Figure 44. VCOM INL vs BIT

Typical Performance Curves
(Unless otherwise specified, Ta=25℃, AVIN,VINB1,VINB2,VINB3=12V, VIO=3.3V, VCORE=1.2V, AVDD=15.6V, HAVDD=7.8V, VGH=35V, VGL=-6.0V, HVLDO=15.2V, VCOM=6.1V, GAMMA=7.8V, RL=no load)

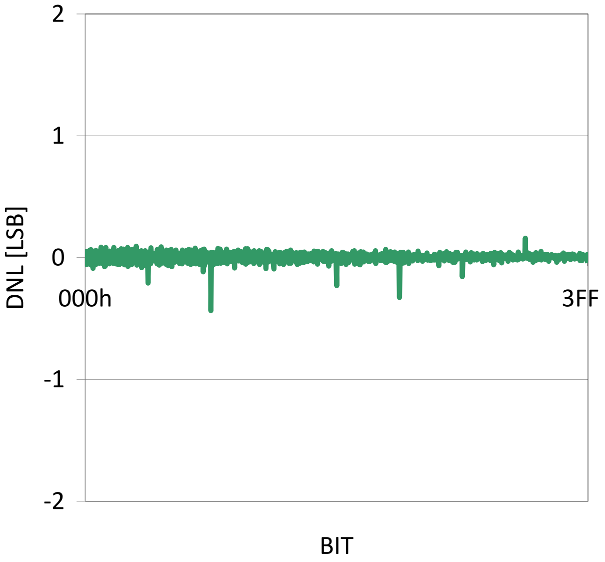


Figure 45. GAMMA DNL vs BIT

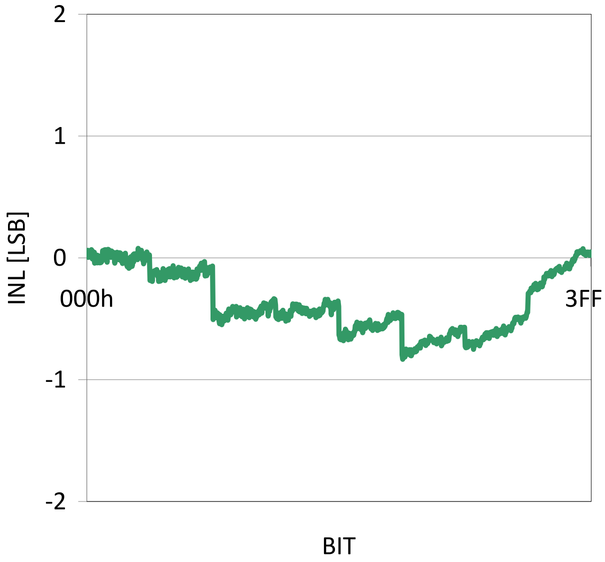


Figure 46. GAMMA INL vs BIT

Timing Chart

ON and OFF Sequence of this IC are shown below.

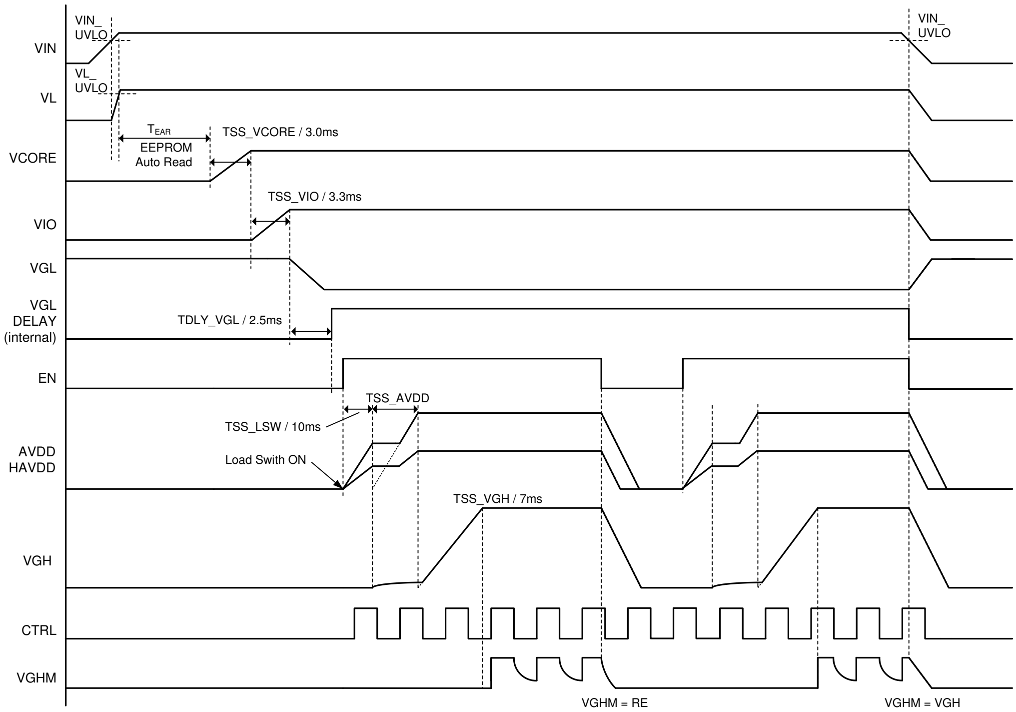


Figure 47. Timing Chart

VL activates with UVLO release of VIN.
It reads EEPROM data by Auto Read operation after VL finish its activation. (T_{EAR}=2msec)
After Auto Read completion, VCORE activates. The Soft Start time of VCORE is 3msec.
After VCORE soft-start completion, VIO activates. The Soft Start time of VIO is 3.3msec if the setting is 3.3V.
After VIO soft-start completion, PG becomes high and VGL activates. (If SWB1 is used)
The Soft Start time of VGL depends on output voltage setting, external capacitor etc.
2.5msec after VIO soft-start completion, Load SW turns ON (10msec) because of EN=High and AVDD activates.
The Soft Start time of AVDD can be changed by register setting. (10msec or 20msec)
After AVDD started, VGH activates. The Soft Start time of VGH is 7msec if the setting is 35V.
After VGH started, CTRL rising or falling will be a trigger to activate GPM operation.
When VGHM voltage at CTRL =L reaches the GPM clamp voltage, VGHM output is high impedance.
GPM, VGH, AVDD, HAVDD shuts down when EN=Low. GPM output (VGHM) will be the same potential with RE.
All output shuts down when UVLO of VIN is detected. VGHM will be the same potential with VGH.

HVLDO, HAVDD and VCOM starts up followed by AVDD output voltage. AMP 1 to 4 startup followed by HVLDO output voltage.

When EN=low, AVDD and HAVDD output become high impedance. HVLDO, VCOM and AMP1 to 4 output shut down followed by AVDD till AVDD is below a certain level.

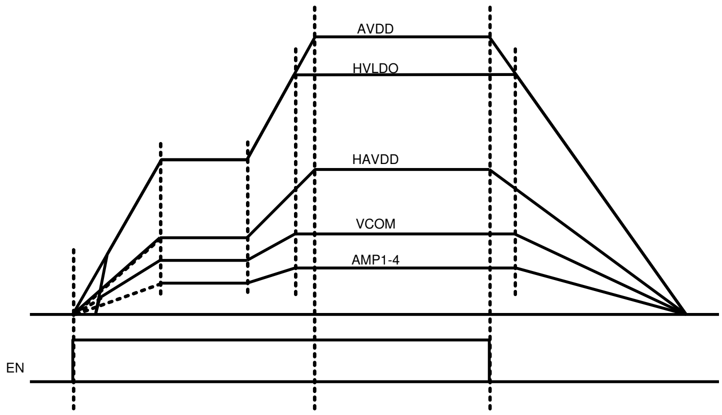


Figure 48. Timing Chart 2

Example Application
(TOP VIEW)

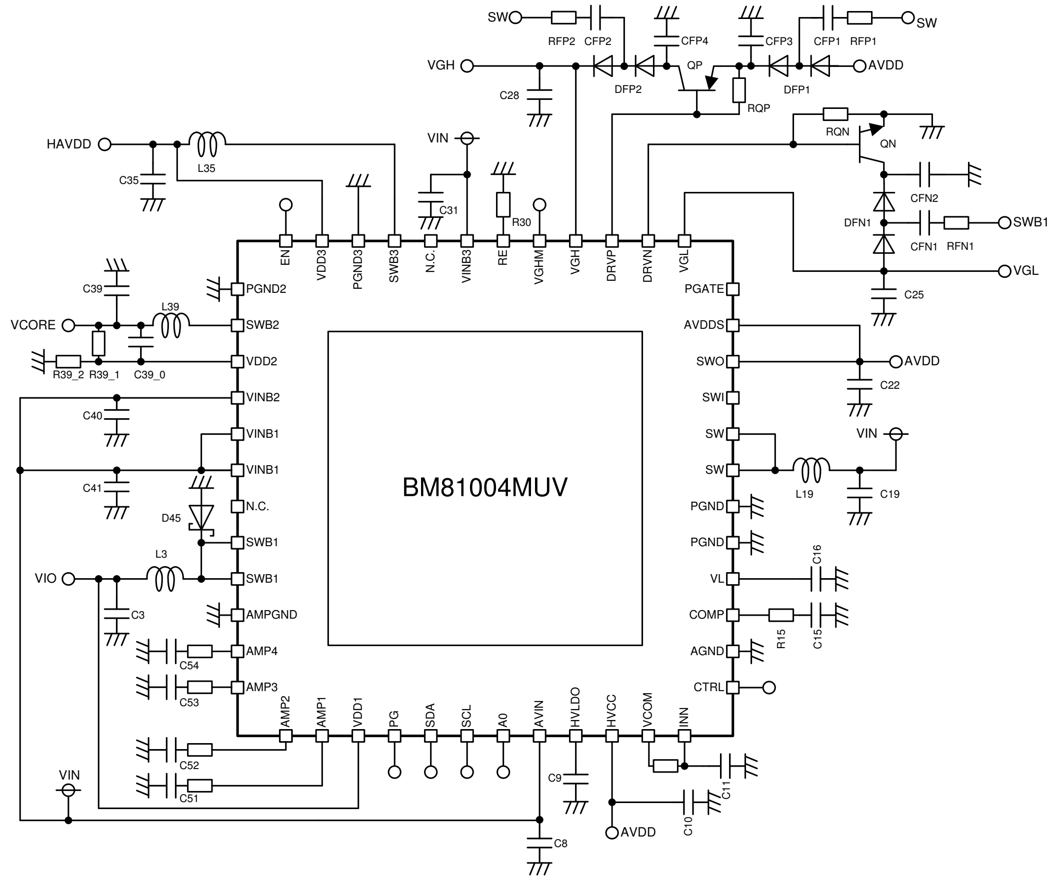


Figure 49. Example Application

Application circuit components list

Parts name	Value	Company	Parts Number	Parts name	Value	Company	Parts Number
C3	4x 10 [uF]	MURATA	GRM21BB31A106KE18	C40	10 [uF]	MURATA	GRM31CB31E106KA75
C8	1 [uF]	MURATA	GRM188B31E105KA75	C41	2x 10 [uF]	MURATA	GRM31CB31E106KA75
C9	10 [uF]	MURATA	GRM31CB31E106KA75	C51-54	0.1 [uF]	MURATA	GRM188B31H104KA92
C10	10 [uF]	MURATA	GRM31CB31E106KA75	R15	2.7 [kΩ]	ROHM	MCR03
C11	10 [uF]	MURATA	GRM31CB31E106KA75	R30	300 [Ω]	ROHM	MCR25
C15	6.8 [nF]	MURATA	GRM188B11E682KA01	R39_1	330 [Ω]	ROHM	MCR03
C16	1 [uF]	MURATA	GRM188CB31E105KA75	R39_2	120 [Ω]	ROHM	MCR03
C19	2x 10 [uF]	MURATA	GRM31CB31E106KA75	RFN1	2.2 [Ω]	ROHM	MCR25
C22	4x 10 [uF]	MURATA	GRM31CB31E106KA75	RFP1-2	2.2 [Ω]	ROHM	MCR25
C25	4.7 [uF]	MURATA	GRM219B31C475KE15	RQN	100 [kΩ]	ROHM	MCR03
CFN1	0.1 [uF]	MURATA	GRM188B31H104KA92	RQP	100 [kΩ]	ROHM	MCR03
CFN2	470 [pF]	MURATA	GRM188B11H471KA01	L19	6.8 [uH]	TAIYO YUDEN	NS10165T6R8N
CFP1	0.1 [uF]	MURATA	GRM188B31H104KA92	L3	6.8 [uH]	TAIYO YUDEN	NRS8040T6R8M
CPF2	0.1 [uF]	MURATA	GRM188B31H104KA92	L35	6.8 [uH]	TAIYO YUDEN	NRS8040T6R8M
CPF3	1 [uF]	MURATA	GRM21BB31H105KA12	L39	6.8 [uH]	TAIYO YUDEN	NRS8040T6R8M
CFP4	2.2 [nF]	MURATA	GRM188B11H222KA01	D45	-	ROHM	RSX301L-30
C28	10 [uF]	MURATA	GRM31CB31H106KA12	DFN1	-	ROHM	RB558W
C31	10 [uF]	MURATA	GRM31CB31E106KA75	DFP1	-	ROHM	RB558W
C35	2x 10 [uF]	MURATA	GRM31CB31E106KA75	DFP2	-	ROHM	RB558W
C39	4x 10 [uF]	MURATA	GRM21BB31A106KE18	QN	PNP	ROHM	2SCR513P
C39_0	22 [nF]	MURATA	GRM188B31H104KA92	QP	NPN	ROHM	2SAR513P

Protection function explanation of each block

1. BUCK CONVERTER BLOCK 1 (VIO)

1-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising VIO voltage.
Voltage inputted to VDD1 pin is monitored and if VIO voltage reaches VIO>110% (Typ), it is considered as unusual condition thus, OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to VIO voltage. After OVP is released, switching is re-started.

1-2. Over Current Protection (OCP)

If excessive load current (SWB1 peak current>3.5A, Typ) is present, it limits current to flow to built–in Power MOS by controlling Switching.

1-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When unusual condition (VIO<80%) is detected, SWB1 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues up to 10msec (Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

2. BUCK CONVERTER BLOCK 2 (VCORE)

2-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising VCORE voltage.
Voltage inputted to VDD2 pin is monitored and if VCORE voltage reaches VCORE>110%(Typ), it is considered as unusual condition thus, OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%,Typ) falls to VCORE voltage. After OVP is released, switching is re-started.

2-2. Over Current Protection (OCP)

If excessive load current (SWB2 peak current>3.0A, Typ) is present, it limits current to flow to built–in Power MOS by controlling Switching.

2-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When unusual condition (VCORE<80%) is detected, SWB2 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues upto 10msec (Typ), all output will be latched in shutdown state. Power reset is needed to remove the latch state and to re-start.

3. VGL REGULATOR BLOCK

3-1. Over Current Protection (OCP)

If excessive load current (I_DRVN>5mA, Min) is present, It controls source current (Base current of NPN Tr) of DRVN.

3-2. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When unusual condition is detected (VGL>80%), UVP time counter get started, and if the unusual condition continues up to 10msec (Typ), all output is latched in shutdown condition. Power reset is needed to cancel the latch state and to re-start.

4. BOOST CONVERTER BLOCK (AVDD)

4-1. Over Voltage Protection (OVP)

OVP function is built in to prevent IC or other components from malfunctioning due to excessive rise in AVDD voltage. The voltage inputted to SWO pin is being monitored. If the SWO pin voltage becomes 19.5V (Typ), OVP is detected. Once OVP is detected, switching is stopped. After AVDD voltage falls below OVP detection release voltage 18V (Typ), switching is restarted.

4-2. Over Current Protection (OCP)

If excessive load current over 5A (Typ) of SW peak current is present, OCP limits current to rush to built-in Power MOS by controlling its output switching.

4-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When an unusual condition is detected (AVDD<80%), UVP timer starts. If the unusual condition continues upto 10msec (Typ), all output is latched in shutdown condition. Power reset is needed to remove the latch state and to re-start.

4-4. Load Switch Over Current Protection (LSW_OCP)

If excessive load current (7A, Typ) is present, It controls current of load switch.

5. BUCK CONVERTER BLOCK 3 (HAVDD)

5-1. Over Voltage Protection (OVP)

OVP function is incorporated for preventing IC or other components from malfunctioning due to rising HAVDD voltage. Voltage inputted to VDD3 pin is being monitored and if HAVDD voltage reaches HAVDD>110% (Typ), it is considered as unusual condition thus, OVP function is operated. If OVP is detected, switching is stopped until OVP release voltage (100%, Typ) falls to HAVDD voltage. After OVP release, switching is re-started.

5-2. Over Current Protection (OCP)

If excessive load current is demanded (SWB3 peak current>1.5A, Typ), it limits current to flow to built–in Power MOS by controlling Switching.

5-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When the unusual condition (HAVDD<80%) is detected, SWB3 frequency is divided into 1/4 and UVP timer starts.
If the unusual condition continues up to 10msec(typ.), all output will be latched with shutdown state. Power reset is needed to remove the latch state and to re-start.

6. HIGH VOLTAGE LDO BLOCK

6-1. Over Current Protection (OCP)

If excessive load current (I_HVLDO>100mA, typ.) is present, It controls source current of HVLDO.

6-2. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built in.
When an unusual condition is detected (HVLDO<80%), UVP timer starts. If unusual condition continues up to 10msec (Typ), all output is latched in shutdown condition. Power reset is needed to remove the latch state and to re-start.

7. VGH REGULATOR BLOCK

7-1. Over Voltage Protection (OVP)

OVP function is incorporated to prevent IC or other components from malfunctioning due to rising VGH voltage.
Voltage inputted to VGH pin is being monitored and if VGH voltage reaches VGH>38V (Typ), it is considered as unusual condition so that OVP function is operated. If OVP is detected, limit DRVP current until OVP release voltage (35V, Typ) falls to VGH voltage. After OVP release, switching is re-started.

7-2. Over Current Protection (OCP)

If excessive load current (I_DRVP>5mA, Min) is present, It controls sink current (Base current of PNP Tr) of DRVP.

7-3. Under Voltage Protection (UVP)

Timer-latch type output UVP function is built-in.
When an unusual condition is detected (VGH<80%), UVP timer starts. If the unusual condition continues up to 10msec (Typ), all output is latched in shutdown condition. Power reset is needed to remove the latch state and to re-start.

8. GENERAL

8-1. Thermal shutdown

All outputs will shut down when the IC temperature exceeds 175℃ (Typ). After the temperature falls below 150℃ (Typ), the operation re-starts.

8-2. VIN Under Voltage Lock Out

VIN Under Voltage Lock Out prevents the circuit malfunction below the UVLO voltage. If VIN voltage is below the UVLO voltage (8.3V / 7.55V), it enters the standby state.

Protection function list

BLOCK	Protective Function	Working Condition	Action	Protective removal
BUCK CONVERTER 1	OVP	VIO>110%	Stops switching.	VIO<100%
	OCP	I_SWB1>3.5A	Control switching pulse duty to not over current limit.	I_SWB1<3.5A
	UVP	VIO<80%	Frequency becomes 1/4	VIO>80%
			IC shutdown if UVP status maintains during 10msec.	IC restart
BUCK CONVERTER 2	OVP	VCORE>110%	Stops switching.	VCORE<100%
	OCP	I_SWB2>3.0A	Control switching pulse duty to not over current limit.	I_SWB2<3.0A
	UVP	VCORE<80%	Frequency becomes 1/4	VCORE>80%
			IC shutdown if UVP status maintains during 10msec.	IC restart
VGL REGULATOR	OCP	I_DRVN>5mA	Limit DRVN current.	I_DRVN<5mA
	UVP	VGL<80%	IC shutdown if UVP status maintains during 10msec.	IC restart
BOOST CONVERTER	OVP	AVDD>19.5V	Stops switching	AVDD<18V
	OCP	I_SW>5A	Control switching pulse duty to not over current limit.	I_SW<5A
	UVP	AVDD<80%	IC shutdown if UVP status maintains during 10msec.	IC restart
LOAD SW	OCP	I_SWO>7.0A	Control switching pulse duty to not over current limit.	IC restart
BUCK CONVERTER 3	OVP	HAVDD>110%	Stops switching.	HAVDD<100%
	OCP	I_SWB3>1.5A	Control switching pulse duty to not over current limit.	I_SWB3<1.5A
	UVP	HAVDD<80%	Frequency becomes 1/4	HAVDD>80%
			IC shutdown if UVP status maintains during 10msec.	IC restart
HIGH VOLTAGE LDO	OCP	I_HVLDO>100mA	Limit HVLDO current.	I_HVLDO<100mA
	UVP	HVLDO<80%	IC shutdown if UVP status maintains during 10msec.	IC restart
VGH REGULATOR	OVP	VGH>45V	DRVP current limit to 0mA	VGH<42V
	OCP	I_DRVP>5 mA	Limit DRVP current.	I_DRVP<5mA
	UVP	VGH<80%	IC shutdown if UVP status maintains during 10msec.	IC restart
GENERAL	TSD	Tj>175℃	IC shutdown	Tj<150℃
	UVLO	VIN<7.55V	IC shutdown	VIN>8.3V

Serial transmission

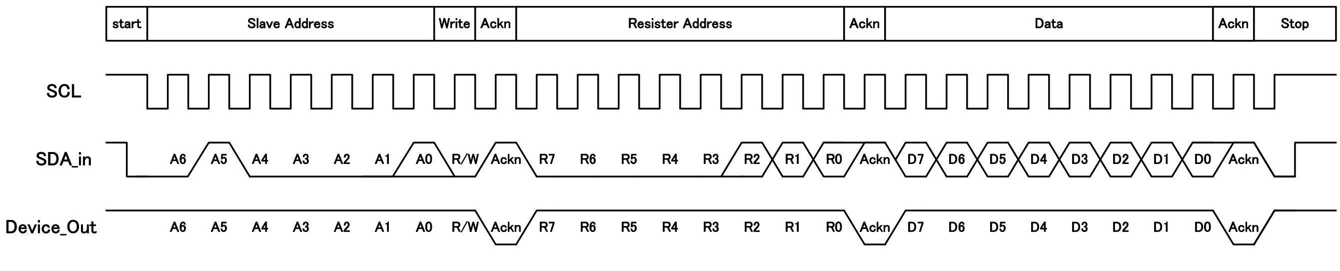
Use I^{2}C BUS control for command interface with Host.
Writing or reading by specifying 1 byte Register address besides Slave address.
I^{2}C BUS slave mode format is shown below.

Write operation	Start	Slave Address							R/W	A	Register Address	A	DATA	A	Stop
		0	1	0	0	0	0	A0	0	0	Select Register Address (8bit)	0	8bit DATA	0	
Read operation	Start	Slave Address							R/W	A	Register Address	A	DATA	A	Stop
		0	1	0	0	0	0	A0	1	0	Select Register Address (8bit)	0	8bit DATA	0	

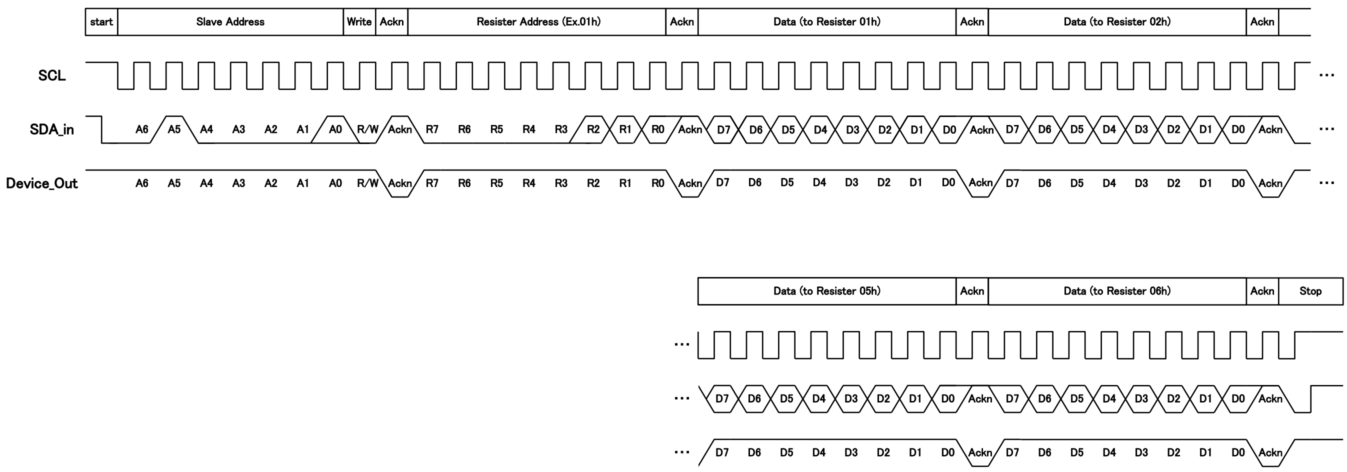
Start	:	Start condition
Slave Address	:	Send 7 bit data in all with bit of Read Mode (H) or Write Mode (L). (MSB First) A0 are selectable (1/0) with the slave address select pin.
ACK	:	Acknowledge Sending or receiving data includes acknowledge bit per byte. If the data is sent and received properly, 'L' is sent and received. If 'H' is sent and received, it means there is no Acknowledge.
Register Address	:	Use 1 byte select address.
Data	:	Data byte. Sending and Receiving data (MSB First)
STOP	:	Stop condition

For writing mode from I2C BUS to register, there are Single mode and Multi-mode.
On single mode, write data to one designated register.
On multi-mode, as a start address register specified in the second byte, writing data can be performed continuously, by entering multiple data.
Single mode or multi-mode setting can be configured by having or not having 'stop bit'.

①Single Mode Timing Chart



②Multi-Mode Timing Chart



I2CTiming Diagram

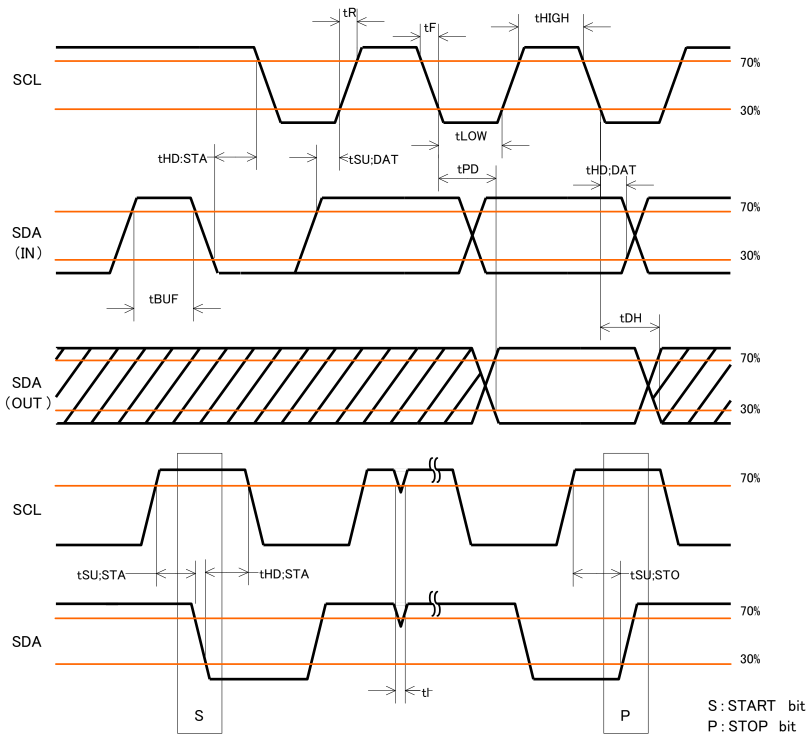


Figure 50. I2C Timing Diagram

・Timing standard values

Parameter	Symbol	NORMA LMODE			FAST MODE			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCL frequency	f SCL	-	-	100	-	-	400	kHz
SCL high time	tHIGH	4.0	-	-	0.6	-	-	us
SCL low time	tLOW	4.7	-	-	1.2	-	-	us
Rise Time	tR	-	-	1.0	-	-	0.3	us
Fall Time	tF	-	-	0.3	-	-	0.3	us
Start condition hold time	tHD ; STA	4.0	-	-	0.6	-	-	us
Start condition setup time	tSU ; STA	4.7	-	-	0.6	-	-	us
SDA hold time	tHD ; DAT	200	-	-	100	-	-	ns
SDA setup time	tSU ; DAT	200	-	-	100	-	-	ns
Acknowledge delay time	tPD	-	-	0.9	-	-	0.9	us
Acknowledge hold time	tDH	-	0.1	-	-	0.1	-	us
Stop condition setup time	tSU ; STO	4.7	-	-	0.6	-	-	us
Bus release time	tBUF	4.7	-	-	1.2	-	-	us
Noise spike width	TI	-	0.1	-	-	0.1	-	us

Command Interface

EEPROM transmission format for data sent and received is shown below.

I2C Write format

Start	Slave Address							R/W	A	Register Address	A	DATA	A	Stop
	0	1	0	0	0	0	A0	0	0	00h to 0Ch	0	N-bytes DATA	0	

It can enter further Register from 3 byte by entering data continuously.
DATA after 0Dh is invalid.
Inputted Data reflect to the Register at the ACK output timing.

I2C Read format

1. Read data from DAC Register

Start	Slave Address							R/W	A	Register Address / DATA	A	
	0	1	0	0	0	0	A0	0	0	00h to 0Ch	0	
Repeated Start	Slave Address							R/W	A	DATA	A	Stop
	0	1	0	0	0	0	A0	1	0	N-bytes DATA	0	

EEPROM Write Format

EEPROM (DAC Register) transmission format for write is shown below.

EEPROM Write format

Start	Slave Address							R/W	A	Register Address								A	DATA								A	Stop
	0	1	0	0	0	0	A0	0	0	1	1	1	1	1	1	1	1	0	1	X	X	X	X	X	X	X	0	

D6 to D0 : Don’t care

Automatic EEPROM Read Function at Start-up

Upon BM81110MUW start-up, a reset signal is generated and each register is initialized.
After VL activation is finished, data which is stored in the EEPROM is copied to the registers.
The automatic EEPROM read function at start-up is further explained by the flow chart below.

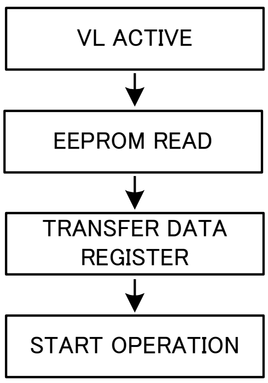


Figure 51. Automatic EEPROM Read Function at Start-up

Content of EEPROM setting

Register Address	Bits	Function	Default(*1)	Resolution
00h	6	Channel Disable Register	00h	-
01h	6	AVDD output voltage setting[5:0]	15.6V [27h]	0.1V [11.7V to 18.0V]
02h	3	AVDD OCP offset setting[2:0]	1.6A [04h]	0.4A [0A to 2.8A]
03h	1	AVDD soft start time setting[0]	10msec [00h]	10msec [10msec or 20msec]
04h	4	VIO output voltage setting[3:0]	3.3V [0Bh]	0.1V [2.2V to 3.7V]
05h	6	HAVDD output voltage setting[5:0]	7.8V [1Eh]	0.1V [4.8V to 11.1V]
06h	5	VGH output voltage setting[4:0]	35V [14h]	0.5V [25V to 40.5V]
07h	2	GPM clamp voltage setting[1:0]	20V [01h]	5V [15V to 30V]
08h	5	VGL output voltage setting[4:0]	-6.0V [0Ah]	0.2V [-10.2V to -4.0V]
09h	6	HVLDO output voltage setting[5:0]	15.2V [23h]	0.1V [11.7V to 18.0V]
0Ah	8	VCOM output voltage setting[7:0]	6.103V[C5h]	HVLDOx0.18/256 [HVLDOx0.36 to HVLDOx0.54]
0Bh[7:6], 0Ch	10	AMP1 output voltage setting[9:0]	7.808V[1F2h]	HVLDO/1024[0V to HVLDO]
0Bh[5:4], 0Dh	10	AMP2 output voltage setting[9:0]	7.808V[1F2h]	HVLDO/1024[0V to HVLDO]
0Bh[3:2], 0Eh	10	AMP3 output voltage setting[9:0]	7.808V[1F2h]	HVLDO/1024[0V to HVLDO]
0Bh[1:0], 0Fh	10	AMP4 output voltage setting[9:0]	7.808V[1F2h]	HVLDO/1024[0V to HVLDO]
FFh	8	Control Register[7:0]		

*1 Factory value.
*2 Value of default voltage setting. The Soft start time of each output changes depending on a setting voltage.

Channel Disable Register

Register Address = 00h							
[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
-	-	VCORE	HAVDD	VGH	VGL	GPM	AVDD_EXT

0 : Enable 1 : Disable
AVDD_EXT 1 : AVDD external mode

Control Register

Register Address	DATA [BIN]	Function
FFh	1xxx_xxxx	Write to EEPROM from DAC Register data.

x : Don't care bit

Register Map

Resister Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
00h	—	—	VCORE	HAVDD	VGH	VGL	GPM	AVDD_EXT	00h
01h	—	—	AVDD[5:0]						27h
02h	—	—	—	—	—	AVDD OCP offset[2:0]			04h
03h	—	—	—	—	—	—	—	AVDD SS	00h
04h	—	—	—	—	VIO [3:0]				0Bh
05h	—	—	HAVDD [5:0]						1Eh
06h	—	—	—	VGH [4:0]					14h
07h	—	—	—	—	—	—	GPM clamp [1:0]		01h
08h	—	—	—	VGL [4:0]					0Ah
09h	—	—	HVLDO[5:0]						23h
0Ah	VCOM [7:0]								C5h
0Bh	AMP1[9:8]		AMP2[9:8]		AMP3[9:8]		AMP4[9:8]		55h
0Ch	AMP1[7:0]								F2h
0Dh	AMP2[7:0]								F2h
0Eh	AMP3[7:0]								F2h
0Fh	AMP4[7:0]								F2h
FFh	（ Control Register ）								—

Command Table 1

	Register Address								
	01	02	03	04	05	06	07	08	09
	[5:0]	[2:0]	[0]	[3:0]	[5:0]	[4:0]	[1:0]	[4:0]	[5:0]
DATA (HEX)	AVDD [V]	AVDD OCP offset [A]	AVDD soft start [msec]	VIO [V]	HAVDD [V]	VGH [V]	GPM clamp [V]	VGL [V]	HVLDO [V]
00	11.7	0.0	10	2.2	4.8	25.0	15	-4.0	11.7
01	11.8	0.4	20	2.3	4.9	25.5	20	-4.2	11.8
02	11.9	0.8		2.4	5.0	26.0	25	-4.4	11.9
03	12.0	1.2		2.5	5.1	26.5	30	-4.6	12.0
04	12.1	1.6		2.6	5.2	27.0		-4.8	12.1
05	12.2	2.0		2.7	5.3	27.5		-5.0	12.2
06	12.3	2.4		2.8	5.4	28.0		-5.2	12.3
07	12.4	2.8		2.9	5.5	28.5		-5.4	12.4
08	12.5			3.0	5.6	29.0		-5.6	12.5
09	12.6			3.1	5.7	29.5		-5.8	12.6
0A	12.7			3.2	5.8	30.0		-6.0	12.7
0B	12.8			3.3	5.9	30.5		-6.2	12.8
0C	12.9			3.4	6.0	31.0		-6.4	12.9
0D	13.0			3.5	6.1	31.5		-6.6	13.0
0E	13.1			3.6	6.2	32.0		-6.8	13.1
0F	13.2			3.7	6.3	32.5		-7.0	13.2
10	13.3				6.4	33.0		-7.2	13.3
11	13.4				6.5	33.5		-7.4	13.4
12	13.5				6.6	34.0		-7.6	13.5
13	13.6				6.7	34.5		-7.8	13.6
14	13.7				6.8	35.0		-8.0	13.7
15	13.8				6.9	35.5		-8.2	13.8
16	13.9				7.0	36.0		-8.4	13.9
17	14.0				7.1	36.5		-8.6	14.0
18	14.1				7.2	37.0		-8.8	14.1
19	14.2				7.3	37.5		-9.0	14.2
1A	14.3				7.4	38.0		-9.2	14.3
1B	14.4				7.5	38.5		-9.4	14.4
1C	14.5				7.6	39.0		-9.6	14.5
1D	14.6				7.7	39.5		-9.8	14.6
1E	14.7				7.8	40.0		-10.0	14.7
1F	14.8				7.9	40.5		-10.2	14.8
20	14.9				8.0				14.9
21	15.0				8.1				15.0
22	15.1				8.2				15.1
23	15.2				8.3				15.2
24	15.3				8.4				15.3
25	15.4				8.5				15.4
26	15.5				8.6				15.5
27	15.6				8.7				15.6
28	15.7				8.8				15.7
29	15.8				8.9				15.8
2A	15.9				9.0				15.9
2B	16.0				9.1				16.0
2C	16.1				9.2				16.1
2D	16.2				9.3				16.2
2E	16.3				9.4				16.3
2F	16.4				9.5				16.4
30	16.5				9.6				16.5
31	16.6				9.7				16.6
32	16.7				9.8				16.7
33	16.8				9.9				16.8
34	16.9				10.0				16.9
35	17.0				10.1				17.0
36	17.1				10.2				17.1
37	17.2				10.3				17.2
38	17.3				10.4				17.3
39	17.4				10.5				17.4
3A	17.5				10.6				17.5
3B	17.6				10.7				17.6
3C	17.7				10.8				17.7
3D	17.8				10.9				17.8
3E	17.9				11.0				17.9
3F	18.0				11.1				18.0

: Default Value

Command Table 2

	Register Address
	0A
	[7:0]
DATA (HEX)	VCOM [V]
00	HVLDOx0.18x(3 - 0/256)
01	HVLDOx0.18x(3 - 1/256)
02	HVLDOx0.18x(3 - 2/256)
⋮	⋮
FD	HVLDOx0.18x(3 - 253/256)
FE	HVLDOx0.18x(3 - 254/256)
FF	HVLDOx0.18x(3 - 255/256)

	Register Address			
	0B[7:6], 0C	0B[5:4], 0D	0B[3:2], 0E	0B[1:0], 0F
	[9:0]	[9:0]	[9:0]	[9:0]
DATA (HEX)	AMP1 [V]	AMP2 [V]	AMP3 [V]	AMP4 [V]
000	HVLDOx(1 - 0/1024)	HVLDOx(1 - 0/1024)	HVLDOx(1 - 0/1024)	HVLDOx(1 - 0/1024)
001	HVLDOx(1 - 1/1024)	HVLDOx(1 - 1/1024)	HVLDOx(1 - 1/1024)	HVLDOx(1 - 1/1024)
002	HVLDOx(1 - 2/1024)	HVLDOx(1 - 2/1024)	HVLDOx(1 - 2/1024)	HVLDOx(1 - 2/1024)
⋮	⋮	⋮	⋮	⋮
3FD	HVLDOx(1 - 1021/1024)	HVLDOx(1 - 1021/1024)	HVLDOx(1 - 1021/1024)	HVLDOx(1 - 1021/1024)
3FE	HVLDOx(1 - 1022/1024)	HVLDOx(1 - 1022/1024)	HVLDOx(1 - 1022/1024)	HVLDOx(1 - 1022/1024)
3FF	HVLDOx(1 - 1023/1024)	HVLDOx(1 - 1023/1024)	HVLDOx(1 - 1023/1024)	HVLDOx(1 - 1023/1024)

・In case of HVLDO=15.2[V]

	Register Address
	0A
	[7:0]
DATA (HEX)	VCOM [V]
00	8.208
01	8.197
02	8.187
⋮	⋮
C5	6.103
⋮	⋮
FD	5.504
FE	5.493
FF	5.483
step幅	0.011

	Register Address			
	0B[7:6], 0C	0B[5:4], 0D	0B[3:2], 0E	0B[1:0], 0F
	[9:0]	[9:0]	[9:0]	[9:0]
DATA (HEX)	AMP1 [V]	AMP2 [V]	AMP3 [V]	AMP4 [V]
000	15.200	15.200	15.200	15.200
001	15.185	15.185	15.185	15.185
002	15.170	15.170	15.170	15.170
⋮	⋮	⋮	⋮	⋮
1F2	7.808	7.808	7.808	7.808
⋮	⋮	⋮	⋮	⋮
3FD	0.045	0.045	0.045	0.045
3FE	0.030	0.030	0.030	0.030
3FF	0.015	0.015	0.015	0.015
step幅	0.015	0.015	0.015	0.015

Selecting Application Components

1. Buck Converter

1-1. Selecting the Output LC Constant

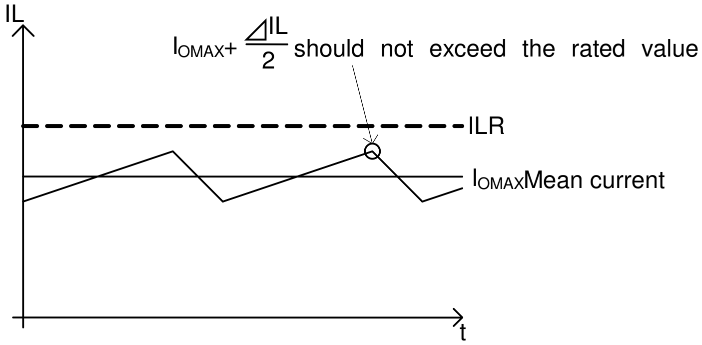


Figure 52. Inductor Current Waveform (Buck Converter).

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{OMAX}) of the inductance.
Adjust so that $I_{OMAX} + \Delta I_L / 2$ does not exceed the rated current value.

ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} \times (VIN - VO) \times \frac{VO}{VIN} \times \frac{1}{f} \text{ [A]}$$

where f is the switching frequency

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the coil current exceeds the rated current (I_{LR}), the IC may be damaged.

1-2. Selecting the Input/Output capacitor

The output capacitor (C_O) smoothens the ripple voltage at the output. Select a capacitor that will regulate the output ripple voltage within the specifications.

Output ripple voltage can be obtained by the following equation.

$$\Delta VPP = \Delta I_L \times R_{ESR} + \frac{\Delta I_L}{2\,Co} \times \frac{VO}{VIN} \times \frac{1}{f}$$

However, since the aforementioned conditions are based on a lot of factors, verify the results using the actual product.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the Input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10µF and less than 100mΩ ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus, it may cause the malfunction of the IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform margin check using the actual product.

1-3. Selecting the Output rectifier diode

A schottky barrier is recommended as rectifier diode to be used at the output stage of the DC/DC converter. Select carefully in consideration of the maximum inductor current, maximum output voltage and power supply voltage.

Maximum inductor current	$I_{OMAX} + \frac{\Delta I_L}{2}$	<	Diode Maximum Absolute Current
Maximum input voltage	V_{IN}	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30% to 40 for each parameter.

2. Boost Converter

2-1. Selecting the Output LC Constant

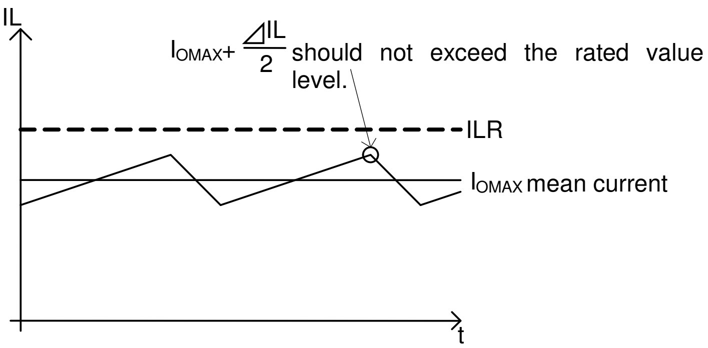


Figure 53. Inductor Current Waveform (Boost Converter).

The output inductance (L) is decided by the rated current (I_{LR}) and maximum input current (I_{INMAX}) of the inductance.
Adjust so that $I_{INMAX} + \Delta I_L / 2$ does not exceed the rated current value.

ΔI_L can be obtained by the following equation.

$$\Delta I_L = \frac{1}{L} VIN \times \frac{VO - VIN}{VO} \times \frac{1}{f} \text{ [A]}$$

where f is the switching frequency

Set with sufficient margin because the inductance value may have a dispersion of ±30%.
If the coil current exceeds the rated current (I_{LR}), the IC may be damaged.

2-2. Selecting the Output capacitor

The output capacitor (C_O) smoothens the ripple voltage at the output. Select a capacitor that will regulate the output ripple voltage within the specifications.

Output ripple voltage can be obtained by the following equation.

$$\Delta V_{PP} = I_{LMAX} \times R_{ESR} + \frac{1}{f \times CO} \times \frac{VIN}{VO} \times \left(I_{LMAX} - \frac{\Delta I_L}{2} \right)$$

However, since the aforementioned conditions are based on a lot of factors, verify the results using the actual product.

Since the peak current flows between the input and output at the DC/DC converter, a capacitor is required to install at the Input side. For the reason, the low ESR capacitor is recommended as an input capacitor which has the value more than 10µF and less than 100mΩ ESR. If an out of range capacitor is selected, the excessive ripple voltage is superimposed on the input voltage, thus, it may cause the malfunction of the IC.

However these conditions may vary according to the load current, input voltage, output voltage, inductance and switching frequency. Be sure to perform the margin check using the actual product.

2-3. Setting phase compensation

Phase setting procedure.
Stable negative feedback condition is achieved as follows:

・When the gain is set to 1 (0 dB), phase delay should not be more than 150° .Consequently, phase margin should not be less than 30° .
Also, since DC/DC converter applications are sampled according to the switching frequency, the whole system GBW should be set to not more than 1/10 of the switching frequency. The target characteristics of the applications can be summarized as follows:

・When the gain is set to 1 (0 dB), the phase delay should not be more than 150° .
And phase margin should not be less than 30° .
・The frequency when the gain is set to 0 dB should not be more than 1/10 of the switching frequency.

The responsiveness is determined by the GBW limitation. Consequently, to increase the circuit response, higher switching frequencies are required.
AVDD is in current mode control. The current mode control is a two-pole single-zero system. The poles are formed by the error amplifier and load while added zero is for phase compensation.
By placing poles appropriately, the circuit can maintain good stability and transient load response.
Bode plot diagram of general DC/DC converter is described below. At point (a), gain starts falling via the output impedance of the error amplifier and forms a pole by capacitor C_{cp}. When point (b) is reached, a zero is formed by resistor R_{pc} and capacitor C_{cp} to cancel the pole by loading and balance variation of Gain and phase.
The GBW (i.e., frequency when the gain is 0 dB) is determined by phase compensation capacitor connected to the error amplifier. If GBW is to be reduced, increase the capacitance of the capacitor.

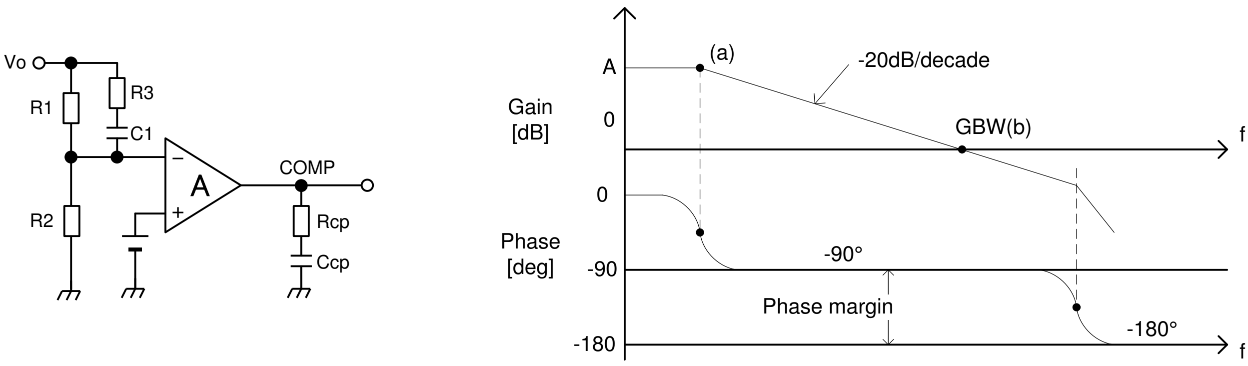


Figure 54. Setting phase compensation.

Formed Zero (fz1) by R_{cp} resistor and C_{cp} Capacitor are shown by using the following equation.
And also, Feed-forward capacitor C1 and R1 resistor both create Formed Zero (fz2) and it is used as boosting phase margin in the limited frequency area.

Phase lead $fZ1 = \frac{1}{2\pi CcpRcp}$ [Hz]

Phase lead $fZ2 = \frac{1}{2\pi C1R1}$ [Hz]

The formed zero fz2 phase compensation is built into the IC.

3. Positive Charge Pump : VGH

3-1. Selecting the Output rectifier diode

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Maximum output current	I_{OMAX}	＜	Diode Maximum Absolute Current
Maximum output voltage	AVDD	＜	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30%~40 for each parameter.

3-2. Selecting the Output PNP transistor

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Boost Converter Duty	$D = \frac{AVDD - VIN}{AVDD}$	
Maximum Output current	$\frac{I_{OMAX}}{D}$	＜Transistor Maximum Absolute Current
Power supply voltage	AVDD x 2	＜Transistor Maximum Absolute Voltage
DC gain	IOMAX / IBASE	＜Transistor hfe
Power dissipation (Doubler Mode)	(2 x AVDD – VGH – 2 x Vf) x IOUT	＜Transistor Power dissipation
Power dissipation (Tripler Mode)	(3 x AVDD – VGH – 4 x Vf) x IOUT	＜Transistor Power dissipation
Maximum DRVP current	IBASE（5mA）	

Provide sufficient design margins for a tolerance of 30%~40 for each parameter.

3-3. Selecting the base emitter resistor

100kΩ base-emitter resistor used to ensure proper operation.

3-4. Selecting the flying capacitor and the switch node resistor

A 0.1uF to 0.47uF flying capacitor and 1Ω to 20Ω resistor are appropriate for most applications.

3-5. Selecting the output capacitor

A 10uF ceramic capacitor is appropriate for most applications. More capacitor can be added to improve the load transient response.

4. Negative Charge Pump : VGL

4-1. Selecting the Output rectifier diode

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Maximum output current	I_{OMAX}	<	Diode Maximum Absolute Current
Maximum switching voltage	VIN	<	Diode Maximum Absolute Voltage

Provide sufficient design margins for a tolerance of 30%~40 for each parameter.

4-2. Selecting the Output NPN transistor

Select carefully in consideration of the maximum load current, maximum output voltage and power supply voltage.

Converter Duty	$D = \frac{VIN - VIO}{VIN}$	
Maximum Output current	$\frac{I_{OMAX}}{D}$	<Transistor Maximum Absolute Current
Power supply voltage	VIN	<Transistor Maximum Absolute Voltage
DC gain	IOMAX / IBASE	<Transistor hfe
Power dissipation (Doubler Mode)	(VIN - ｜ VGL ｜ – 2 x Vf) x IOUT	<Transistor Power dissipation
Maximum DRVN current	IBASE（5mA）	

Provide sufficient design margins for a tolerance of 30%~40 for each parameter.

4-3. Selecting the base emitter resistor

100kΩ base-emitter resistor used to ensure proper operation.

4-4. Selecting the flying capacitor and the switch node resistor

A 0.1uF to 0.47uF flying capacitor and 1Ω to 20Ω resistor are appropriate for most applications.

4-5. Selecting the output capacitor

A 10uF ceramic capacitor is appropriate for most applications. More capacitor can be added to improve the load transient response.

5. High Voltage LDO : HVLDO

5-1. Selecting the output capacitor

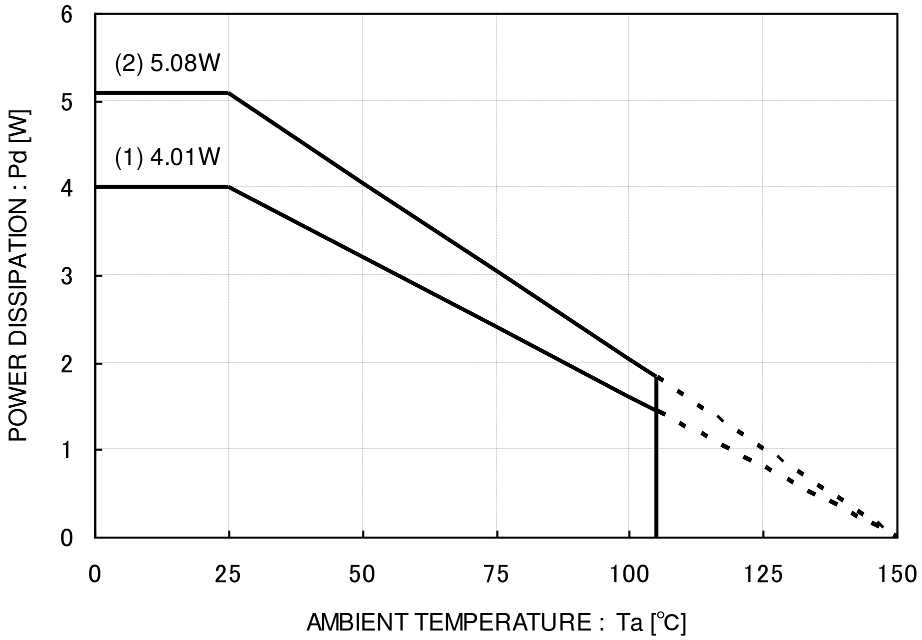
A 4.7uF to10uF ceramic capacitor is appropriate for most applications.

Layout Guideline

DC/DC converter switching line must be as short and thick as possible to reduce line impedance. If the wiring is long, ringing caused by switching would increase and this may exceed the absolute maximum voltage ratings. If the parts are located far apart, consider inserting a snubber circuit.

The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective. When there is unused area on PCB, please arrange the copper foil plain of DC nodes, such as GND, VIN and VOUT for helping heat dissipation of IC or circumference parts.

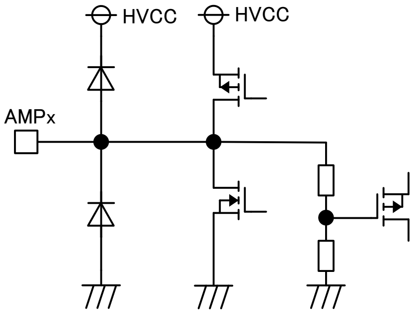
Power Dissipation



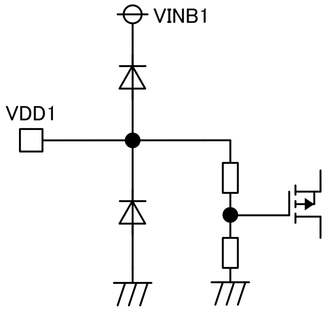
VQFN48V7070A Package
On 4-layer 114.3mm × 74.2mm × 1.6mm glass epoxy PCB
(1) 2-layer board (Backside copper foil area 74.2 mm × 74.2 mm)
(2) 4-layer board (The 2nd, 3rd layers and backside copper foil area 74.2 mm × 74.2 mm)

I/O Equivalence Circuit

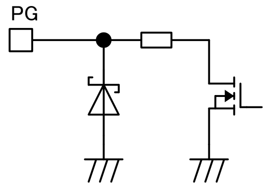
1, 2, 47, 48. AMP1~4



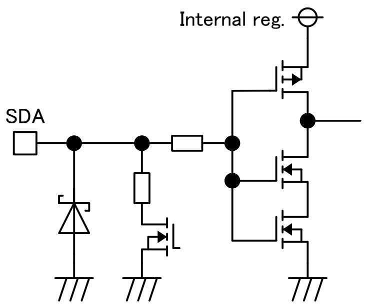
3. VDD1



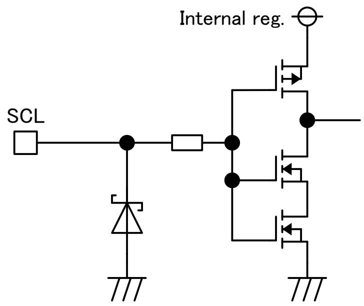
4.PG



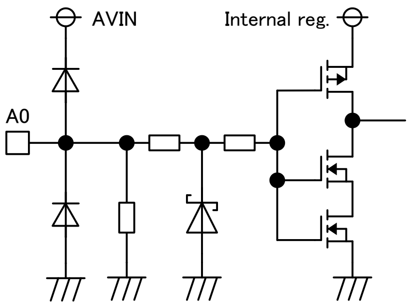
5.SDA



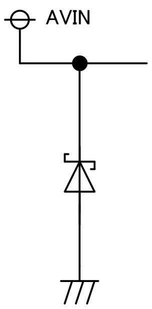
6.SCL



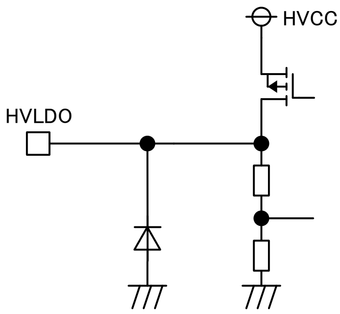
7.A0



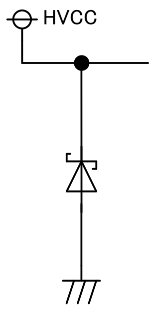
8. AVIN



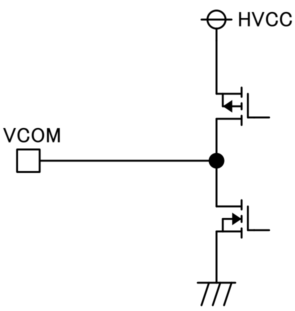
9.HVLDO



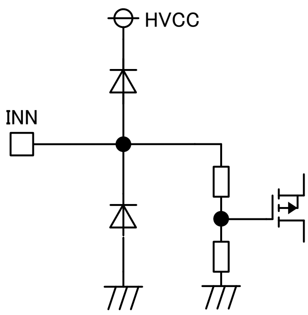
10. HVCC



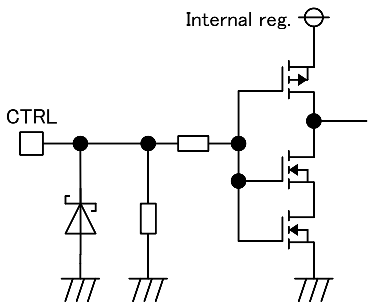
11.VCOM



12. INN

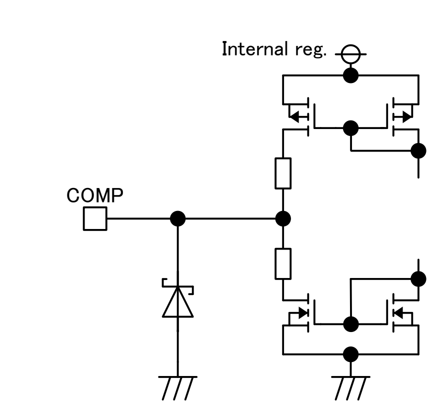


13. CTRL

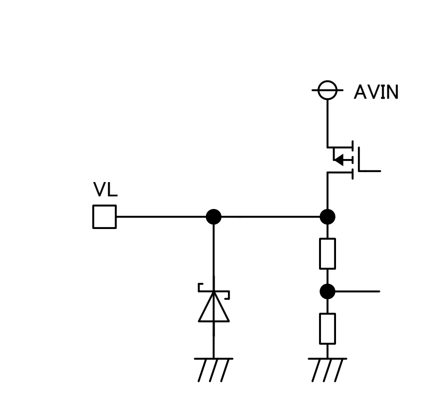


I/O Equivalence Circuit - continued

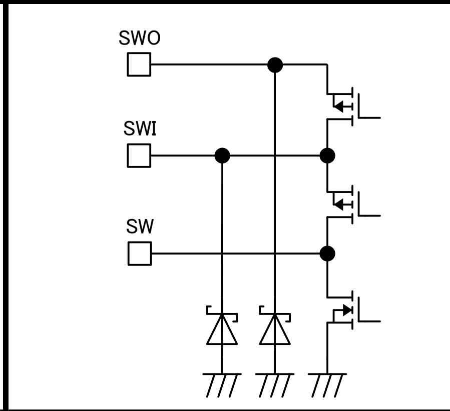
15.COMP



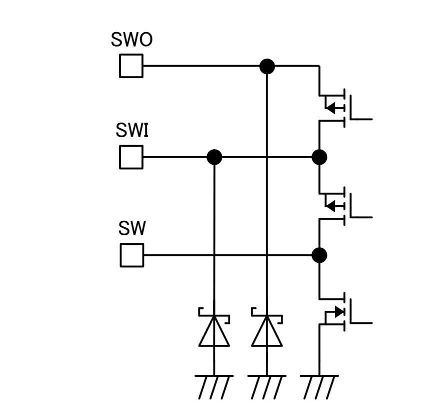
16.VL



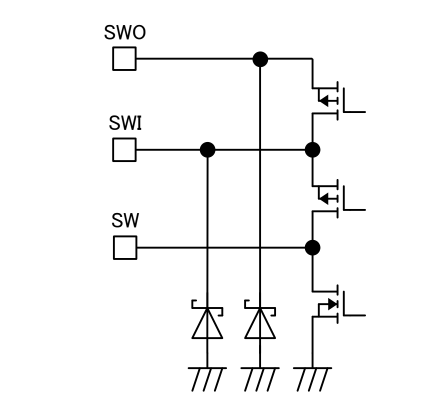
19, 20.SW



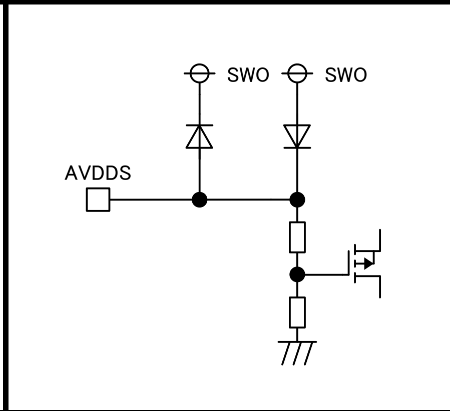
21.SWI



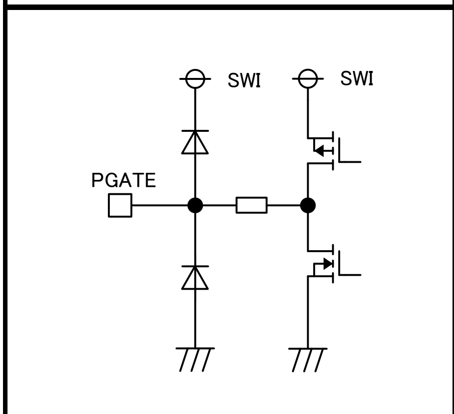
22.SWO



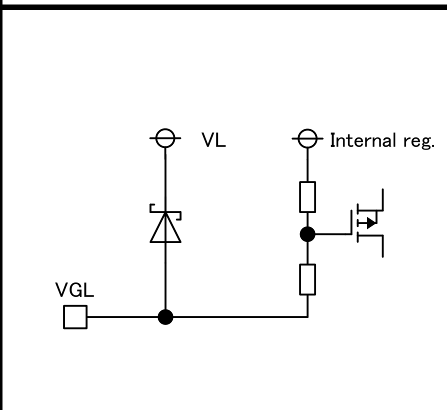
23.AVDDS



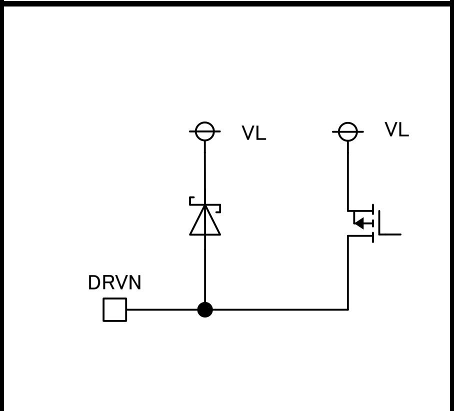
24.PGATE



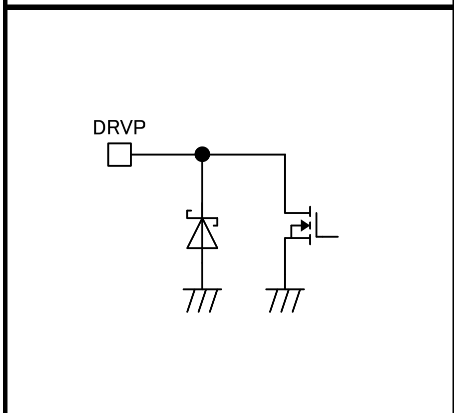
25.VGL



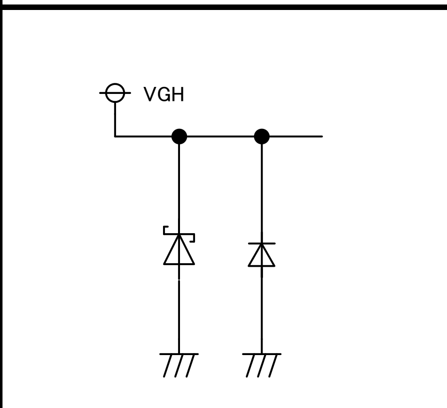
26.DRVN



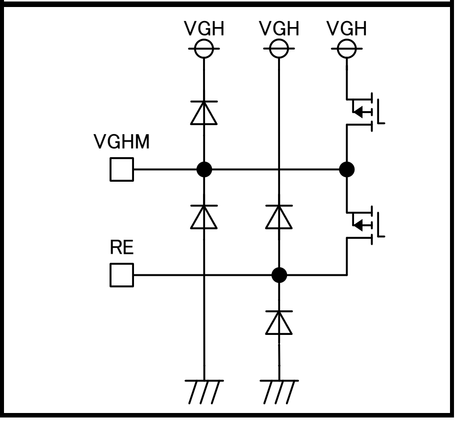
27.DRVP



28.VGH

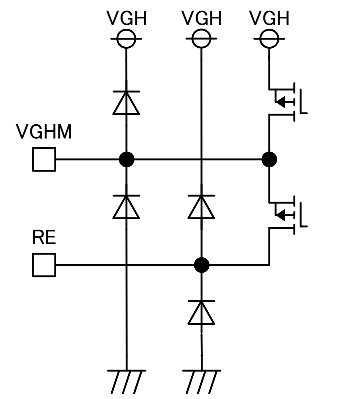


29.VGHM

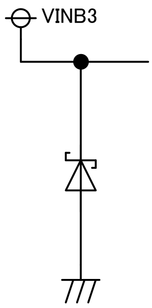


I/O Equivalence Circuit - continued

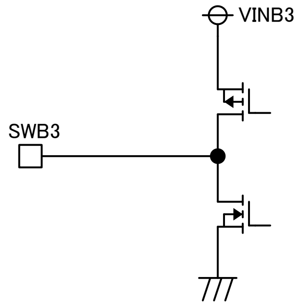
30.RE



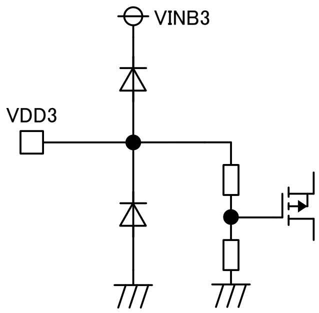
31.VINB3



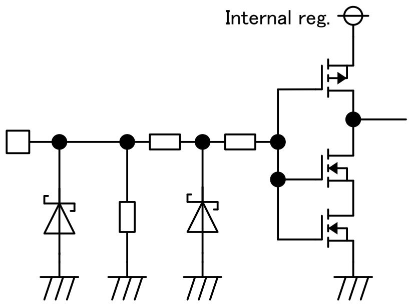
33. SWB3



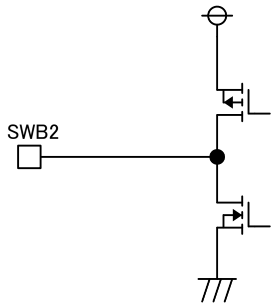
35. VDD3



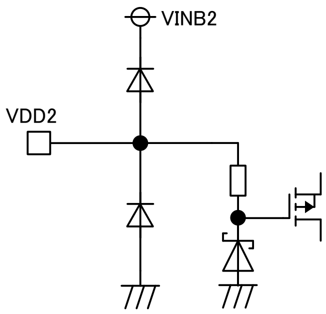
36. EN



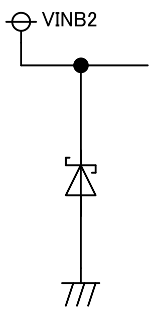
38. SWB2



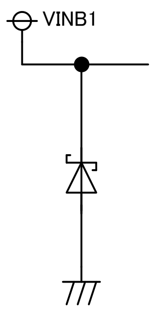
39. VDD2



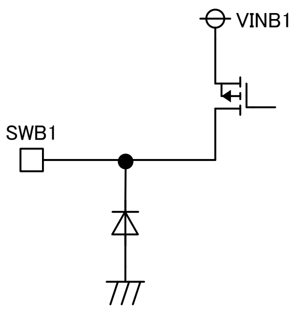
40. VINB2



41, 42.VINB1



44, 45. SWB1



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Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

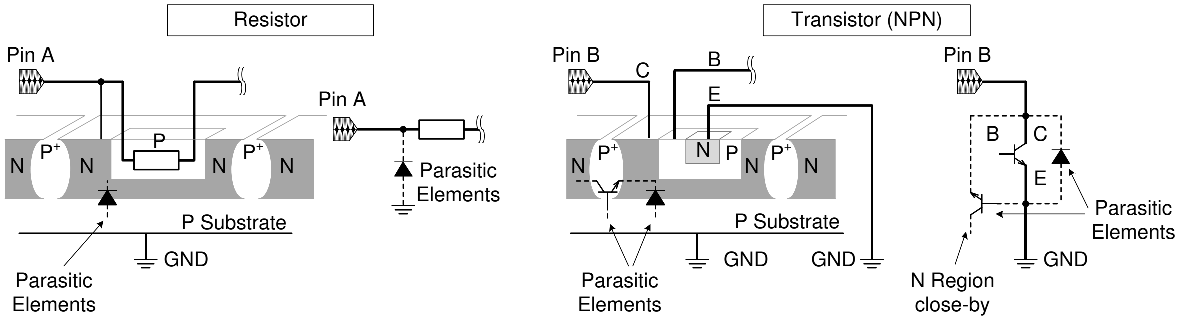


Figure 55. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

B	M	8	1	0	0	4	M	U	V		ZE2

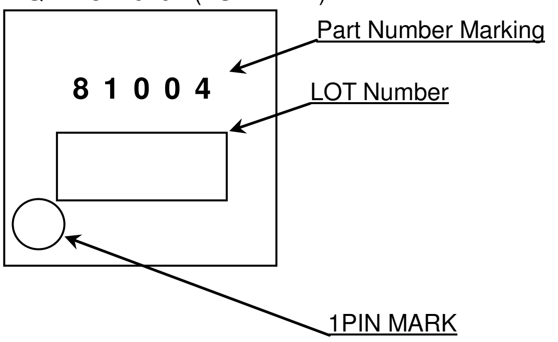
Part number

Package
MUV:VQFN48V7070A

Packaging and forming specification
ZE2: Embossed tape and reel

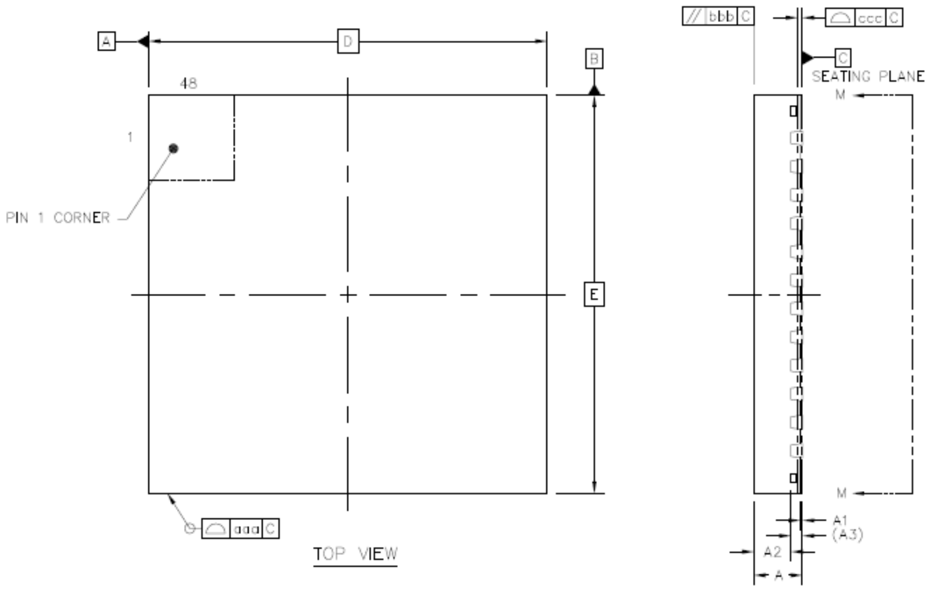
Marking Diagram

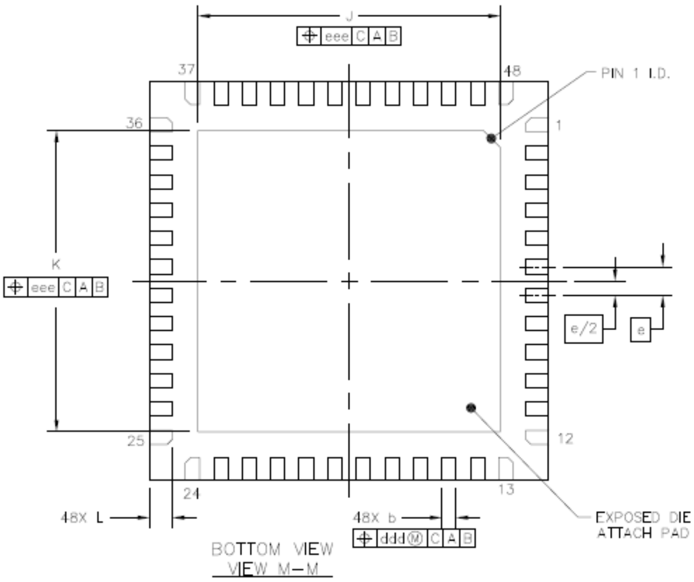
VQFN48V7070A (TOP VIEW)



Physical Dimension Tape and Reel Information

Package Name	VQFN48V7070A

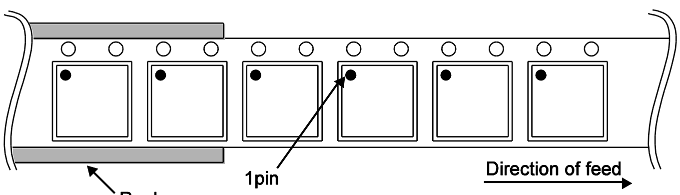




		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	**ZE2** (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision history

Date	Revision	Contents
2014.09.16	001	New release
2014.12.04	002	Page 8/49 TSD: MIN, MAX added Page 9/49 VOVP_VIO, VOVP_VCORE and VOVP_HAVDD: MIN, MAX added

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since our Products might fall under controlled goods prescribed by the applicable foreign exchange and foreign trade act, please consult with ROHM representative in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data. ROHM shall not be in any way responsible or liable for infringement of any intellectual property rights or other damages arising from use of such information or data.:

2. No license, expressly or implied, is granted hereby under any intellectual property rights or other rights of ROHM or any third parties with respect to the information contained in this document.

Other Precaution

1. This document may not be reprinted or reproduced, in whole or in part, without prior written consent of ROHM.

2. The Products may not be disassembled, converted, modified, reproduced or otherwise changed without prior written consent of ROHM.

3. In no event shall you use in any way whatsoever the Products and the related technical information contained in the Products or this document for any military purposes, including but not limited to, the development of mass-destruction weapons.

4. The proper names of companies or products described in this document are trademarks or registered trademarks of ROHM, its affiliated companies or third parties.

General Precaution

1. Before you use our Products, you are requested to carefully read this document and fully understand its contents. ROHM shall not be in any way responsible or liable for failure, malfunction or accident arising from the use of any ROHM's Products against warning, caution or note contained in this document.

2. All information contained in this document is current as of the issuing date and subject to change without any prior notice. Before purchasing or using ROHM's Products, please confirm the latest information with a ROHM sales representative.

3. The information contained in this document is provided on an "as is" basis and ROHM does not warrant that all information contained in this document is accurate and/or error-free. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties resulting from inaccuracy or errors of or concerning such information.