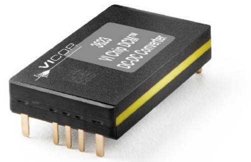
DCM™ DC-DC Converter

MIL-COTS
MDCM28AP480M320A50



Isolated, Regulated DC Converter

Features

- Isolated, regulated DC-DC converter
- Up to 320 W, 6.67 A continuous
- 92.6% peak efficiency
- 818 W/in³ Power density
- Wide input range 16 – 50 Vdc
- Safety Extra Low Voltage (SELV) 48.0 V Nominal Output
- 2250 Vdc isolation
- ZVS high frequency switching
  - Enables low-profile, high-density filtering
- Optimized for array operation
  - Up to 8 units – 2560 W
  - No power derating needed
  - Sharing strategy permits dissimilar line voltages across an array
- Fully operational current limit
- OV, OC, UV, short circuit and thermal protection
- 3623 through-hole ChiP package
  - 1.524" x 0.898" x 0.286" (38.72 mm x 22.8 mm x 7.26 mm)

Typical Applications

- Radar, Range Finding
- Guidance Systems, Computing
- Motor Drive
- Display, GPS, Radio

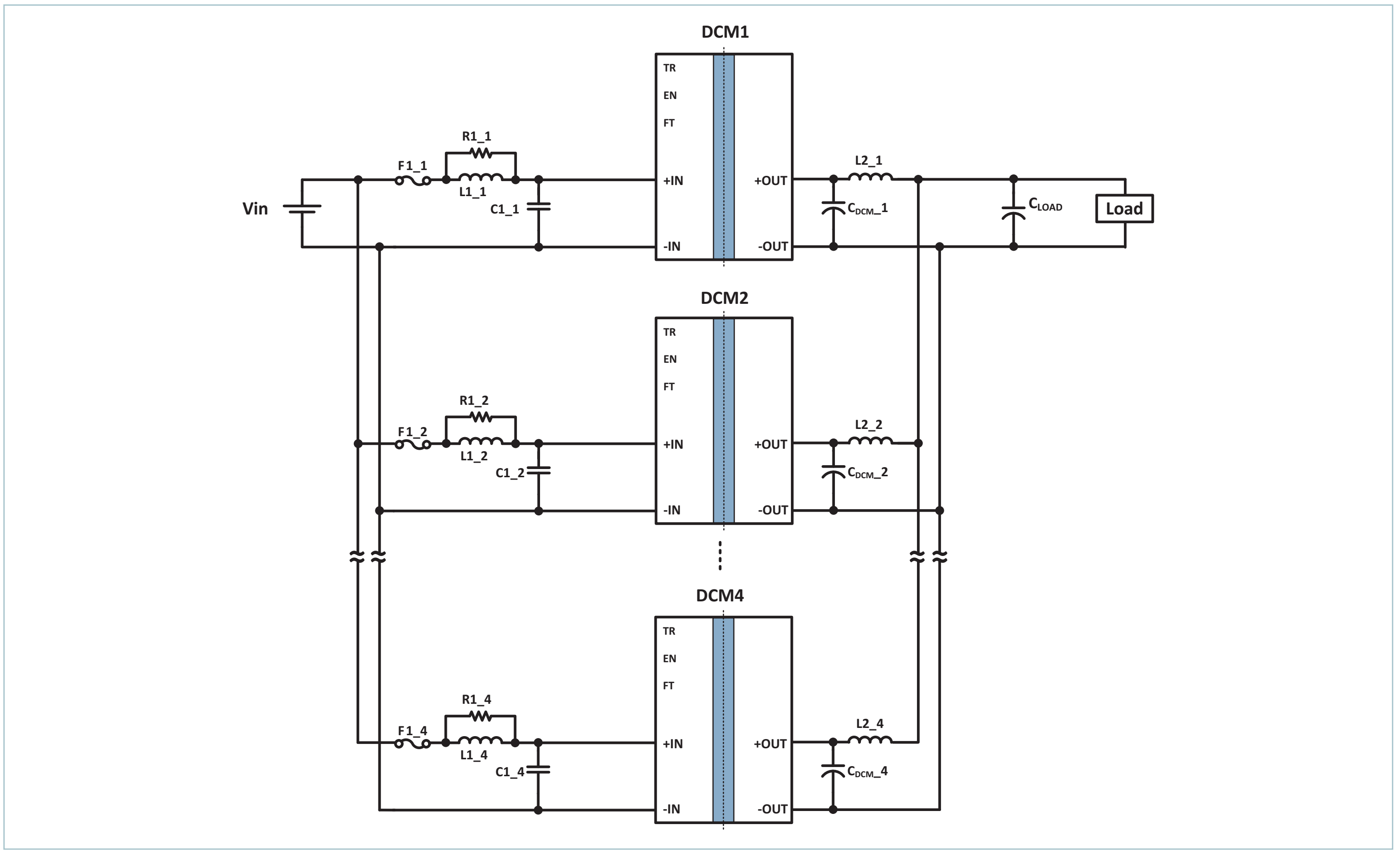
Product Ratings	
V_{IN} = 16 V to 50 V	P_{OUT} = 320 W
V_{OUT} = 48.0 V (28.8 V to 52.8 V Trim)	I_{OUT} = 6.67 A

Product Description

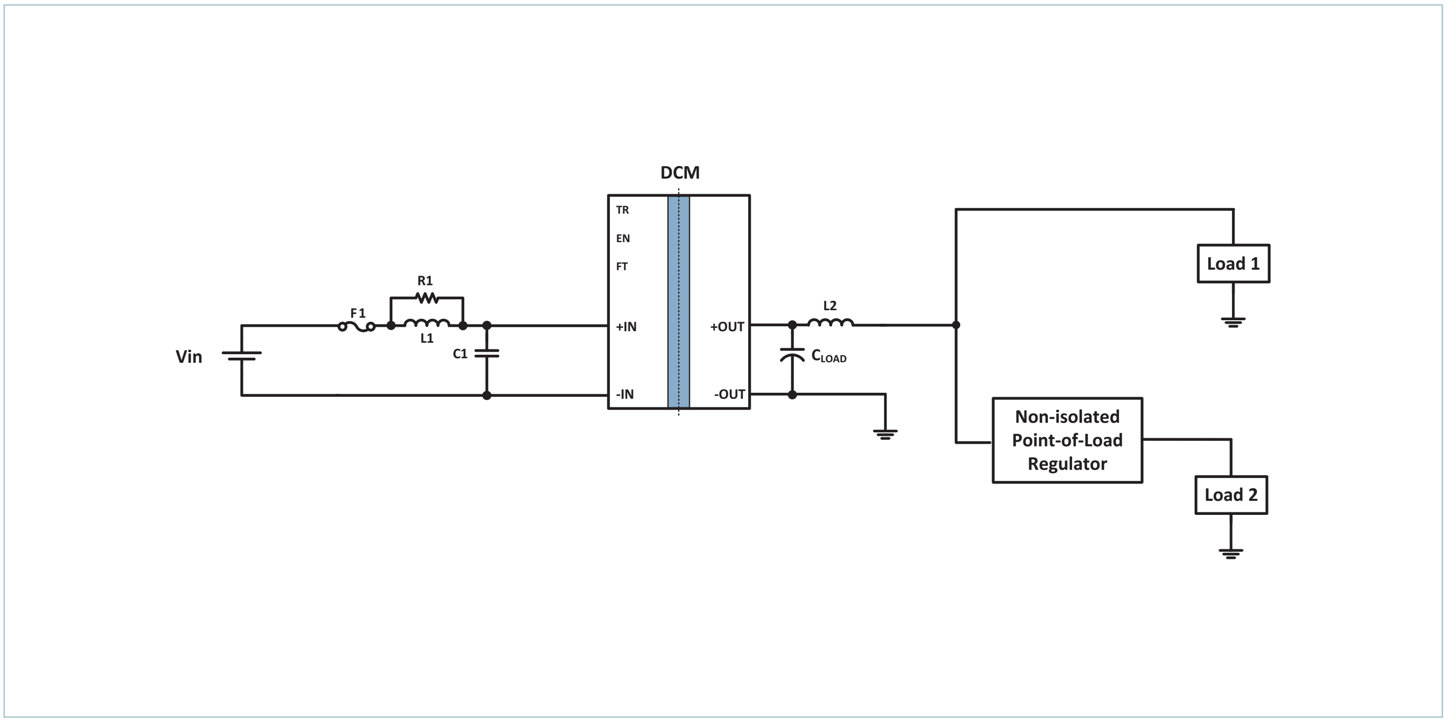
The DCM Isolated, Regulated DC Converter is a DC-DC converter, operating from an unregulated, wide range input to generate an isolated 48.0 Vdc output. With its high frequency zero voltage switching (ZVS) topology, the DCM converter consistently delivers high efficiency across the input line range. Modular DCM converters and downstream DC-DC products support efficient power distribution, providing superior power system performance and connectivity from a variety of unregulated power sources to the point-of-load.

Leveraging the thermal and density benefits of Vicor's ChiP packaging technology, the DCM module offers flexible thermal management options with very low top and bottom side thermal impedances. Thermally-adept ChiP based power components enable customers to achieve cost effective power system solutions with previously unattainable system size, weight and efficiency attributes, quickly and predictably.

Typical Application

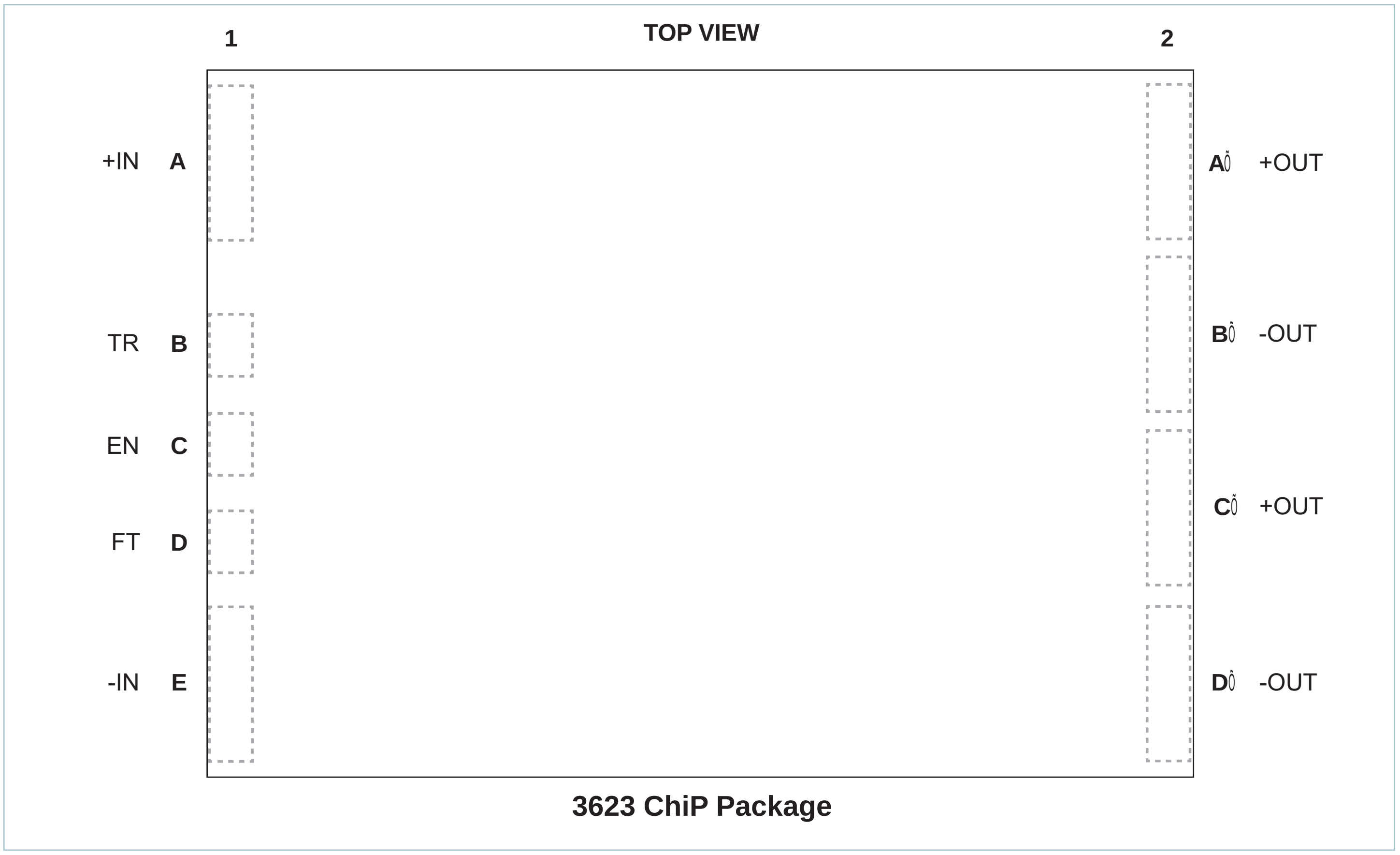


Typical Application 1: MDCM28AP480M320A50 in an array of four units



Typical Application 2: Single MDCM28AP480M320A50, to a non-isolated regulator, and direct to load

Pin Configuration



Pin Descriptions

Pin Number	Signal Name	Type	Function
A1	+IN	INPUT POWER	Positive input power terminal
B1	TR	INPUT	Enables and disables trim functionality. Adjusts output voltage when trim active.
C1	EN	INPUT	Enables and disables power supply
D1	FT	OUTPUT	Fault monitoring
E1	-IN	INPUT POWER RETURN	Negative input power terminal
A'2, C'2	+OUT	OUTPUT POWER	Positive output power terminal
B'2, D'2	-OUT	OUTPUT POWER RETURN	Negative output power terminal

Part Ordering Information

Device	Input Voltage Range	Package Type	Output Voltage x 10	Temperature Grade	Output Power	Revision	Version
MDCM	28A	P	480	M	320	A5	0
MDCM = MDCM	28A = 16/28/50 V	P = ChiP TH	480 = 48 V	M = -55 to 125°C	320 = 320 W	A5	Analog Control Interface Version

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device. Electrical specifications do not apply when operating beyond rated operating conditions.

Parameter	Comments	Min	Max	Unit
Input Voltage (+IN to –IN)		-0.5	65.0	V
Input Voltage Slew Rate		-1	1	V/µs
TR to - IN		-0.3	3.5	V
EN to -IN		-0.3	3.5	V
FT to -IN		-0.3	3.5	V
			5	mA
Output Voltage (+Out to –Out)		-0.5	62.4	V
Dielectric withstand (input to output)	Basic insulation	2250		Vdc
Internal Operating Temperature	M Grade	-55	125	°C
Storage Temperature	M Grade	-65	125	°C
Average Output Current			10.3	A

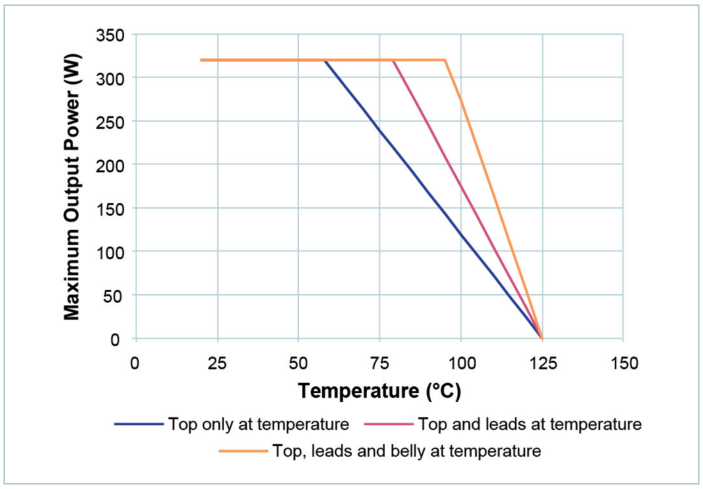


Figure 1 *— Thermal Specified Operating Area: Max Output Power vs. Case Temp, Single unit at minimum full load efficiency*

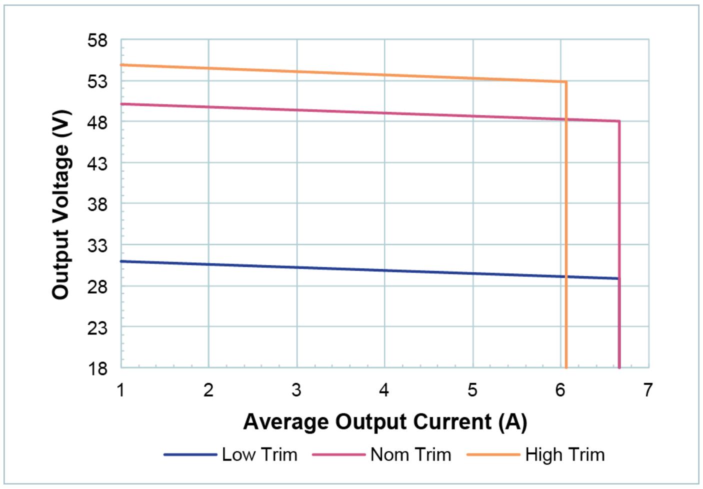


Figure 2 *— Electrical Specified Operating Area*

Electrical Specifications

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of -55°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Input Specification						
Input voltage range	V_{IN}	Continuous operation	**16**	**28**	**50**	V
Inrush current (peak)	I_{INRP}	With maximum $C_{OUT-EXT}$, full resistive load			**25.0**	A
Input capacitance (internal)	C_{IN-INT}	Effective value at nominal input voltage		29.7		µF
Input capacitance (internal) ESR	$R_{CIN-INT}$	At 1 MHz		0.73		mΩ
Input inductance (external)	L_{IN}	Differential mode, with no further line bypassing			**1**	µH
No Load Specification						
Input power – disabled	P_Q	Nominal line, see Fig. 3		0.4	0.8	W
		Worst case line, see Fig. 3			**1.0**	W
Input power – enabled with no load	P_{NL}	Nominal line, see Fig. 4		8.2	9.9	W
		Worst case line, see Fig. 4			**12.0**	W
Power Output Specification						
Output voltage set point	$V_{OUT-NOM}$	V_{IN} = 28 V, nominal trim, at 100% Load, T_{INT} = 25°C	47.75	48.0	48.24	V
Rated output voltage trim range	$V_{OUT-TRIMMING}$	Trim range over temp, with > 10% rated load. Specifies the Low, Nominal and High Trim conditions.	**28.8**	**48.0**	**52.8**	V
Output voltage load regulation	$\Delta V_{OUT-LOAD}$	Linear load line. Output voltage increase from full rated load current to no load (Does not include light load regulation). See Fig. 6 and Sec. Design Guidelines	2.2618	2.5262	2.7936	V
Output voltage light load regulation	ΔV_{OUT-LL}	0% to 10% load, additional V_{OUT} relative to calculated load-line point; see Fig. 6 and Sec. Design Guidelines	**0.0**		**5.05**	V
Output voltage temperature coefficient	$\Delta V_{OUT-TEMP}$	Nominal, linear temperature coefficient, relative to T_{INT} = 25°C. See Fig. 5 and Design Guidelines Section		**-6.40**		mV/°C
V_{OUT} accuracy	$\%V_{OUT-ACCURACY}$	The total output voltage setpoint accuracy from the calculated ideal V_{OUT} based on load, temp and trim. Excludes ΔV_{OUT-LL}	**-2.0**		**2.0**	%
Rated output power	P_{OUT}	Continuous, V_{OUT} ≥ 48.0 V	**320**			W
Rated output current	I_{OUT}	Continuous, V_{OUT} ≤ 48.0 V	**6.67**			A
Output current limit	I_{OUT-LM}	Of rated I_{OUT} max. Fully operational current limit, for nominal trim and below	100	120	143	%
Current limit delay	$t_{IOUT-LIM}$	The module will power limit in a fast transient event		1		ms
Efficiency	η	Full load, nominal line, nominal trim	92.1	92.6		%
		Full load, over line and temperature, nominal trim	**88.5**			%
		50% load, over rated line, temperature and trim	**87.2**			%
Output voltage ripple	V_{OUT-PP}	Over all operating steady-state line and trim conditions, 20 MHz BW, minimum $C_{OUT-EXT}$, and at least 10 % rated load		1072		mV
Output capacitance (internal)	$C_{OUT-INT}$	Effective value at nominal output voltage		11		µF
Output capacitance (internal) ESR	$R_{COUT-INT}$	At 1 MHz		0.222		mΩ
Output capacitance (external)	$C_{OUT-EXT}$	20 MHz bandwidth. At nominal trim, minimum $C_{OUT-EXT}$ and at least > 10% rated load	**200**		**2000**	µF
Output capacitance (external)	$C_{OUT-EXT-TRANS}$	Excludes component temperature coefficient For load transients down to 0% rated load, with static trim	**200**		**2000**	µF
Output capacitance (external)	$C_{OUT-EXT-TRANS-TRIM}$	Excludes component temperature coefficient For load transients down to 0% rated load, with dynamic trimming	**200**		**2000**	µF

Electrical Specifications (cont.)

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of -55°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Power Output Specifications (Cont.)						
Output capacitance, ESR (ext.)	$R_{COUT\text{-}EXT}$	At 10 kHz, excludes component tolerances	**10**			mΩ
Initialization delay	t_{INIT}	See state diagram		25	**40**	ms
Output turn-on delay	t_{ON}	From rising edge EN, with V_{IN} pre-applied. See timing diagram		200		µs
Output turn-off delay	t_{OFF}	From falling edge EN. See timing diagram			**600**	µs
Soft start ramp time	t_{SS}	At full rated resistive load. Typ spec is 1-up with min $C_{OUT\text{-}EXT}$. Max spec is for arrays with max $C_{OUT\text{-}EXT}$		120	**200**	ms
V_{OUT} threshold for max rated load current	$V_{OUT\text{-}FL\text{-}THRESH}$	During startup, V_{OUT} must achieve this threshold before output can support full rated current			**24.0**	V
I_{OUT} at startup	$I_{OUT\text{-}START}$	Max load current at startup while V_{OUT} is below $V_{OUT\text{-}FL\_THRESH}$	**0.66**			A
Monotonic soft-start threshold voltage	$V_{OUT\text{-}MONOTONIC}$	Output voltage rise becomes monotonic with 25% of preload once it crosses $V_{OUT\text{-}MONOTONIC}$			**24.0**	V
Minimum required disabled duration	$t_{OFF\text{-}MIN}$	This refers to the minimum time a module needs to be in the disabled state before it will attempt to start via EN			**2**	ms
Minimum required disabled duration for predictable restart	$t_{OFF\text{-}MONOTONIC}$	This refers to the minimum time a module needs to be in the disabled state before it is guaranteed to exhibit monotonic soft-start and have predictable startup timing			**100**	ms
Voltage deviation (transient)	$\%V_{OUT\text{-}TRANS}$	Minimum C_{OUT_EXT} (10 ↔ 90% load step), excluding load line.		<10		%
Settling time	t_{SETTLE}			12.0		ms
Powertrain Protections						
Input Voltage Initialization threshold	$V_{IN\text{-}INIT}$	Threshold to start t_{INIT} delay			**6**	V
Input Voltage Reset threshold	$V_{IN\text{-}RESET}$	Latching faults will clear once V_{IN} falls below $V_{IN\text{-}RESET}$	**3**			V
Input undervoltage recovery threshold	$V_{IN\text{-}UVLO-}$		**10**		**15**	V
Input undervoltage lockout threshold	$V_{IN\text{-}UVLO+}$	See Timing diagram			**16**	V
Input overvoltage lockout threshold	$V_{IN\text{-}OVLO+}$				**55**	V
Input overvoltage recovery threshold	$V_{IN\text{-}OVLO-}$	See Timing diagram	**50**			V
Output overvoltage threshold	$V_{OUT\text{-}OVP}$	From 25% to 100% load. Latched shutdown	**60.0**			V
Output overvoltage threshold	$V_{OUT\text{-}OVP\text{-}LL}$	From 0% to 25% load. Latched shutdown	**62.4**			V
Minimum current limited V_{OUT}	$V_{OUT\text{-}UVP}$	Over all operating steady-state line and trim conditions			**18**	V
Overtemperature threshold (internal)	$T_{INT\text{-}OTP}$		**125**			°C
Power limit	P_{LIM}				**700**	W
V_{IN} overvoltage to cessation of powertrain switching	$t_{OVLO\text{-}SW}$	Independent of fault logic		1.4		µs
V_{IN} overvoltage response time	t_{OVLO}	For fault logic only			**200**	µs
V_{IN} undervoltage response time	t_{UVLO}				**100**	ms
Short circuit response time	t_{SC}	Powertrain on, operational state			**200**	µs
Short circuit, or temperature fault recovery time	t_{FAULT}	See Timing diagram		1		s

Signal Specifications

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of -55°C < T_{INT} < 125°C.

Enable: EN

- The EN pin enables and disables the DCM converter; when held low the unit will be disabled.
- The EN pin has an internal pull-up to VCC and is referenced to the -IN pin of the converter.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	NOM	MAX	UNIT
DIGITAL INPUT	Any	EN enable threshold	$V_{ENABLE-EN}$				**2.31**	V
		EN disable threshold	$V_{ENABLE-DIS}$		**0.99**			V
		Internally generated V_{CC}	V_{CC}		**3.21**	3.30	**3.39**	V
		EN internal pull up resistance to V_{CC}	$R_{ENABLE-INT}$		**9.5**	10.0	**10.5**	kΩ

Trim: TR

- The TR pin enables and disables trim functionality when V_{IN} is initially applied to the DCM converter. When Vin first crosses $V_{IN-UVLO+}$, the voltage on TR determines whether or not trim is active.
- If TR is not floating at power up and has a voltage less than TR trim enable threshold, trim is active.
- If trim is active, the TR pin provides dynamic trim control with at least 30Hz of -3dB control bandwidth over the output voltage of the DCM converter.
- The TR pin has an internal pull-up to V_{CC} and is referenced to the -IN pin of the converter.

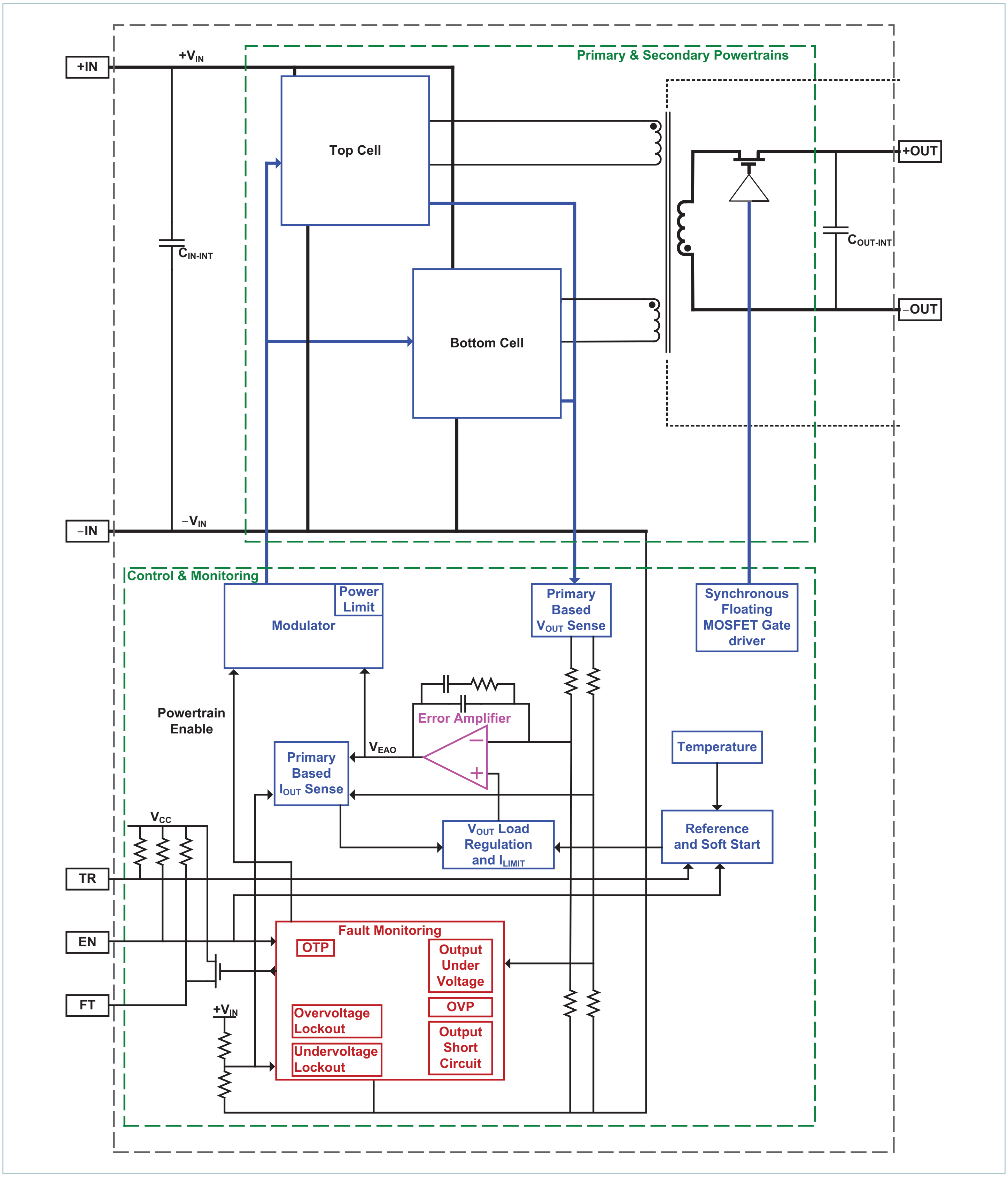
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	NOM	MAX	UNIT
DIGITAL INPUT	Startup	TR trim disable threshold	$V_{TRIM-DIS}$	Trim disabled when TR above this threshold at power up			**3.20**	V
		TR trim enable threshold	$V_{TRIM-EN}$	Trim enabled when TR below this threshold at power up	**3.15**			V
ANALOG INPUT	Operational with Trim enabled	Internally generated V_{CC}	V_{CC}		**3.21**	3.30	**3.39**	V
		TR pin functional range	$V_{TRIM-RANGE}$		0.00	2.46	3.16	V
		V_{OUT} referred TR pin resolution	$V_{OUT-RES}$	With V_{CC} = 3.3 V		70		mV
		TR internal pull up resistance to V_{CC}	$R_{TRIIM-INT}$		**9.5**	10.0	**10.5**	kΩ

Fault: FT

- The FT pin is a Fault flag pin.
- When the module is enabled and no fault is present, the FT pin does not have current drive capability.
- Whenever the powertrain stops (due to a fault protection or disabling the module by pulling EN low), the FT pin output Vcc and provides current to drive an external ciruit.
- When module starts up, the FT pin is pulled high to V_{CC} during microcontroller initialization and will remain high until soft start process starts.

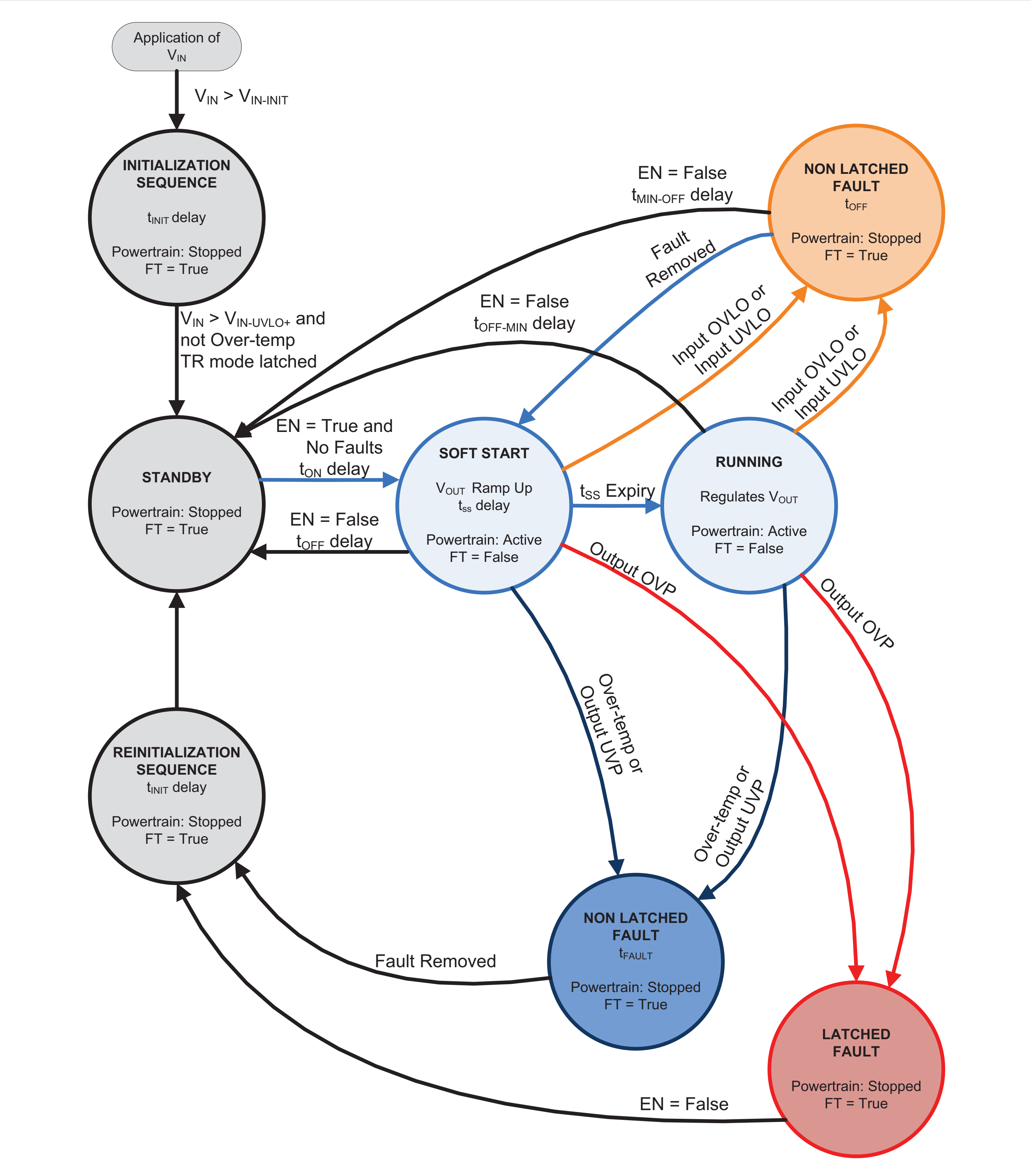
SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	NOM	MAX	UNIT
DIGITAL OUTPUT	Any	FT internal pull up resistance to V_{CC}	$R_{FAULT-INT}$		**474**	499	**524**	kΩ
	FT Active	FT voltage	$V_{FAULT-ACTIVE}$	At rated current drive capability	**3.0**			V
		FT current drive capability	$I_{FAULT-ACTIVE}$	Over-load beyond the ABSOLUTE MAXIMUM ratings may cause module damage	**4**			mA
		FT response time	$t_{FT-ACTIVE}$	Delay from cessation of switching to FT Pin Active			**200**	µs

Functional Block Diagram



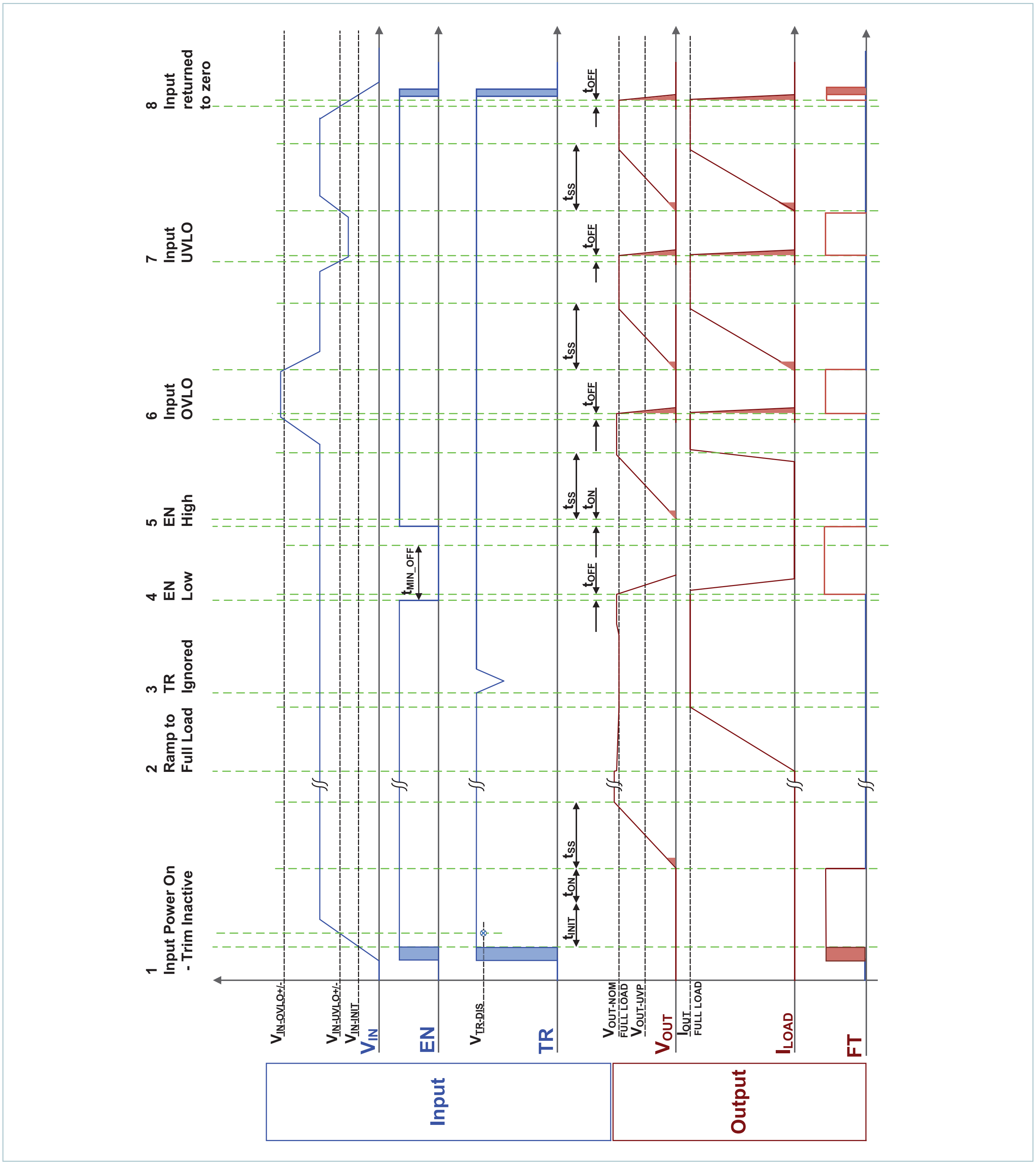
High Level Functional State Diagram

Conditions that cause state transitions are shown along arrows. Sub-sequence activities listed inside the state bubbles.



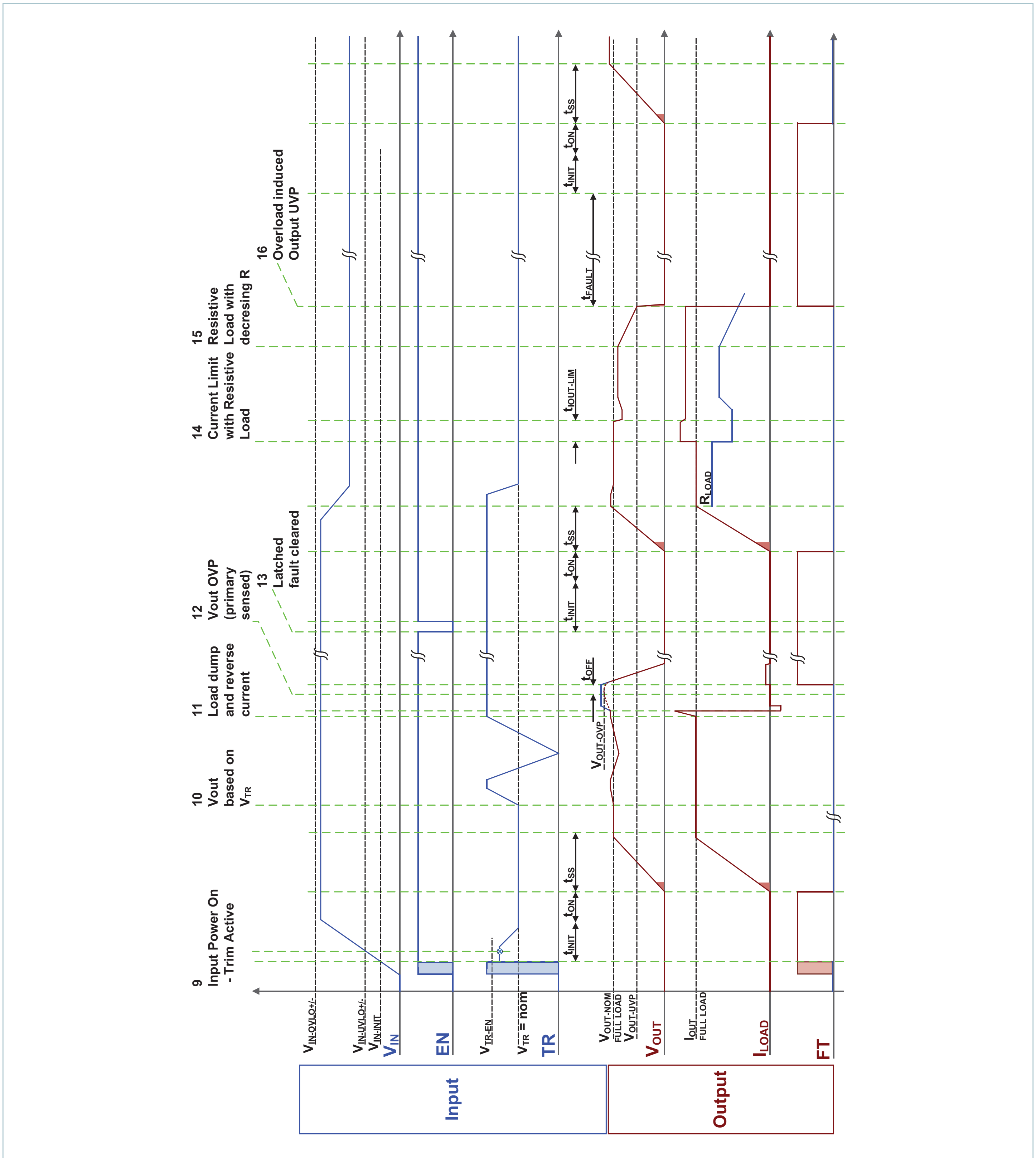
Timing Diagrams

Module Inputs are shown in blue; Module Outputs are shown in brown.



Timing Diagrams (Cont.)

Module Inputs are shown in blue; Module Outputs are shown in brown.



Typical Performance Characteristics

The following figures present typical performance at T_C = 25°C, unless otherwise noted. See associated figures for general trend data.

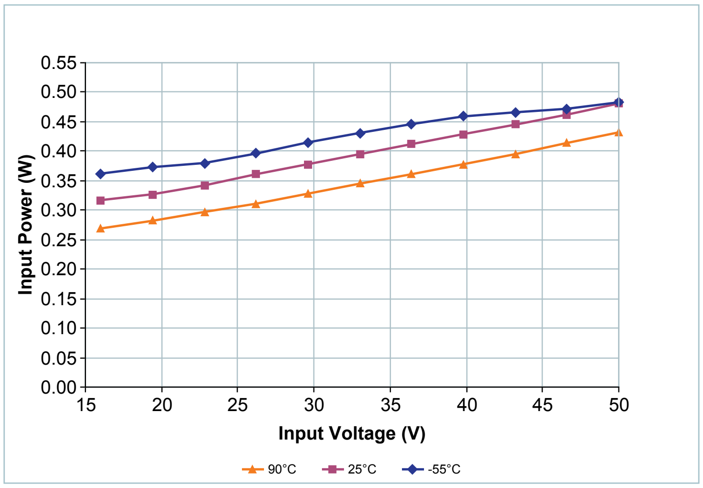


Figure 3 *— Disabled power dissipation vs. V_{IN}*

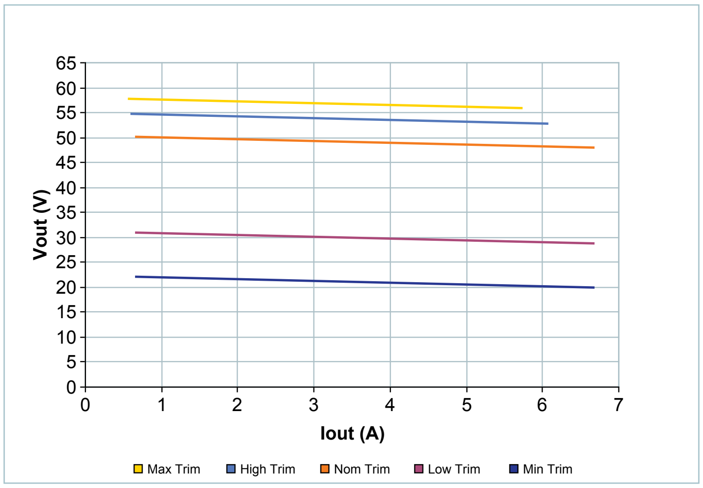


Figure 6 *— Ideal V_{OUT} vs. load current, at 25°C case*

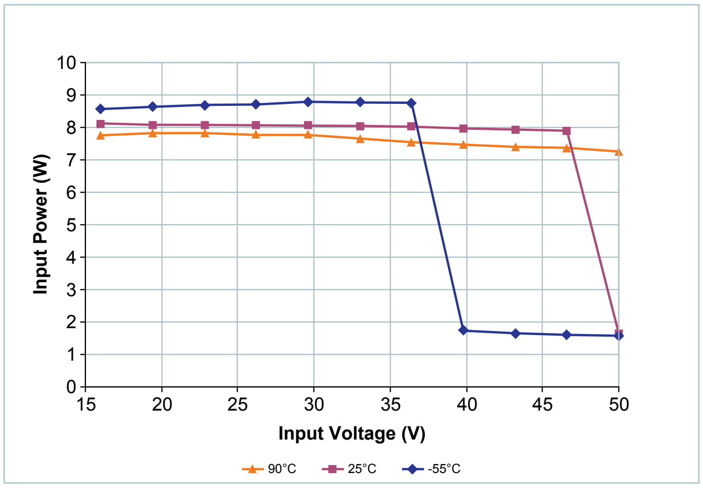


Figure 4 *— No load power dissipation vs. V_{IN}, at nominal trim*

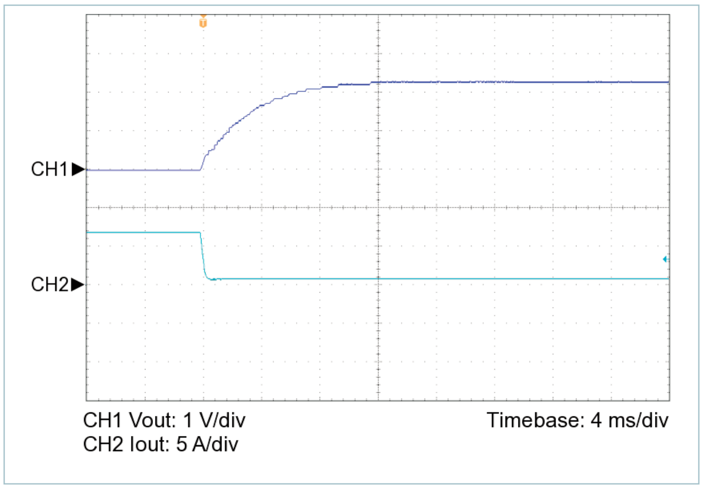


Figure 7 *— 100% to 10% load transient response, V_{IN} = 28 V, nominal trim, C_{OUT_EXT} = 200 µF*

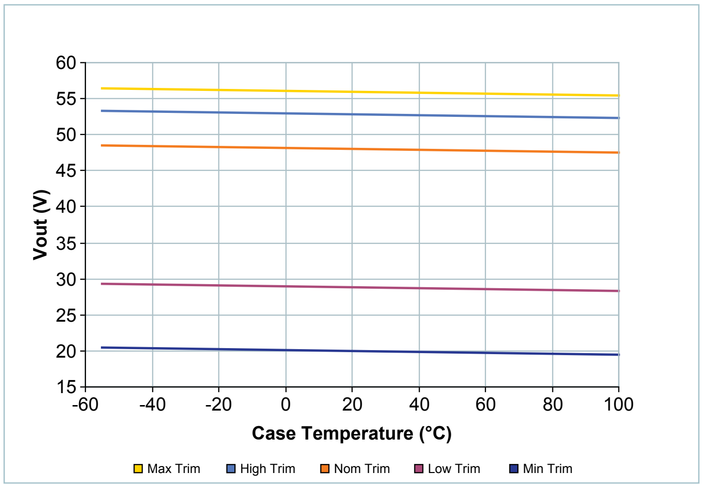


Figure 5 *— Ideal V_{OUT} vs. case temperature, at full load*

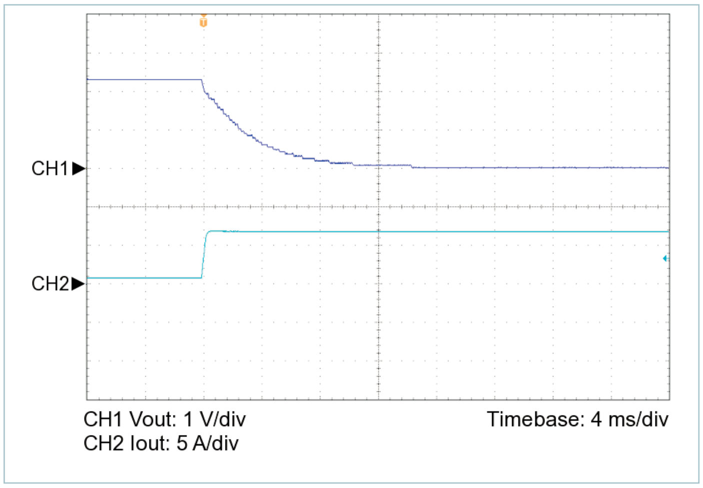


Figure 8 *— 10% to 100% load transient response, V_{IN} = 28 V, nominal trim, C_{OUT_EXT} = 200 µF*

Typical Performance Characteristics (cont.)

The following figures present typical performance at $T_C = 25°C$, unless otherwise noted. See associated figures for general trend data.

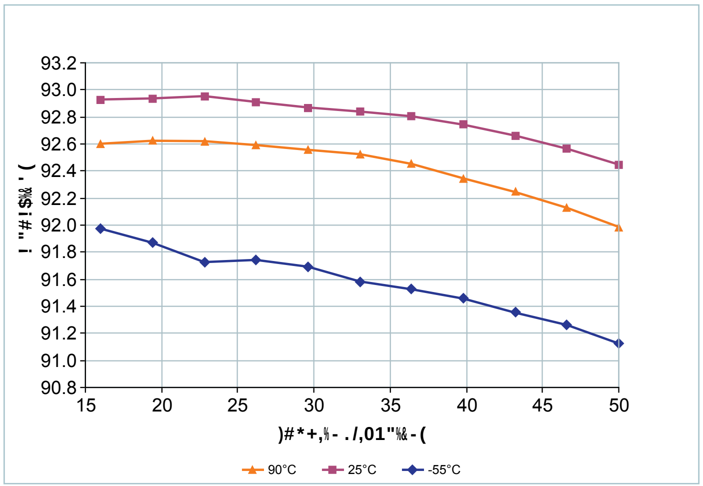


Figure 9 *— Full Load Efficiency vs. V_{IN}, at low trim*

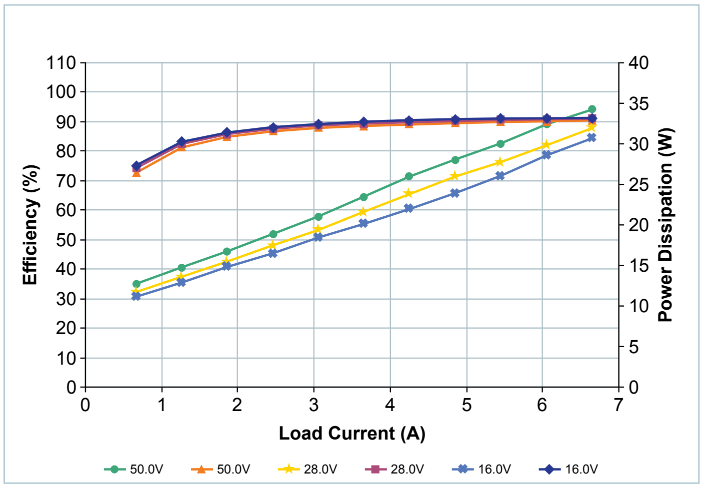


Figure 12 *— Efficiency and power dissipation vs.load at T_{CASE} = -55°C, nominal trim*

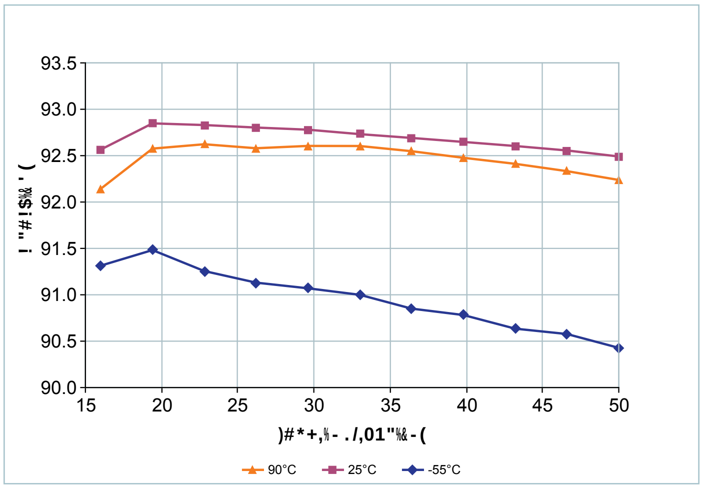


Figure 10 *— Full Load Efficiency vs. V_{IN}, at nominal trim*

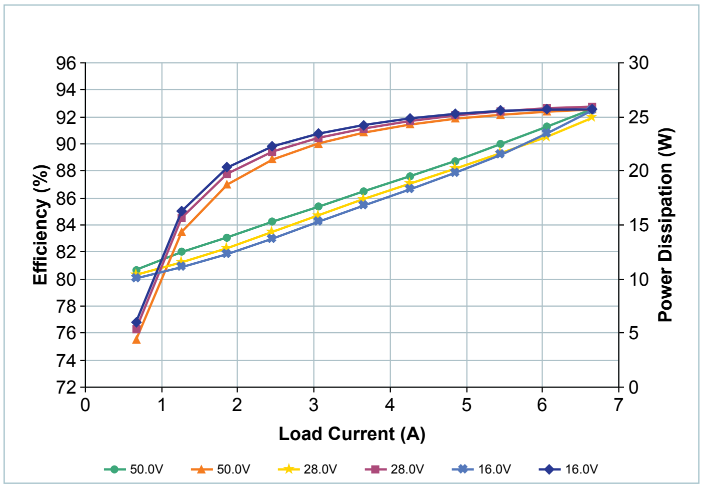


Figure 13 *— Efficiency and power dissipation vs.load at T_{CASE} = 25°C, nominal trim*

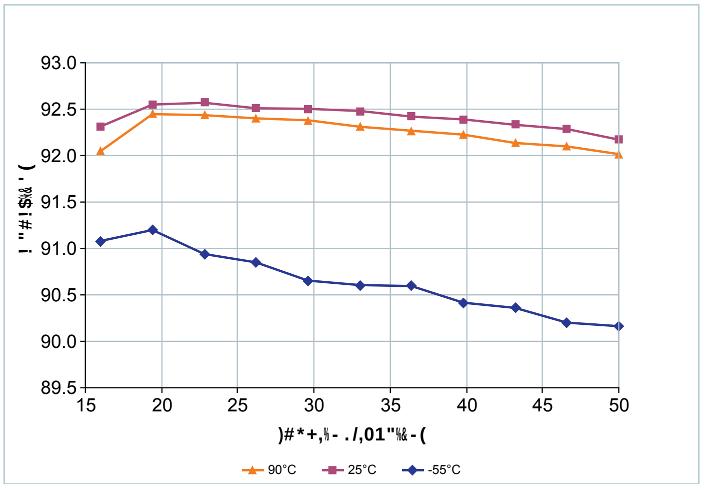


Figure 11 *— Full Load Efficiency vs. V_{IN}, at high trim*

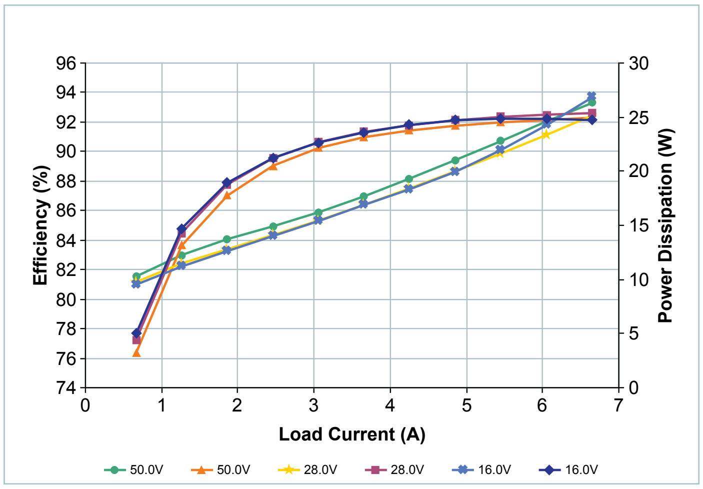


Figure 14 *— Efficiency and power dissipation vs.load at T_{CASE} = 90°C, nominal trim*

Typical Performance Characteristics (cont.)

The following figures present typical performance at $T_C = 25°C$, unless otherwise noted. See associated figures for general trend data.

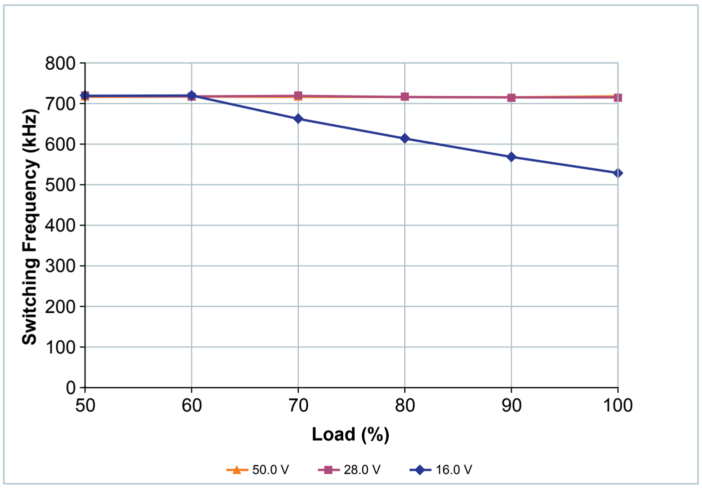


Figure 15 *— Nominal powertrain switching frequency vs. load, at nominal trim*

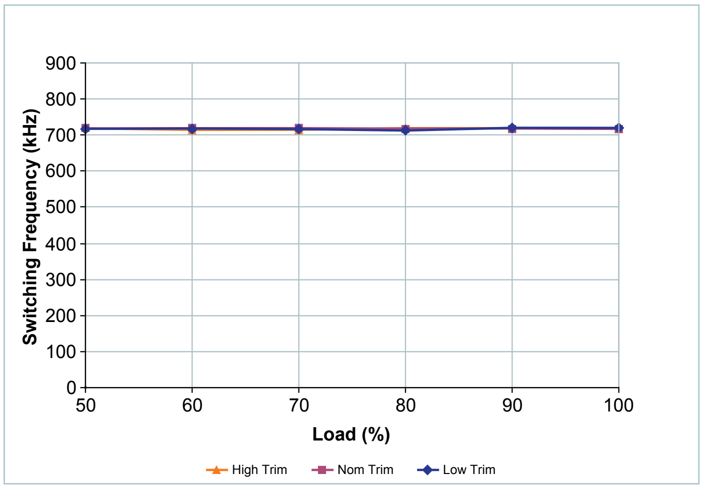


Figure 18 *— Nominal powertrain switching frequency vs. load, at nominal* V_{IN}

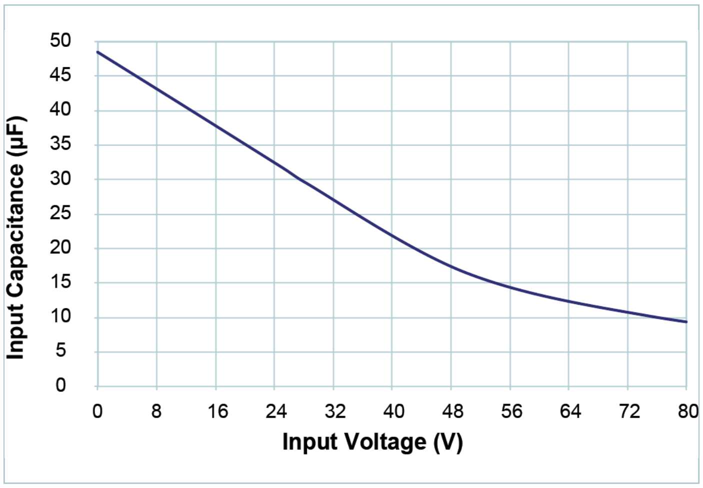


Figure 16 *— Effective internal input capacitance vs. applied voltage*

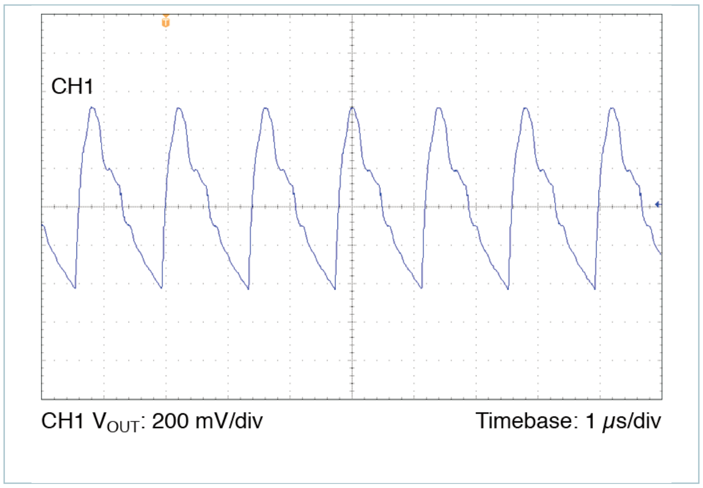


Figure 19 *— Output voltage ripple,* $V_{IN} = 28$ *V,* $V_{OUT} = 48.0$ *V,* $C_{OUT\_EXT} = 200$ *µF,* $R_{LOAD} = 7.200\ \Omega$

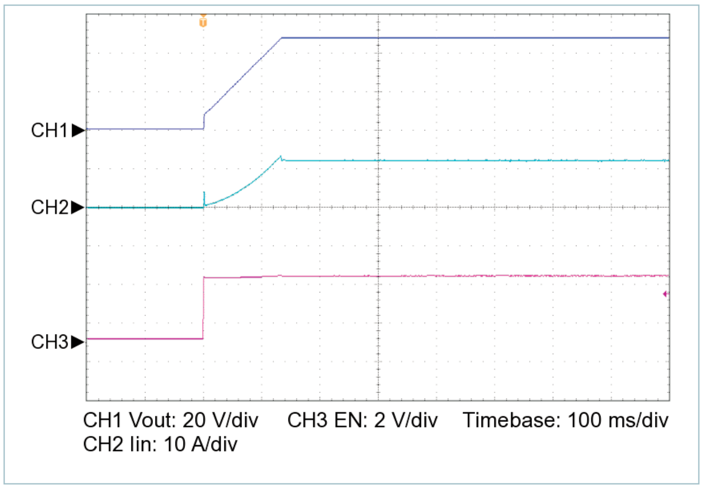


Figure 17 *—Startup from EN,* $V_{IN} = 28$ *V,* $C_{OUT\_EXT} = 2000$ *µF,* $R_{LOAD} = 7.200\ \Omega$

General Characteristics

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of -55°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
Length	L		38.13/[1.501]	38.72/[1.524]	38.89/[1.531]	mm/[in]
Width	W		22.67/[0.893]	22.8/[0.898]	22.93/[0.903]	mm/[in]
Height	H		7.21/[0.284]	7.26/[0.286]	7.31/[0.288]	mm/[in]
Volume	Vol	No heat sink		6.41/[0.39]		cm^3/[in^3]
Weight	W			24.0/[0.85]		g/[oz]
Lead finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating internal temperature	T_{INT}	M-Grade	-55		125	°C
Thermal resistance top side	$\Phi_{INT\text{-}TOP}$	Estimated thermal resistance to maximum temperature internal component from isothermal top		2.01		°C/W
Thermal resistance leads	$\Phi_{INT\text{-}LEADS}$	Estimated thermal resistance to maximum temperature internal component from isothermal leads		4.46		°C/W
Thermal resistance bottom side	$\Phi_{INT\text{-}BOTTOM}$	Estimated thermal resistance to maximum temperature internal component from isothermal bottom		2.21		°C/W
Thermal capacity				17.7		Ws/°C
Assembly						
Storage temperature	T_{ST}	M-Grade	-65		125	°C
ESD rating	HBM	Method per Human Body Model Test ESDA/JEDEC JDS-001-2012	CLASS 1C			V
	CDM	Charged Device Model JESD22-C101E	CLASS 2			
Soldering [1]						
Peak temperature top case		For further information, please contact factory applications			135	°C

[1] Product is not intended for reflow solder attach.

General Characteristics (Cont.)

Specifications apply over all line, trim and load conditions, internal temperature T_{INT} = 25°C, unless otherwise noted. **Boldface** specifications apply over the temperature range of -55°C < T_{INT} < 125°C.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Safety						
Dielectric Withstand Test	V_{HIPOT}	IN to OUT	**2250**			Vdc
		IN to CASE	**2250**			Vdc
		OUT to CASE	**707**			Vdc
Reliability						
MTBF		MIL-HDBK-217 FN2 Parts Count 25°C Ground Benign, Stationary, Indoors / Computer		3.386		MHrs
		Telcordia Issue 2, Method I Case 3, 25°C, 100% D.C., GB, GC		5.684		MHrs
Agency Approvals						
Agency approvals/standards		cTÜVus, EN 60950-1				
		cURus, UL 60950-1				
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable				

Pin Functions

+IN, -IN
Input power pins. -IN is the reference for all control pins, and therefore a Kelvin connection for the control signals is recommended as close as possible to the pin on the package, to reduce effects of voltage drop due to -IN currents.

+OUT, -OUT
Output power pins.

EN (Enable)
This pin enables and disables the DCM converter; when held low the unit will be disabled. It is referenced to the -IN pin of the converter. The EN pin has an internal pull-up to V_{CC} through a 10 kΩ resistor.

- Output enable: When EN is allowed to pull up above the enable threshold, the module will be enabled. If leaving EN floating, it is pulled up to V_{CC} and the module will be enabled.
- Output disable: EN may be pulled down externally in order to disable the module.
- EN is an input only, it does not pull low in the event of a fault.
- The EN pins of multiple units should be driven high concurrently to permit the array to start in to maximum rated load. However, the direct interconnection of multiple EN pins requires additional considerations, as discussed in the section on Array Operation.

TR (Trim)
The TR pin is used to select the trim mode and to trim the output voltage of the DCM converter. The TR pin has an internal pull-up to V_{CC} through a 10.0 kΩ resistor.

The DCM will latch trim behavior at application of V_{IN} (once V_{IN} exceeds $V_{IN\text{-}UVLO+}$), and persist in that same behavior until loss of input voltage.

- At application of V_{IN}, if TR is sampled at above $V_{TRIM\text{-}DIS}$, the module will latch in a non-trim mode, and will ignore the TR input for as long as V_{IN} is present.
- At application of V_{IN}, if TR is sampled at below $V_{TRIM\text{-}EN}$, the TR will serve as an input to control the real time output voltage, relative to full load, 25°C. It will persist in this behavior until V_{IN} is no longer present.

If trim is active when the DCM is operating, the TR pin provides dynamic trim control at a typical 30 Hz of -3dB bandwidth over the output voltage. TR also decreases the current limit threshold when trimming above $V_{OUT\text{-}NOM}$.

FT (Fault)
The FT pin provides a Fault signal.

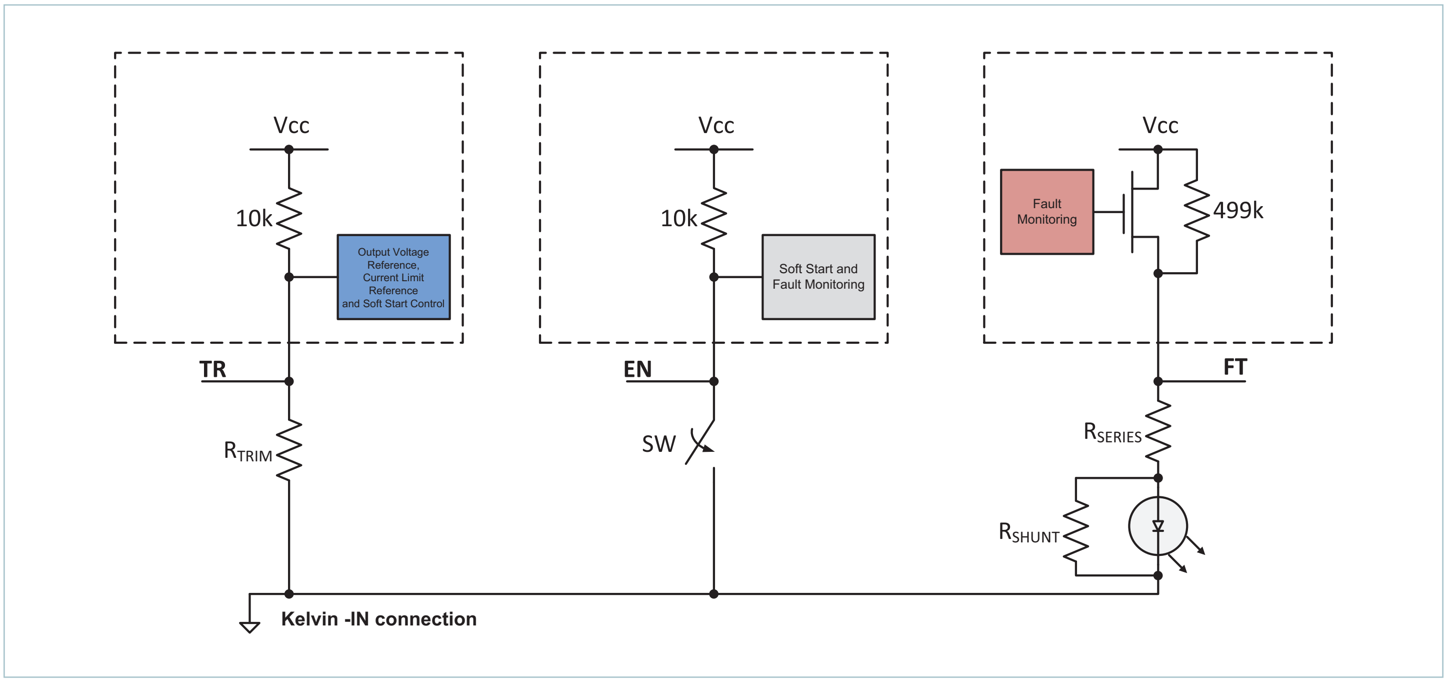
Anytime the module is enabled and has not recognized a fault, the FT pin is inactive. FT has an internal 499 kΩ pull-up to Vcc, therefore a shunt resistor, R_{SHUNT}, of approximately 50 kΩ can be used to ensure the LED is completly off when there is no fault, per the diagram below.

Whenever the powertrain stops (due to a fault protection or disabling the module by pulling EN low), the FT pin becomes active and provides current to drive an external circuit.

When active, FT pin drives to V_{CC}, with up to 4 mA of external loading. Module may be damaged from an over-current FT drive, thus a resistor in series for current limiting is recommended.

The FT pin becomes active momentarily when the module starts up.

Typical External Circuits for Signal Pins (TR, EN, FT)



Design Guidelines

Building Blocks and System Design

The DCM™ converter input accepts the full 16 to 50 V range, and it generates an isolated trimmable 48.0 Vdc output. Multiple DCMs may be paralleled for higher power capacity via wireless load sharing, even when they are operating off of different input voltage supplies.

The DCM converter provides a regulated output voltage around defined nominal load line and temperature coefficients. The load line and temperature coefficients enable configuration of an array of DCM converters which manage the output load with no share bus among modules. Downstream regulators may be used to provide tighter voltage regulation, if required.

The MDCM28AP480M320A50 may be used in standalone applications where the output power requirements are up to 320 W. However, it is easily deployed as arrays of modules to increase power handling capacity. Arrays of up to eight units have been qualified for 2560 W capacity. Application of DCM converters in an array requires no derating of the maximum available power versus what is specified for a single module.

Soft Start

When the DCM starts, it will go through a soft start. The soft start routine ramps the output voltage by modulating the internal error amplifier reference. This causes the output voltage to approximate a piecewise linear ramp. The output ramp finishes when the voltage reaches either the nominal output voltage, or the trimmed output voltage in cases where trim mode is active.

During soft-start, the maximum load current capability is reduced. Until Vout achieves at least $V_{OUT\text{-}FL\text{-}THRESH}$, the output current must be less than $I_{OUT\text{-}START}$ in order to guarantee startup. Note that this is current available to the load, above that which is required to charge the output capacitor.

Nominal Output Voltage Load Line

Throughout this document, the programmed output voltage, (either the specified nominal output voltage if trim is inactive or the trimmed output voltage if trim is active), is specified at full load, and at room temperature. The actual output voltage of the DCM is given by the programmed trimmed output voltage, with modification based on load and temperature. The nominal output voltage is 48.0 V, and the actual output voltage will match this at full load and room temperature with trim inactive.

The largest modification to the actual output voltage compared to the programmed output is due to the 5.263% $V_{OUT\text{-}NOM}$ load line, which for this model corresponds to $\Delta V_{OUT\text{-}LOAD}$ of 2.5262V. As the load is reduced, the internal error amplifier reference, and by extension the output voltage, rises in response. This load line is the primary enabler of the wireless current sharing amongst an array of DCMs.

The load line impact on the output voltage is absolute, and does not scale with programmed trim voltage.

For a given programmed output voltage, the actual output voltage versus load current at <u>for nominal trim and room temperature</u> is given by the following equation:

$$V_{OUT} @ 25° = 48.0 + 2.5262 \bullet (1 - I_{OUT} / 6.67) \qquad (1)$$

Nominal Output Voltage Temperature Coefficient

A second additive term to the programmed output voltage is based on the temperature of the module. This term permits improved thermal balancing among modules in an array, especially when the factory nominal trim point is utilized (trim mode inactive). This term is much smaller than the load line described above, representing only a -6.40 mV/°C change. Regulation coefficient is relative to 25°C.

For nominal trim and full load, the output voltage relates to the temperature according to the following equation:

$$V_{OUT\text{-}FL} = 48.0 - 6.400 \bullet 0.001 \bullet (T_{INT} - 25) \qquad (2)$$

where T_{INT} is in °C.

The impact of temperature coefficient on the output voltage is absolute, and does not scale with trim or load.

Trim Mode and Output Trim Control

When the input voltage is initially applied to a DCM, and after t_{INIT} elapses, the trim pin voltage V_{TR} is sampled. The TR pin has an internal pull up resistor to V_{CC}, so unless external circuitry pulls the pin voltage lower, it will pull up to V_{CC}. If the initially sampled trim pin voltage is higher than $V_{TRIM\text{-}DIS}$, then the DCM will disable trimming as long as the V_{IN} remains applied. In this case, for all subsequent operation the output voltage will be programmed to the nominal. This minimizes the support components required for applications that only require the nominal rated Vout, and also provides the best output setpoint accuracy, as there are no additional errors from external trim components

If at initial application of V_{IN}, the TR pin voltage is prevented from exceeding $V_{TRIM\text{-}EN}$, then the DCM will activate trim mode, and it will remain active for as long as V_{IN} is applied.

V_{OUT} set point under full load and room temperature can be calculated using the equation below:

$$V_{OUT\text{-}FL} @ 25°C = 19.95 + (37.560 \bullet V_{TR}/V_{CC}) \qquad (3)$$

Note that the trim mode is not changed when a DCM recovers from any fault condition or being disabled.

Module performance is guaranteed through output voltage trim range $V_{OUT\text{-}TRIMMING}$. If V_{OUT} is trimmed above this range, then certain combinations of line and load transient conditions may trigger the output OVP.

Overall Output Voltage Transfer Function

Taking load line (equation 1), temperature coefficient (equation 2) and trim (equation 3) into account, the general equation relating the DC V_{OUT} to programmed trim (when active), load, and temperature is given by:

$$\begin{aligned} V_{OUT} = \ & 19.95 + (37.560 \bullet V_{TR}/V_{CC}) \\ & + 2.5262 \bullet (1 - I_{OUT} / 6.67) \\ & - 6.400 \bullet 0.001 \bullet (T_{INT} - 25) + \Delta V_{OUT\text{-}LL} \end{aligned} \qquad (4)$$

Finally, note that when the load current is below 10% of the rated capacity, there is an additional ΔV which may add to the output voltage, depending on the line voltage which is related to Burst Mode. Please see the section on Burst Mode below for details.

Use 0 V for $\Delta V_{OUT\text{-}LL}$ when load is above 10% of rated load. See section on Burst Mode operation for light load effects on output voltage.

temperature fault is registered, the powertrain immediately stops switching, the output voltage of the converter falls, and the converter remains disabled for at least time t_{FAULT}. Then, the converter waits for the internal temperature to return to below $T_{INT-OTP}$ before recovering. Provided the converter is still enabled, the DCM will restart after t_{INIT} and t_{ON}.

Output Overvoltage Fault Protection (OVP)

The converter monitors the output voltage during each switching cycle by a corresponding voltage reflected to the primary side control circuitry. If the primary sensed output voltage exceeds $V_{OUT-OVP}$, the OVP fault protection is triggered. The control logic disables the powertrain, and the output voltage of the converter falls.

This type of fault is latched, and the converter will not start again until the latch is cleared. Clearing the fault latch is achieved by either disabling the converter via the EN pin, or else by removing the input power such that the input voltage falls below $V_{IN-INIT}$.

External Output Capacitance

The DCM converter internal compensation requires a minimum external output capacitor. An external capacitor in the range of 200 to 2000 µF with ESR of 10 mΩ is required, per DCM for control loop compensation purposes.

However some DCM models require an increase to the minimum external output capacitor value in certain loading and trim condition. In applications where the load can go below 10% of rated load but the output trim is held constant, the range of output capacitor required is given by $C_{OUT-EXT-TRANS}$ in the Electrical Specifications table. If the load can go below 10% of rated load and the DCM output trim is also dynamically varied, the range of output capacitor required is given by $C_{OUT-EXT-TRANS-TRIM}$ in the Electrical Specifications table.

Burst Mode

Under light load conditions, the DCM converter may operate in burst mode depending on the line voltage. Burst mode occurs whenever the internal power consumption of the converter combined with the external output load is less than the minimum power transfer per switching cycle. In order to maintain regulation, the error amplifier will switch the powertrain off and on repeatedly, to effectively lower the average switching frequency, and permit operation with no external load. During the time when the power train is off, the module internal consumption is significantly reduced, and so there is a notable reduction in no-load input power in burst mode. When the load is less than 10% of rated Iout, the output voltage may rise by a maximum of 5.05 V, above the output voltage calculated from trim, temperature, and load line conditions.

Thermal Design

Based on the safe thermal operating area shown in page 5, the full rated power of the MDCM28AP480M320A50 can be processed provided that the top, bottom, and leads are all held below 95°C. These curves highlight the benefits of dual sided thermal management, but also demonstrate the flexibility of the Vicor ChiP platform for customers who are limited to cooling only the top or the bottom surface.

The OTP sensor is located on the top side of the internal PCB structure. Therefore in order to ensure effective over-temperature fault protection, the case bottom temperature must be constrained by the thermal solution such that it does not exceed the temperature of the case top.

The ChiP package provides a high degree of flexibility in that it presents three pathways to remove heat from internal power dissipating components. Heat may be removed from the top surface, the bottom surface and the leads. The extent to which these three surfaces are cooled is a key component for determining the maximum power that is available from a ChiP, as can be seen from Figure 20.

Since the ChiP has a maximum internal temperature rating, it is necessary to estimate this internal temperature based on a real thermal solution. Given that there are three pathways to remove heat from the ChiP, it is helpful to simplify the thermal solution into a roughly equivalent circuit where power dissipation is modeled as a current source, isothermal surface temperatures are represented as voltage sources and the thermal resistances are represented as resistors. Figure 20 shows the "thermal circuit" for a 3623 ChiP DCM, in an application where both case top and case bottom, and leads are cooled. In this case, the DCM power dissipation is PD_{TOTAL} and the three surface temperatures are represented as T_{CASE_TOP}, T_{CASE_BOTTOM}, and T_{LEADS}. This thermal system can now be very easily analyzed with simple resistors, voltage sources, and a current source.

This analysis provides an estimate of heat flow through the various pathways as well as internal temperature.

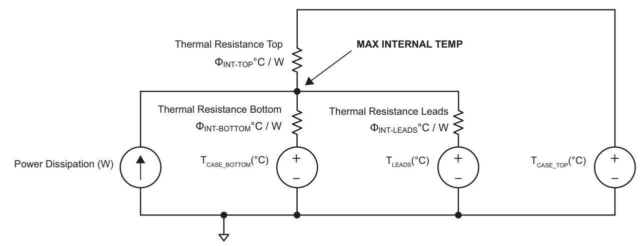


Figure 20 — *Double side cooling and leads thermal model*

Alternatively, equations can be written around this circuit and analyzed algebraically:

$$T_{INT} - PD_1 \bullet \Phi_{INT-TOP} = T_{CASE\_TOP}$$
$$T_{INT} - PD_2 \bullet \Phi_{INT-BOTTOM} = T_{CASE\_BOTTOM}$$
$$T_{INT} - PD_3 \bullet \Phi_{INT-LEADS} = T_{LEADS}$$
$$PD_{TOTAL} = PD_1 + PD_2 + PD_3$$

Where T_{INT} represents the internal temperature and PD_1, PD_2, and PD_3 represent the heat flow through the top side, bottom side, and leads respectively.

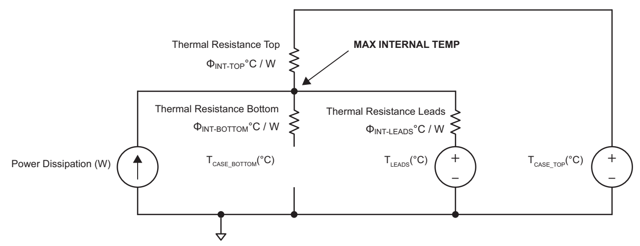


Figure 21 — *One side cooling and leads thermal model*

Figure 21 shows a scenario where there is no bottom side cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE\_TOP}$$
$$T_{INT} - PD_3 \bullet \Phi_{INT\text{-}LEADS} = T_{LEADS}$$
$$PD_{TOTAL} = PD_1 + PD_3$$

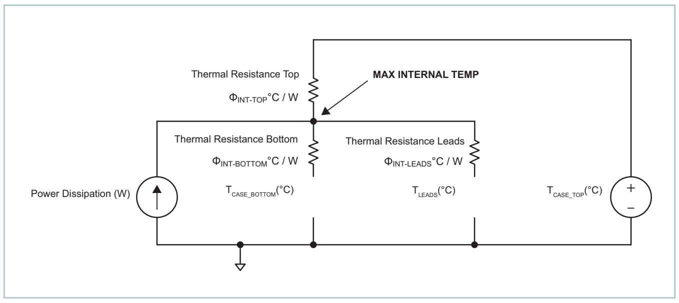


***Figure 22** — One side cooling thermal model*

Figure 22 shows a scenario where there is no bottom side and leads cooling. In this case, the heat flow path to the bottom is left open and the equations now simplify to:

$$T_{INT} - PD_1 \bullet \Phi_{INT\text{-}TOP} = T_{CASE\_TOP}$$
$$PD_{TOTAL} = PD_1$$

Vicor provides a suite of online tools, including a simulator and thermal estimator which greatly simplify the task of determining whether or not a DCM thermal configuration is sufficient for a given condition. These tools can be found at: www.vicorpower.com/powerbench.

Array Operation

A decoupling network is needed to facilitate paralleling:

- An output inductor should be added to each DCM, before the outputs are bussed together to provide decoupling.
- Each DCM needs a separate input filter, even if the multiple DCMs share the same input voltage source. These filters limit the ripple current reflected from each DCM, and also help suppress generation of beat frequency currents that can result when multiple powertrains input stages are permitted to direclty interact.

If signal pins (TR, EN, FT) are not used, they can be left floating, and DCM will work in the nominal output condition.

When common mode noise in the input side is not a concern, TR and EN can be driven and FT received using a single Kelvin connection to the shared -IN as a reference.

An example of DCM paralleling circuit is shown in Figure 23.

Recommended values to start with:
L1_x: 1 uH, minimized DCR;
R1_x: 0.3 Ω;
C1_x: Ceramic capacitors in parallel, C1 = 20 µF;
L2_x: L2 ≥ 0.15 uH;
C3_x: electrolytic or tantalum capacitor, 200 uF ≤ C3 ≤2000 uF;
C4, C5: additional ceramic /electrolytic capacitors, if needed for output ripple filtering;
In order to help sensitive signal circuits reject potential noise, additional components are recommended:
R2_x: 301 Ohm, facilitate noise attenuation for TR pin;
FB1_x, C2_x: FB1 is a ferrite bead with an impedance of at least 10 Ω at 100MHz. **C2_x** can be a ceramic capacitor of 0.1uF. Facilitate noise attenuation for EN pin.

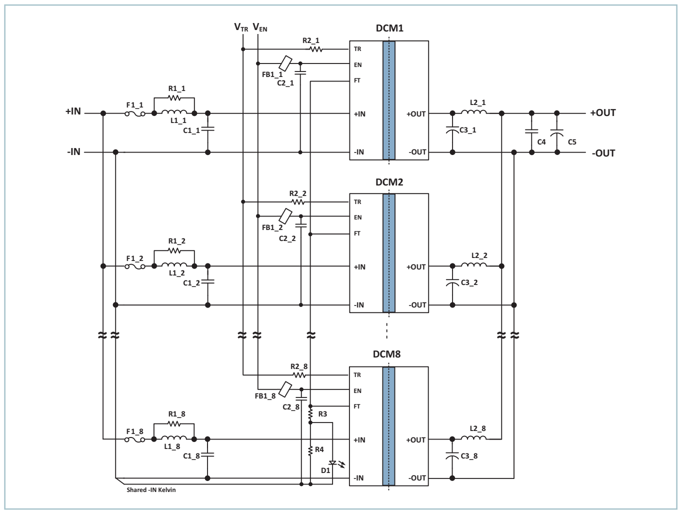


***Figure 23** — DCM paralleling configuration circuit 1*

When common mode noise rejection in the input side is needed, common modes choke can be added in the input side of each DCM. An example of DCM paralleling circuit is shown below:

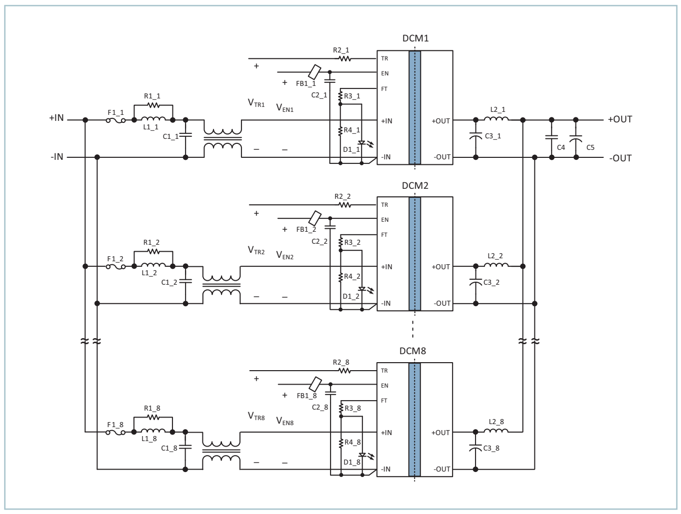


***Figure 24** — DCM paralleling configuration circuit 2*

Notice that each group of control pins need to be individually driven and isolated from the other groups control pins. This is because -IN of each DCM can be at a different voltage due to the common mode chokes. Attempting to share control pin circuitry could lead to incorrect behavior of the DCMs.

An array of DCMs used at the full array rated power may generally have one or more DCMs operating at current limit, due to sharing errors. Load sharing is functionally managed by the load line. Thermal balancing is improved by the nominal effective temperature coefficient of the output voltage setpoint.

DCMs in current limit will operate with higher output current or power than the rated levels. Therefore the following Thermal Safe Operating Area plot should be used for array use, or loads that drive the DCM in to current limit for sustained operation.

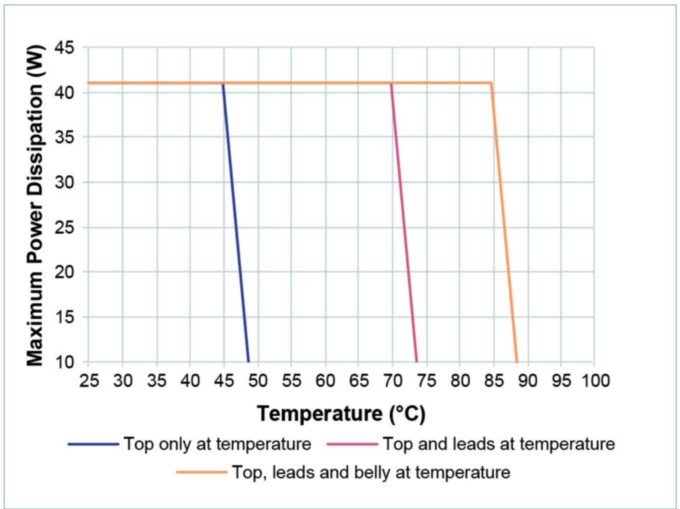
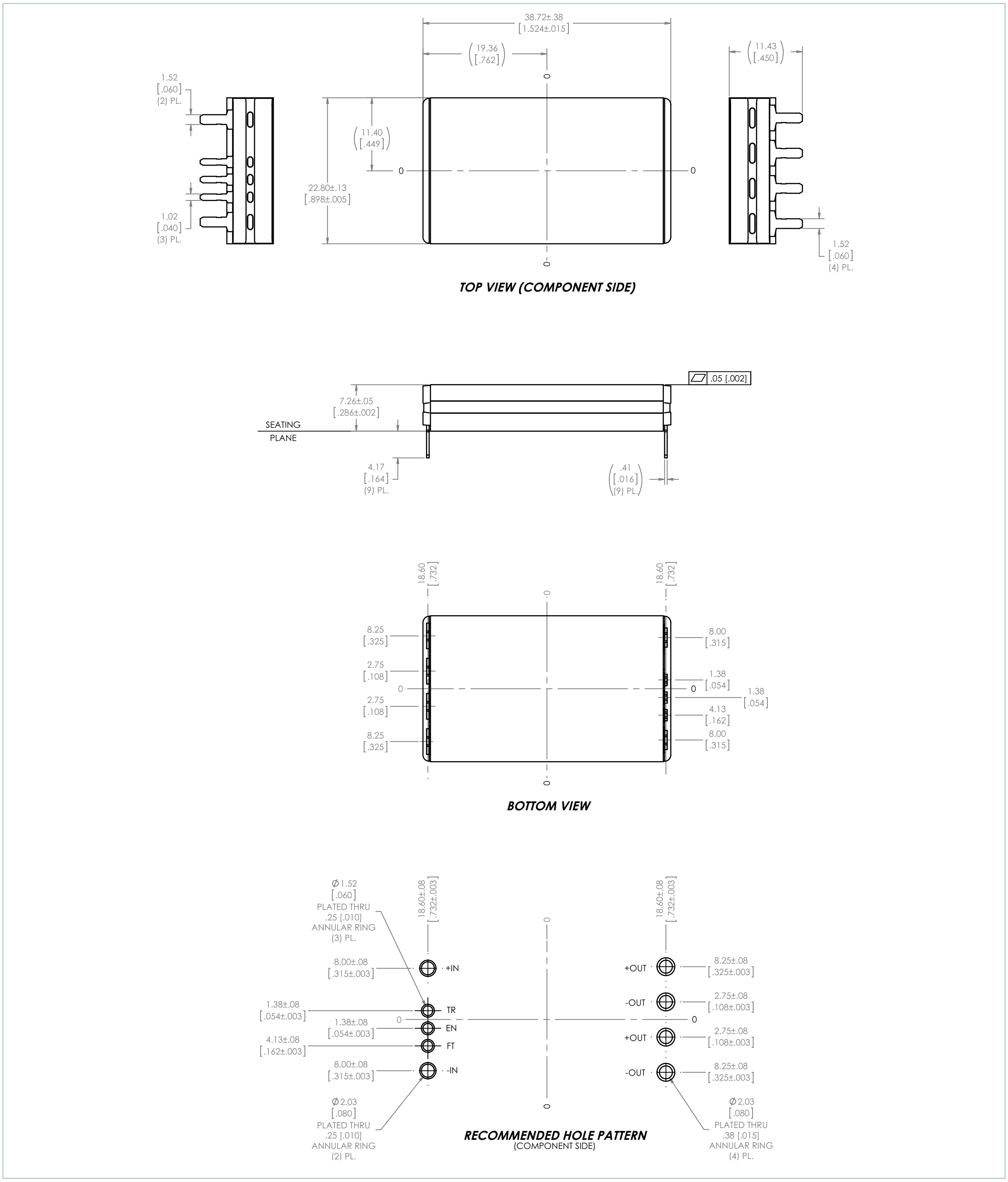


Figure 25 — *Thermal Specified Operating Area: Max Power Dissipation vs. Case Temp for arrays or current limited operation*

DCM Module Product Outline Drawing Recommended PCB Footprint and Pinout



Revision History

Revision	Date	Description	Page Number(s)
1.0	11/18/13	Intital release	n/a
1.1	01/23/15	Fig 17 MTBF hours Revision history	14 16 24
1.2	7/27/15	General updates for clarity Updated fig 2 to show rated electrical performance ABSMAX Vin-max corrected (increased) Changed Vout regulation error terms to absolute voltage FT response time replaced with max Output turn on-delay typ, and Output turn-off delay max values corrected Figure 19	All 4 4 5 6 7 14
1.3	02/09/16	Updated Part Ordering Information	4

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