TOSHIBA Field Effect Transistor Silicon N Channel MOS Type $(\pi - MOSVII)$

TK7P50D

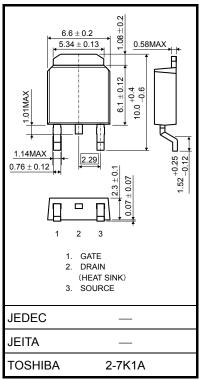
Switching Regulator Applications

Unit: mm

- Low drain-source ON-resistance: RDS (ON) = 1.0Ω (typ.)
- High forward transfer admittance: $|Y_{fs}| = 2.5 \text{ S (typ.)}$
- Low leakage current: $I_{DSS} = 10 \mu A \text{ (max) (V}_{DS} = 500 \text{ V)}$
- Enhancement-mode: $V_{th} = 2.4 \text{ to } 4.4 \text{ V (V}_{DS} = 10 \text{ V, I}_{D} = 1 \text{ mA)}$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	500	V	
Gate-source voltage		V _{GSS}	±30	V	
Drain current	DC (Note 1)	I _D	7		
	Pulse (t = 1 ms) (Note 1)	I _{DP}	28	Α	
Drain power dissipation	on (Tc = 25°C)	PD	100	W	
Single pulse avalanche energy (Note 2)		E _{AS}	105	mJ	
Avalanche current		I _{AR}	7	Α	
Repetitive avalanche energy (Note 3)		E _{AR}	10	mJ	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	



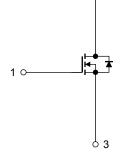
Weight: 0.36 g (typ.)

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	R _{th (ch-c)}	1.25	°C/W
Thermal resistance, channel to ambient	R _{th (ch-a)}	125	°C/W

Internal Connection



Note 1: Please use devices on conditions that the channel temperature is below $150\,^{\circ}\text{C}$.

Note 2: V_{DD} = 90 V, T_{ch} = 25°C (initial), L = 3.64 mH, R_G = 25 Ω , I_{AR} = 7 A

Note 3: Repetitive rating: pulse width limited by maximum channel temperature

This transistor is an electrostatic sensitive device. Please handle with caution.

Start of commercial production 2009-12

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TK7P50D



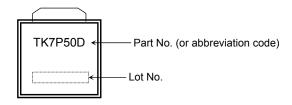
Electrical Characteristics (Ta = 25°C)

Chara	acteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Gate leakage current		I _{GSS}	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0 \text{ V}$	_	_	±1	μΑ
Drain cut-off current		I _{DSS}	V _{DS} = 500 V, V _{GS} = 0 V	_	_	10	μΑ
Drain-source brea	akdown voltage	V (BR) DSS	I _D = 10 mA, V _{GS} = 0 V	500	_	_	V
Gate threshold vo	oltage	V _{th}	V _{DS} = 10 V, I _D = 1 mA	2.4	_	4.4	V
Drain-source ON	-resistance	R _{DS} (ON)	V _{GS} = 10 V, I _D = 3.5 A	_	1.0	1.22	Ω
Forward transfer	admittance	Y _{fs}	V _{DS} = 10 V, I _D = 3.5 A	0.7	2.5	_	S
Input capacitance		C _{iss}		_	600	_	
Reverse transfer capacitance		C _{rss}	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	_	4	_	pF
Output capacitance		Coss			70	_	
Switching time	Rise time	t _r	$\begin{array}{c c} 10 \text{ V} & \text{I}_D = 3.5 \text{ A} & \text{V}_{OUT} \\ \hline \text{VGS} & \text{O} & \text{V} & \text{ERL} = \\ 50 & \text{S} & \text{V}_{DD} \approx 200 \text{ V} \\ \\ \hline \text{Duty} \leq 1\%, t_W = 10 \mu\text{s} \\ \end{array}$	_	18	_	
	Turn-on time	t _{on}			40	_	ns
	Fall time	t _f			8		
	Turn-off time	t _{off}		_	55	_	
Total gate charge		Qg		_	12	_	
Gate-source charge		Q _{gs}	$V_{DD} \approx 400 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 7 \text{ A}$	_	7	_	nC
Gate-drain charge		Q _{gd}			5		

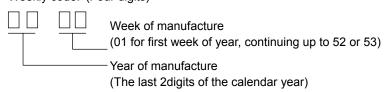
Source-Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Тур.	Max	Unit
Continuous drain reverse current (Note 1)	I _{DR}	_	_	_	7	Α
Pulse drain reverse current (Note 1)	I _{DRP}	_	_	_	28	Α
Forward voltage (diode)	V _{DSF}	I _{DR} = 7 A, V _{GS} = 0 V	_	_	-1.7	V
Reverse recovery time	t _{rr}	$I_{DR} = 7 \text{ A}, V_{GS} = 0 \text{ V},$	_	1200	_	ns
Reverse recovery charge	Q _{rr}	dI _{DR} /dt = 100 A/μs	_	7	_	μС

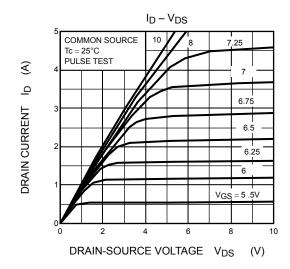
Marking (Note 4)

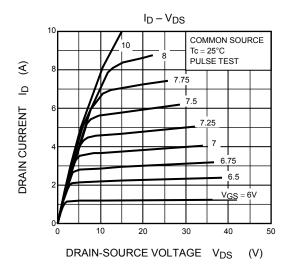


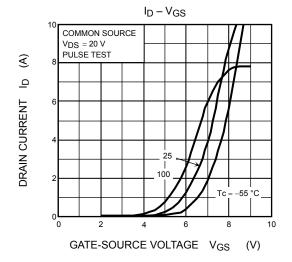
Note 4: * Weekly code: (Four digits)

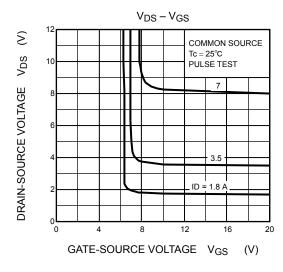


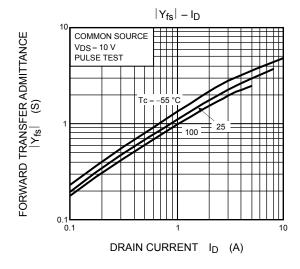
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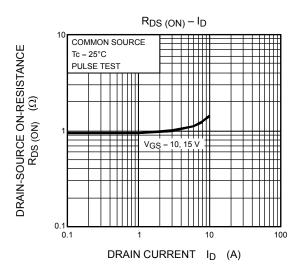




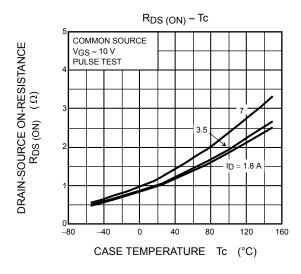


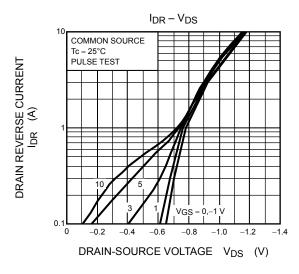


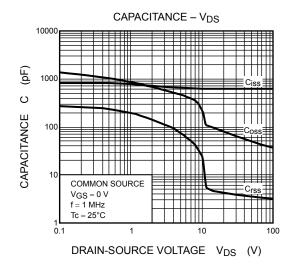


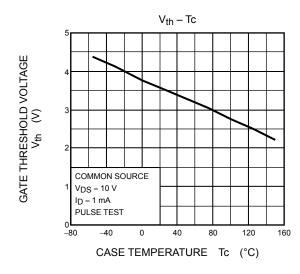


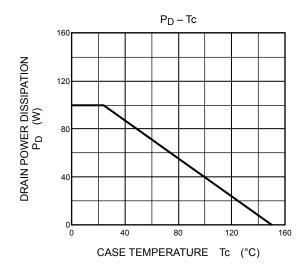
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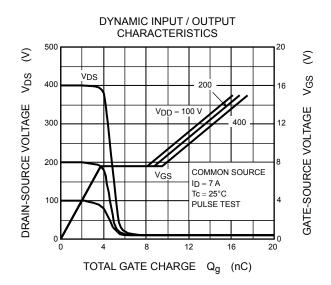


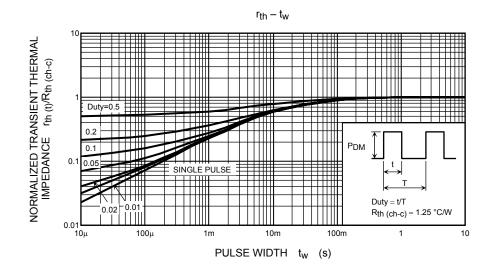


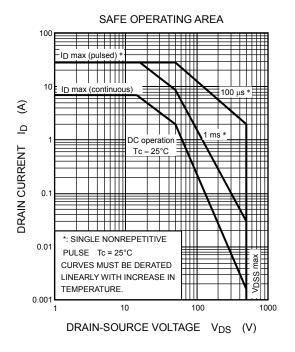


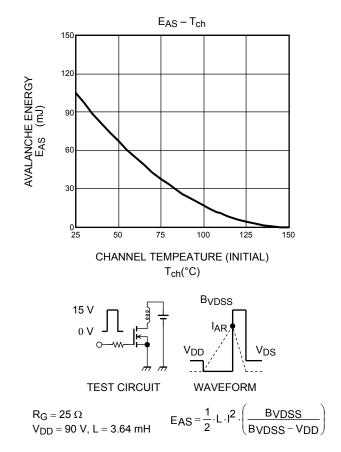












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