DATA SHEET

JUNE 1997

Revision 2.1

LXT944

Quad Ethernet Interface Adapter

General Description

The LXT944 is the first quad 10BASE-T transceiver device with integrated filters. The LXT944 Quad Ethernet Adapter is designed for IEEE 802.3 physical layer applications. This single CMOS device includes all of the active circuitry for interfacing most standard 802.3 controllers to 10BASE-T media.

The LXT944 includes four Manchester encoders/decoders, receiver squelch and transmit pulse shaping, jabber, link integrity testing and reversed polarity detection and correction per port. The LXT944 drives four independent 10BASE-T twisted-pair cables with only isolation transformers. Integrated filters simplify the design work required for FCC compliant EMI performance.

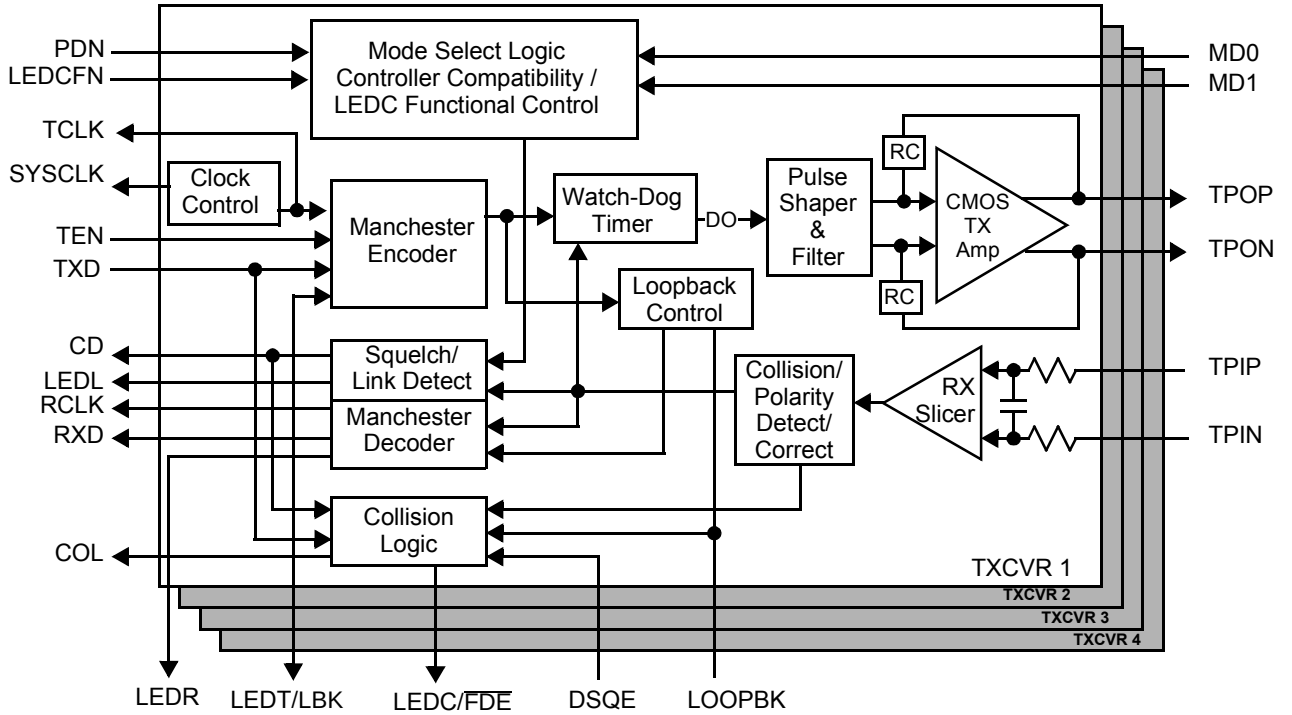
Applications

- Hub/switched Dedicated LANs for 10BASE-T
- Multi-port 10BASE-T Server products

Features

- Quad Independent 10BASE-T compliant transceivers with Integrated filters
- Quad Integrated Manchester encoder/decoder
- Power-down mode with tri-stated outputs
- Automatic Polarity Detection & Correction
- Global SQE enable/disable
- Four LED drivers per port
- Full duplex capability per port
- External Loopback with port disable
- Available in 100-pin Plastic Quad Flat Pack

LXT944 Block Diagram



LEVEL ONE

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PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: LXT944 Pin Assignments

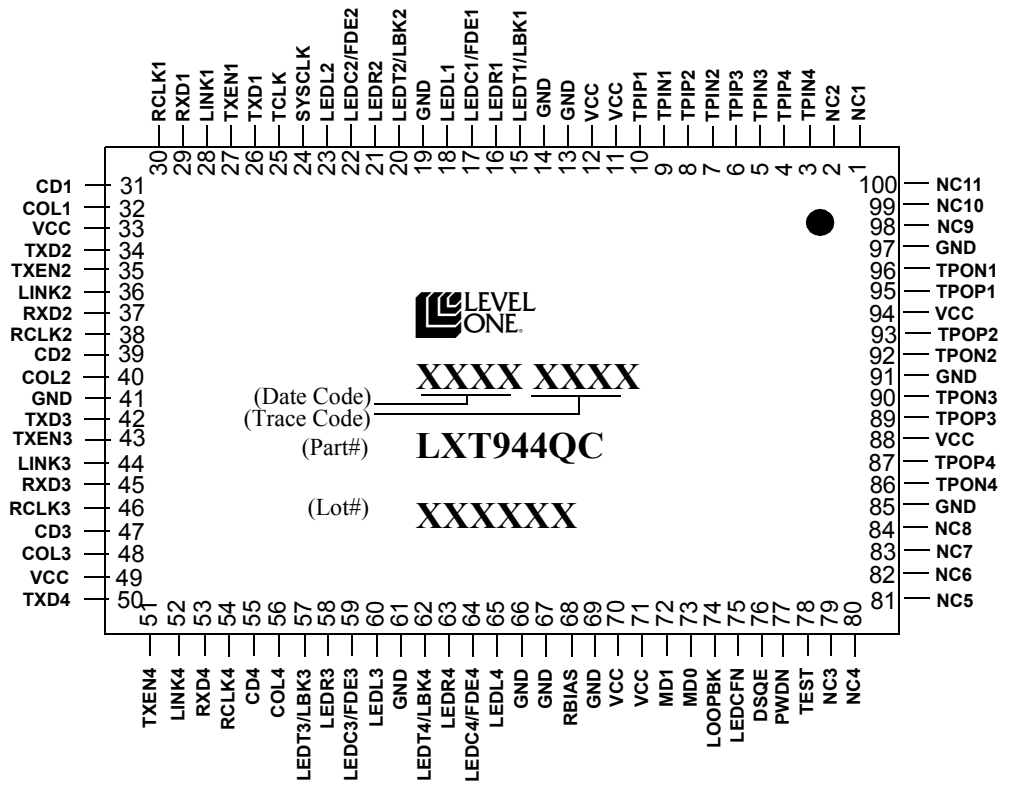


Table 1: Twisted-Pair Interface Signal Descriptions

Pin	Symbol	I/O	Description
10	TPIP1	I	**Twisted Pair Data Inputs, Positive & Negative (ports 1–4).** These pins are the positive (TPIP) and negative (TPIN), twisted-pair data input pins for ports 1 - 4, respectively.
9	TPIN1	I	
8	TPIP2	I	
7	TPIN2	I	
6	TPIP3	I	
5	TPIN3	I	
4	TPIP4	I	
3	TPIN4	I	
95	TPOP1	O	**Twisted Pair Data Outputs, Positive & Negative (ports 1–4).** These pins are the positive (TPOP) and negative (TPON), twisted-pair data output pins for ports 1 - 4, respectively. The outputs are pre-equalized; no external filters are required.
96	TPON1	O	
93	TPOP2	O	
92	TPON2	O	
89	TPOP3	O	
90	TPON3	O	
87	TPOP4	O	
86	TPON4	O	

Table 2: MAC Interface Signal Descriptions

Pin	Symbol	I/O	Description
27 35 43 51	TXEN1 TXEN2 TXEN3 TXEN4	I I I I	**Transmit Enable (ports 1–4).** These pins enable data transmission from the respective controller and start the watch dog timers. The signals are synchronous to TCLK. Pulled Low internally.
26 34 42 50	TXD1 TXD2 TXD3 TXD4	I I I I	**Transmit Data (ports 1–4).** These pins are input signals containing NRZ data to be transmitted on the network. The TXD pins should be tied directly to the data output of the respective controller. Pulled Low internally.
25	TCLK ***(global)***	O	**Transmit Clock.** 10 MHz clock output. This clock signal should be directly connected to the transmit clock input of each controller.
29 37 45 53	RXD1 RXD2 RXD3 RXD4	O O O O	**Receive Data (ports 1–4).** These are the output signals and should be connected directly to the data input of the respective controller.
30 38 46 54	RCLK1 RCLK2 RCLK3 RCLK4	O O O O	**Receive Clock (ports 1–4).** These pins provide recovered 10MHz clocks which are synchronous to the receive data from the respective port. These pins should be connected to the receive clock input of the respective controller.
31 39 47 55	CD1 CD2 CD3 CD4	O O O O	**Carrier Detect (ports 1–4).** Outputs for notifying the controller that activity exists on the respective network.
32 40 48 56	COL1 COL2 COL3 COL4	O O O O	**Collision Detect (ports 1–4).** Outputs for driving the respective collision detect inputs of the controller. COL1 - COL4 also carry signal quality error (SQE) signals.

Table 3: Control Signal Descriptions

Pin	Symbol	I/O	Description
73 72	MD0 MD1 ***(global)***	I	**Mode Select 0 (MD0), Mode Select 1 (MD1).** These pins determine the controller compatibility mode as specified in Table 7. Default is mode 3.
74	LOOPBK ***(global)***	I	**Global Loopback.** When Low, all ports are forced to internal loopback, disabling collision and the transmission of both data and link pulses. When High, the loopback function is controlled on a per port basis using LEDT1 - 4/LBK1 - 4.
76	DSQE ***(global)***	I	**SQE Disable.** When this pin is pulled High, the SQE function is disabled. When this pin is driven Low or floated, the SQE function is enabled. This pin controls the SQE function for all four TP ports.
77	PWDN ***(global)***	I	**Power Down.** When driven High the LXT944 enters power down state with all outputs tri–stated. When Low the LXT944 is in operational mode.

Table 4: Status Indication Signal Descriptions

Pin	Symbol	I/O	Description
28 36 44 52	LINK1 LINK2 LINK3 LINK4	O O O O	**Link Status (ports 1–4).** These four signals indicate link status for each port: Low = link test pass. High = link test fail. The link status is valid for both half and full duplex modes.
75	LEDCFN ***(global)***	I	**LEDC Function Select.** When driven Low or floated, the LEDC1–4/FDE1–4 pins are bidirectional. When driven High the LEDC1–4/FDE1–4 pins are TTL inputs only.
17 22 59 64	LEDC1/FDE1 LEDC2/FDE2 LEDC3/FDE3 LEDC4/FDE4	I/O I/O I/O I/O	**Collision LED drivers (ports 1–4).** Open drain drivers for the collision indicators. The output is pulled Low and the pulse is extended for 100ms to indicate collision. **Full Duplex Enable (ports 1–4).** If Externally tied Low, the respective port is forced into Full Duplex Mode. These pins are internally pulled up.
15 20 57 62	LEDT1/LBK1 LEDT2/LBK2 LEDT3/LBK3 LEDT4/LBK4	I/O I/O I/O I/O	**Transmit LED drivers (ports 1–4).** Open drain drivers for the transmit indicators. The output is pulled Low and the pulse is extended for 100 ms to indicate transmit activity. **Loopback (ports 1–4).** If Externally tied Low, the respective port is forced to Internal Loopback, disabling collision detection and the transmission of both data and link pulses. See LOOPBK pin 74. These pins are internally pulled up.
16 21 58 63	LEDR1 LEDR2 LEDR3 LEDR4	O O O O	**Receive LED drivers (ports 1–4).** Open drain drivers for the receive indicators. The output is pulled Low and the pulse is extended for 100 ms to indicate receive activity.
18 23 60 65	LEDL1 LEDL2 LEDL3 LEDL4	O O O O	**Link LED drivers (ports 1–4).** These tri–level LED drivers indicate Link status for each port. The outputs are pulled Low to indicate half duplex link pass state. The outputs are driven High to indicate full duplex link pass state. When in link fail state the driver is tri–stated.

Table 5: Miscellaneous Signal Descriptions

78	TEST	I	**Test.** Factory use only. This pin must be tied to **ground**.
24	SYSCLK	I	**System Clock.** A 20 MHz clock input is required at this pin.
1 2 79 80 81 82 83 84 98 99 100	NC1 NC2 NC3 NC4 NC5 NC6 NC7 NC8 NC9 NC10 NC11	– – – – – – – – – – –	**No Connects.** These pins must be left unconnected.

Table 6: Power and Ground Signal Descriptions

Pin	Symbol	I/O	Description
11 12 33 49 70 71 88 94	VCC	–	**Power Input.** These pins are to be connected to the power supply (**+5 volts**)
13 14 19 41 61 66 67 69 85 91 97	GND	–	**Ground.** These pins are to be connected to the **ground** plane.
68	RBIAS	I	**Bias.** Bias current for internal circuitry. This pin should be connected to ground through an external **7.5 kΩ 1%** resistor.

FUNCTIONAL DESCRIPTION

Introduction

The LXT944 Quad Ethernet Transceiver performs the physical layer signaling (PLS) and Media Attachment Unit (MAU) functions as defined by the IEEE 802.3 specification. It functions as an integrated PLS/MAU for use with four 10BASE-T twisted-pair networks.

The LXT944 interfaces between the Media Access Controller (four singles or one Quad MAC) and four twisted-pair (TP) cables. The MAC interface includes transmit and receive clock and NRZ data channels, as well as mode control logic and signaling. The twisted-pair interfaces include Twisted-Pair Input (TPI±) and Twisted-Pair Output (TPO±) pairs. In addition to the two basic interfaces, the LXT944 has a 20 MHz system clock input; a single 10 MHz TCLK output to all four controllers; LED drivers for Collision, Receive, Transmit, and Link Status of each port; independent or global internal loopback; full duplex operation on a per port basis; and four TTL link status outputs.

LXT944 functions are defined from the back end controller side of the interface. The LXT944 Transmit function refers to data transmitted by the back end controllers to the twisted-pair network. The LXT944 receive function refers to the data received by the back end controllers from the twisted-pair networks. The LXT944 performs all required MAU functions defined by the IEEE 802.3 10BASE-T specification such as collision detection, link integrity testing, signal quality error messaging, jabber control and loopback.

Controller Compatibility Modes

The LXT944 is compatible with most industry standard controllers including devices produced by Advanced Micro Devices (AMD), Fujitsu, Intel, Motorola, National Semiconductor, Seeq and Texas Instruments.

NOTE

Refer to Level One Application Note 51 when designing with Intel controllers. Note that Seeq controllers require inverters on the following signals: SYSCLK, LBK1-4, RCLK1-4 and COL1-4.

Four different control signal timing and polarity schemes (modes 1 through 4) are required to achieve this compatibility. The Mode select pins (MD1 & MD0) determine the controller compatibility mode as listed in Table 7. Controller compatibility mode is selected globally. Each of the four independent controller inputs (one per port) is configured to operate in the same mode. The user must select a single controller operating mode for all four ports. Refer to the Test Specification section for the timing parameters.

Transmit Function

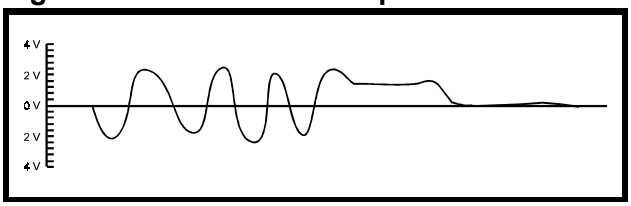
The LXT944 receives NRZ data from the controller at the TXD input (as shown in the block diagram on the first page of the data sheet) and passes it through a Manchester encoder. The encoder data is then transferred to the twisted-pair network (the four TPO circuits). The advanced integrated pulse shaping and filtering network produces the output signal on TPON*x* and TPOP*x*, shown in Figure 2. The TPO output is pre-distorted and pre-filtered to meet the 10BASE-T jitter template. An internal, continuous, resistor-capacitor filter removes high frequency clocking noise from the pulse shaping circuitry. Integrated filters simplify the design work required for FCC compliant EMI performance. During idle periods the LXT944 transmits link integrity test pulses on the TPO*x* circuits (if the Loopback function is disabled).

Table 7: Controller Compatibility Modes

Ethernet Controllers Supported	Mode	MD1	MD0
Advanced Micro Devices AM7990, Motorola 68EN360, MPC860 and compatible controllers	Mode 1	Low	Low
Intel 82596 and compatible controllers[1]	Mode 2	Low	High
Fujitsu MB86950, MB86960, Seeq 8005, and compatible controllers[2]	Mode 3	High	Low
National Semiconductor 8390, Texas Instruments TMS380C26, and compatible controllers	Mode 4	High	High

1. Refer to Level One Application Note 51 when designing with Intel controllers.
2. Seeq controllers require inverters on CLKI, LBK, RCLK and COL.

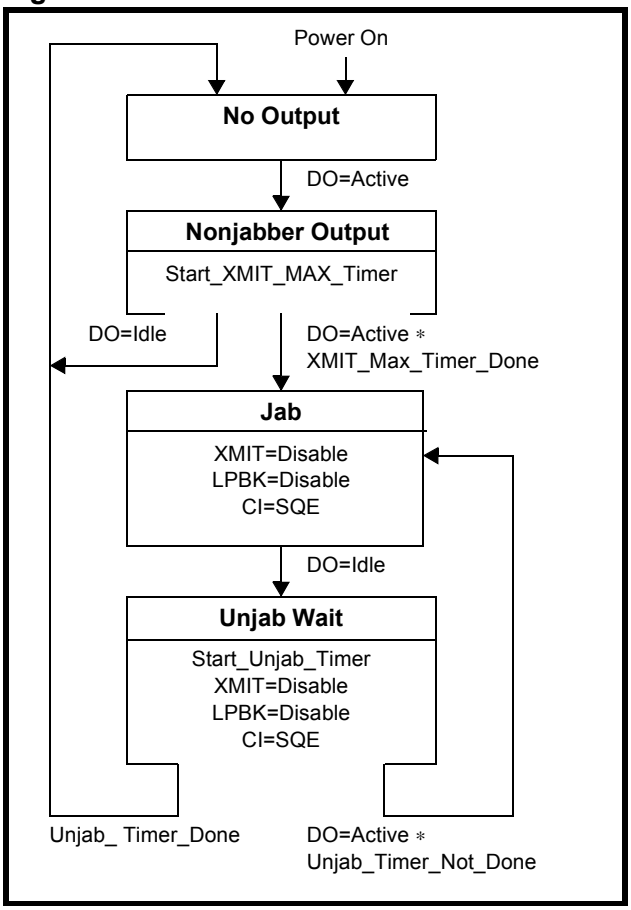
Figure 2: LXT944 TPO Output Waveform



Jabber Control Function

Figure 3 is a state diagram of the LXT944 jabber control function per port. The LXT944 on-chip watchdog timer prevents the DTE from locking into a continuous transmit mode. When a transmission exceeds the time limit, the watchdog timer disables the transmit and loopback functions and activates the COL*x* pins. Once the LXT944 is in jabber state, the TXD circuit must remain idle for a period of 0.25 to 0.75 seconds before it will exit the jabber state.

Figure 3: LXT944 Jabber Control Function

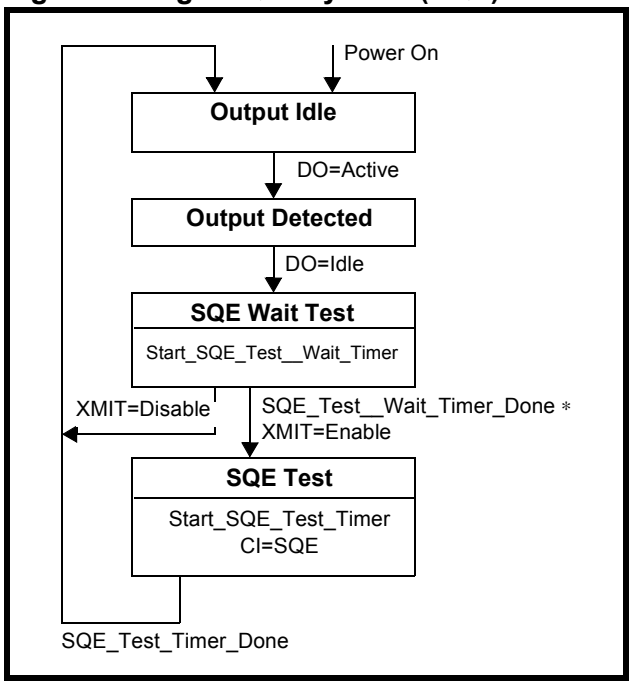


SQE Function

The LXT944 supports the Signal Quality Error (SQE) function as shown in Figure 4. After every successful transmission on the 10BASE-T network, the LXT944 transmits the SQE signal for 10 bit times (BT) ±5 BT on the COL*x* pins of the device.

The SQE function can be disabled for repeater or switch applications. When the DSQE pin = High, the SQE function is disabled. When DSQE = Low, the SQE function is enabled. The pin has an internal pull down enabling the SQE function when unconnected.

Figure 4: Signal Quality Error (SQE) Function



Receive Function

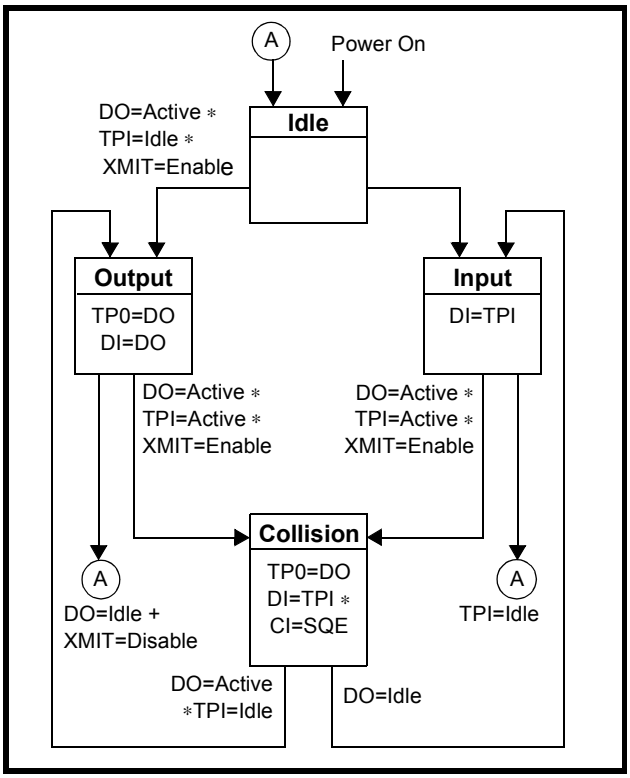
The LXT944 receive function acquires timing and data from the twisted-pair network (the TPI*x* circuits). Valid receive signals are passed through the on-chip filters and Manchester decoder then output as decoded NRZ data receive timing on the RXD RCLK pins, respectively.

An internal RC filter and an intelligent squelch function discriminates noise from link test pulses and valid data streams. The receive function is activated only by valid data streams above the squelch level and with proper timing. If the differential signals at the TPI*x* circuit inputs fall below 85% of the threshold level (unsquelched) for 8 bit times (typical), the LXT944 receive function enters the idle state. The LXT944 automatically corrects reversed polarity on the TPI*x* circuits.

Collision Detection Function

A collision is defined as the simultaneous presence of valid signals on both the TPI*x* circuits and the TPO*ix* circuits. The LXT944 reports collisions to the back-end via the COL*x* pins. If the TPI*x* circuits become active while there is activity on the TPO*x* circuits, the TPI*x* data is passed to the back-end over the RXD circuit, disabling normal loopback. Figure 5 is a state diagram of the LXT944 collision detection function per port.

Figure 5: LXT944 Collision Detection State Machine



Polarity Reverse Function

The LXT944 supports auto polarity detection and correction. The polarity reverse function uses both the link pulses and the end-of-frame data to determine polarity of the received signal. A reversed polarity condition is detected when eight consecutive opposite receive link pulses are detected without receipt of a link pulse of the expected polarity. Reversed polarity is also detected if four consecutive frames are received with a reversed start-of-idle. Whenever a corrected polarity frame is received, these two counters are reset to zero. If the LXT944 enters the link fail state and no valid data or link pulses are received within 96 to 128 ms, the polarity is reset to the default non-flipped condition. (If Link Integrity testing is disabled, polarity detection is based only on receive data.) Polarity correction is always enabled.

Loopback Function

The LXT944 provides the normal loopback function specified by the 10BASE-T standard for the twisted-pair port, as well as a forced loopback function. The loopback function operates in conjunction with the transmit function. Data transmitted by the back-end is internally looped back within the LXT944 from the TXD*x* pins through the Manchester encoder/decoder to the RXD1-4 pins and returned to the back-end. This "normal" loopback function is disabled when a data collision occurs, clearing the RXD*x* circuits for the TPI*x* data. Normal loopback is also disabled during link fail, jabber, and full duplex states. Loopback is always enabled during the forced loopback state.

The LXT944 provides an additional loopback function. **External loopback mode**, useful for system-level testing, is controlled by the LEDC*x*/FDE*x* pins. With both LEDC*x*/FDE*x*, and LEDT*x*/LBK*x*, or the global Loopback pins Low, the LXT944 device:

- disables internal loopback circuits
- disables SQE
- disables the collision detection circuitry
- enables full duplex mode

This allows for external loopback testing. This can be controlled on a per port basis using the individual port controls or globally by using the "Loopback" pin.

Full Duplex Operation

Full duplex operation is enabled by driving the LEDC*x*/FDE*x* pins with an open collector driver. The LEDCFN pin when enabled will disable the collision LED driver and allow the LEDC*x*/FDE*x* pin to be driven by a TTL driver to enable or disable the full duplex operation of the TP ports.

LED Driver Functions

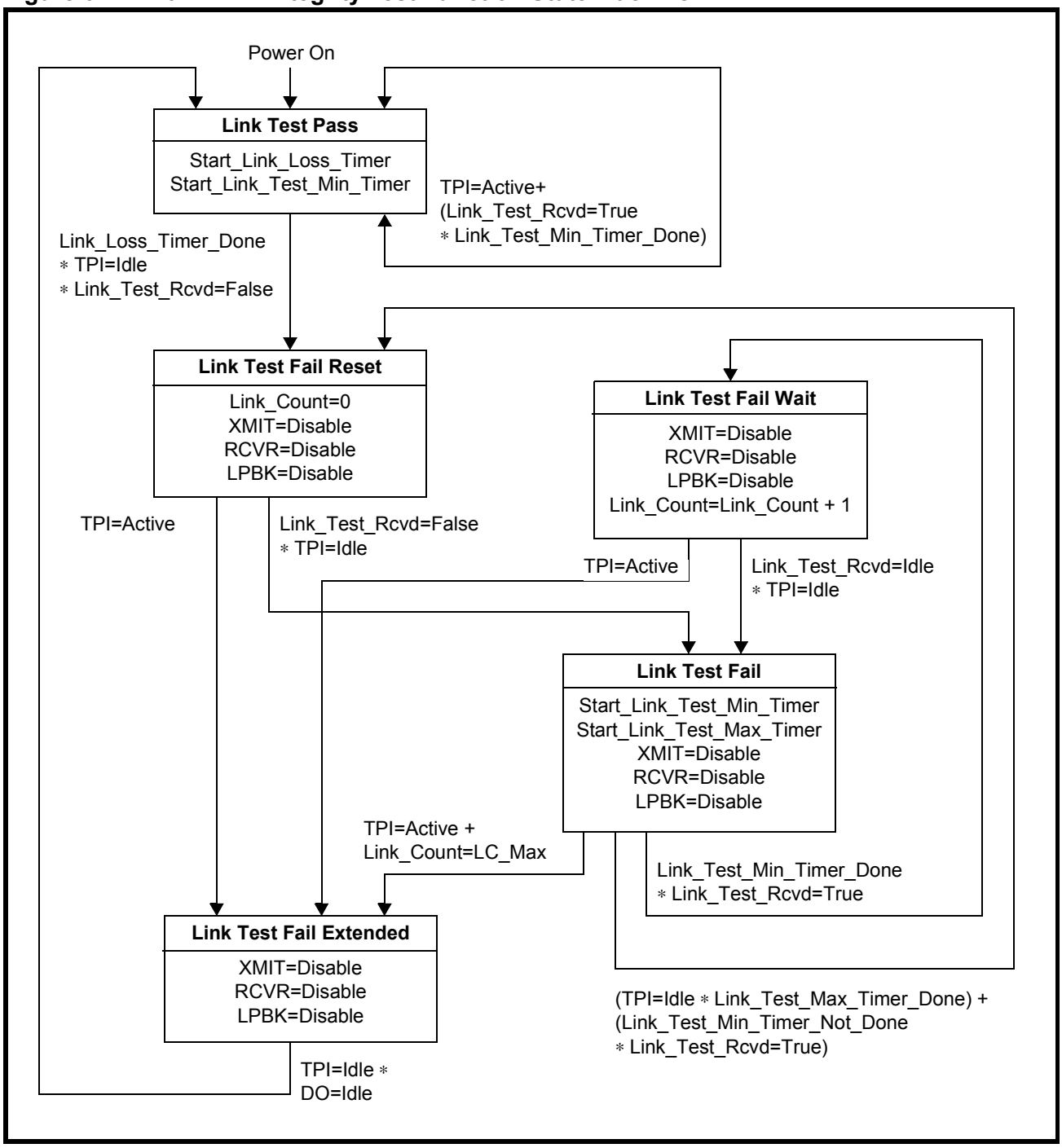
The LXT944 supports individual LED drivers for each port. Per-port LED drivers include link (both half & full duplex), receive, transmit, and collision. The signal pulse widths on all activity outputs (receive, transmit, and collision) are a minimum of a 100 ms to increase visual recognition of the LED status.

The LINK*x* signals are TTL level outputs indicating link pass state for both half and full duplex operation. The signal is active Low and can be read as a status bit or be used to activate port link LEDs.

Link Integrity Test Function

Figure 6 is a state diagram of the LXT944 Link Integrity Test function. The link integrity test is used to determine the status of the receive side twisted-pair cable. Link integrity testing is always enabled unless the loopback function is enabled (LBK or Loopback = High). When enabled, the receiver recognizes link integrity pulses which are transmitted in the absence of receive traffic. If no serial data stream or link integrity pulses are detected within 50-150 ms, the device enters a link fail state and disables the transmit and normal loopback functions. The LXT944 ignores any link integrity pulse with an interval less than 2-7 ms. The LXT944 will remain in the Link Fail state until it detects either a serial data packet or two or more link integrity pulses.

Figure 6: LXT944 Link Integrity Test Function State Machine



APPLICATION INFORMATION

The following diagrams group similar pins; they do not portray the actual chip pinout. The controller interface pins (transmit, data, clock, and enable; receive data and clock; and the collision detect and carrier detect pins) are at the upper left.

The VCC and GND pins are at the bottom of each diagram. All VCC pins use a single power supply with decoupling capacitors installed between the VCC and GND pins and their respective planes.

Magnetics Information

The LXT944 requires a 1:1 ratio for the receive transformers and a 1:$\sqrt{2}$ ratio for the transmit transformers. The LXT944 uses the same magnetics which are currently used on the LXT914 Quad Repeater. Various front end design options are available: a simple per port Rx/Tx pair configuration (see Figure 7), the receive quad and the transmit quad (see Figure 8), and the new single 40 pin octal transformer configuration (see Figure 9).

Transformers for these designs are available from various manufacturers (see Table 8) is a list of available Quad and Single port transformers with manufacturers and their part numbers. Before committing to a specific component, designers should test and validate all specifications of the magnetics used in all applications.

Table 8: Magnetics Manufacturers

Mfgr.	Quad Tx	Quad Rx	Tx/Rx Pairs
Bell Fuse	S553-5999-02	S553-5999-03	
Fil-Mag	23Z339	23Z338	
HALO	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TD42-2006Q TD43-2006K TG42-1406N1 TG43-1406N
(Octal)			TG44-S010NX
Kappa	TP4003P	TP497P101	
Nan-opulse	5976	5977	
PCA	EPE6009	EPE6010	
VALOR	PT4116	PT4117	PT4069N1 PT4068N1 ST7011S2 ST7010S2

Layout Requirements

The Twisted-Pair Interface

The four, twisted-pair output circuits are identical. Each TPDOP/TDPON signal has a 24.9 Ω, 1%, series resistor and a 120 pF capacitor differentially across the positive and negative outputs. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TPDIN signals have a 100 Ω resistor across the positive and negative input signals to terminate the 100 Ω signal received from the line. To calculate the impedance on the output line interface, use:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

The layout of the twisted-pair ports is critical in complex designs. Run the signals directly from the device to the discrete termination components (located close to the transformers).

The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side. Careful planning during the schematic and layout stages can avoid these problems.

The PCB layout should have no ground or power planes between the transformers and the connectors. The data signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield with the chassis.

The RBIAS Pin

The RBIAS signal sets the levels for the output drivers of the LXT944. Any emissions or common mode noise entering the device here could be measured on the twisted-pair output signals.

The LXT944 requires a 7.5 kΩ, 1% resistor directly connected between pin 68 and ground. These traces should be as short as possible. The ground signals from pins 67 & 69 should come directly off of the device to enclose the resistor and pin forming a shielded area between the RBIAS connection and the switching signals on the PCB.

Figure 7: Simple Receive/Transmit on Each Port Application

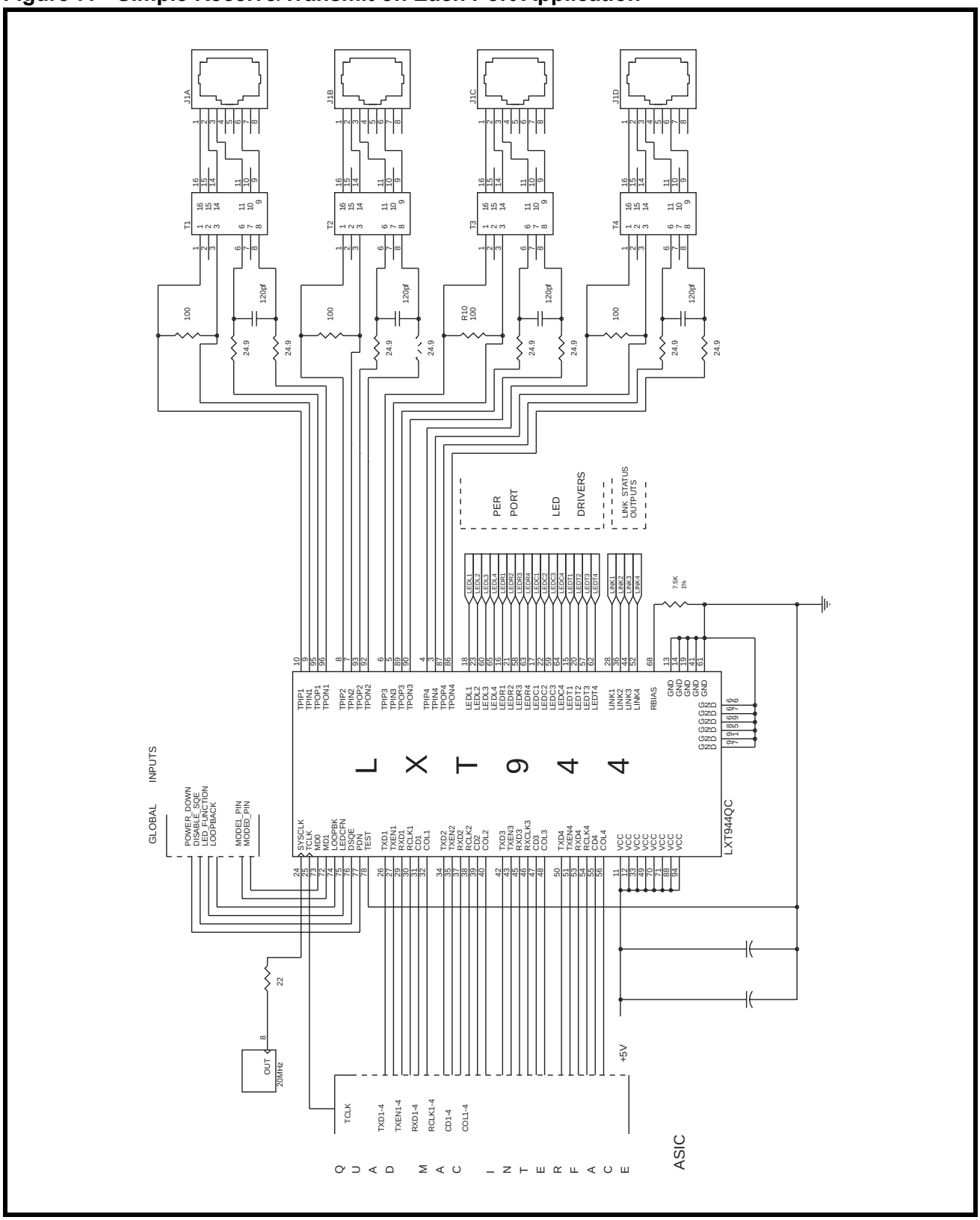


Figure 8: Receive Quad and Transmit Quad Application

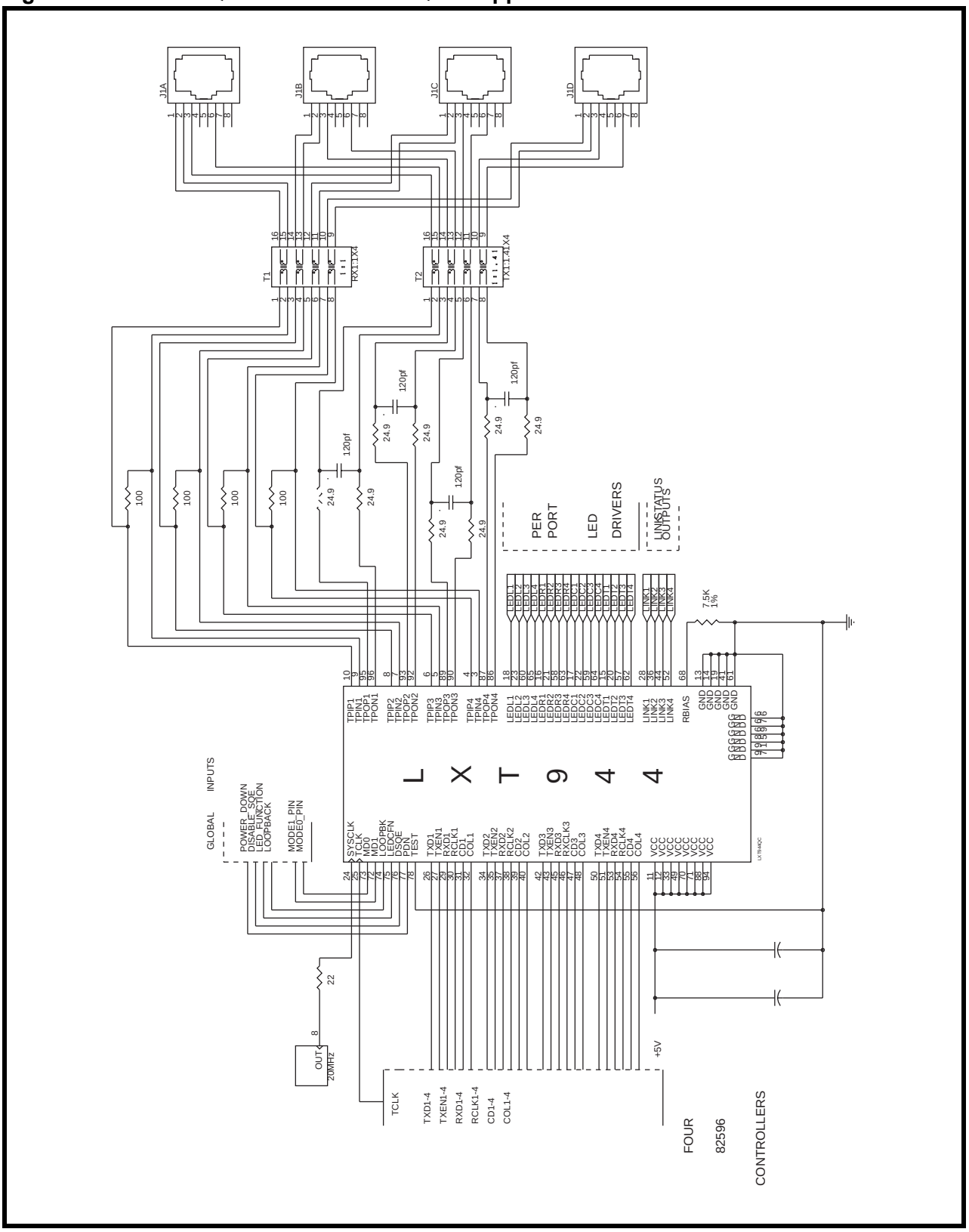
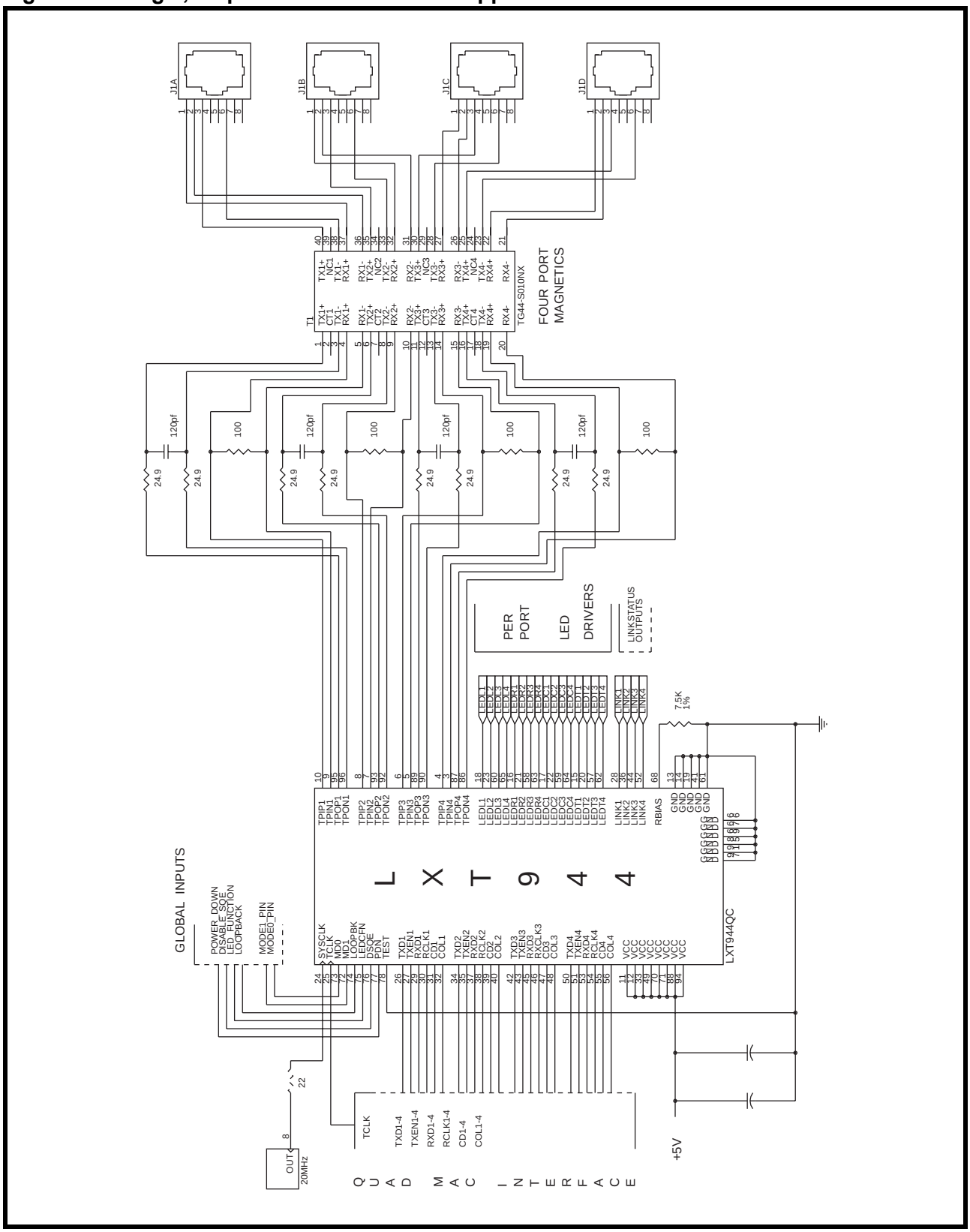


Figure 9: Single, 40-pin Octal Transformer Application



TEST SPECIFICATIONS

NOTE

The minimum and maximum values in Tables 9 through 17 and Figures 10 through 25 represent the performance specifications of the LXT944 and are guaranteed by test, except where noted by design

Table 9: Absolute Maximum Values

Parameter	Symbol	Min	Max	Units
Supply Voltage	VCC	-0.3	6	V
Operating Temperature	TOP	0	70	ºC
Storage Temperature	TST	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 10: Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Recommended Supply Voltage[1]	VCC	4.75	5.0	5.25	V	
Recommended Operating Temperature	TOP	0	-	70	ºC	

1. Voltages with respect to ground unless otherwise specified.

Table 11: I/O Electrical Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage		VIL	–	–	0.8	V	
Input High voltage		VIH	2.0	–	–	V	
Output Low voltage		VOL	–	–	0.4	V	IOL = 1.6 mA
		VOL	–	–	10	%VCC	IOL < 10 µA
Output Low voltage - LEDs		VOLL	–	–	1.0	%VCC	IOLL = 5 mA
Output High voltage		VOH	2.4	–	–	V	IOH = 40 µA
		VOH	90	–	–	%VCC	IOH < 10 µA
Output High voltage - LEDs		VOHL	2.4	–	–	V	IOHL = -5 mA
Input Low current		IIL	–	–	2	mA	VOL = .4 V
Output Rise Time	CMOS	-	-	3	15	ns	CLOAD = 20 pF
TCLK & RCLK	TTL	-	-	2	15	ns	
Output Fall Time	CMOS	-	-	3	15	ns	CLOAD= 20 pF
TCLK & RCLK	TTL	-	-	2	15	ns	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 11: I/O Electrical Characteristics (Over Recommended Range) – continued

Parameter		Sym	Min	Typ[1]	Max	Units	Test Conditions
CLKI rise time (externally driven)		-	-	-	10	ns	
CLKI duty cycle (externally driven)		-	-	50/50	40/60	%	
Supply Current	Normal Mode	ICC	0	140	200	mA	Idle
	Normal Mode	ICC	0	180	220	mA	Transmitting on TP
	Power Down Mode	ICC	-	0.1	100	µA	

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 12: Twisted-Pair Electrical Characteristics (Over Recommended Range)

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmit output impedance	ZOUT	–	2	–	Ω	
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receive input impedance	ZIN	–	24	–	kΩ	Between TPIP/TPIN
Differential Squelch Threshold	VDS	300	420	585	mV	5 MHz square wave input

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Guaranteed by design; not subject to production testing.
3. IEEE 802.3 specifies maximum jitter additions at 0.5 ns from the encoder and 3.5 ns from the MAU.

Table 13: Switching Characteristics (Over Recommended Range)

Parameter		Sym	Min	Typ[1]	Max	Units
Jabber Timing	Maximum Transmit Timing	-	20	-	150	ms
	Unjab Timing	-	250	-	750	ms
Link Integrity Timing	Time Link Loss Receive	-	50	-	150	ms
	Link Min Receive	-	2	-	7	ms
	Link Max Receive	-	50	-	150	ms
	Link Transmit Period	-	8	10	24	ms

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 14: RCLK/Start-of-Frame Timing (Over Recommended Range)

Parameter	Sym.	Min	Typ[1]	Max	Units
Decoder acquisition time	tDATA	-	900	1100	ns
CD turn-on delay	tCD	-	50	200	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 14: RCLK/Start-of-Frame Timing (Over Recommended Range) – continued

Parameter		Sym.	Min	Typ[1]	Max	Units
Receive data setup from RCLK	Mode 1	tRDS	60	70	-	ns
	Modes 2, 3 and 4	tRDS	30	45	-	ns
Receive data hold from RCLK	Mode 1	tRDH	10	20	-	ns
	Modes 2, 3 and 4	tRDH	30	45	-	ns
RCLK shut off delay from CD assert (Mode 3)		tSWS	-	±100	-	ns

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 15: RCLK/End-of-Frame Timing (Over Recommended Range)

Parameter	Type	Sym	Mode 1	Mode 2	Mode 3	Mode 4	Units
RCLK after CD off	Minimum	tRC	5	1	27	5	bit times
Rx data throughput delay	Maximum	tRD	400	375	375	375	ns
CD turn off delay [1]	Maximum	tCDOFF	500	475	475	475	ns
Receive block out after TEN off [2]	Typical[3]	tIFG	5	50	-	-	bit times
RCLK switching delay after CD off	Typical[3]	tSWE	-	-	120 (±80)	-	bit times

1. CD Turnoff delay measured from middle of last bit: timing specification is unaffected by the value of the last bit.
2. Blocking of Carrier Detect is disabled during full duplex operation.
3. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

Table 16: Transmit Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
TEN Setup from TCLK	tEHCH	22	-	-	ns
TXD Setup from TCLK	tDSCH	22	-	-	ns
TEN Hold after TCLK	tCHEL	5	-	-	ns
TXD Hold after TCLK	tCHDU	5	-	-	ns
Transmit Start-up Delay	tSTUD	-	350	450	ns
Transmit Through-put Delay	tTPD	-	338	350	ns

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

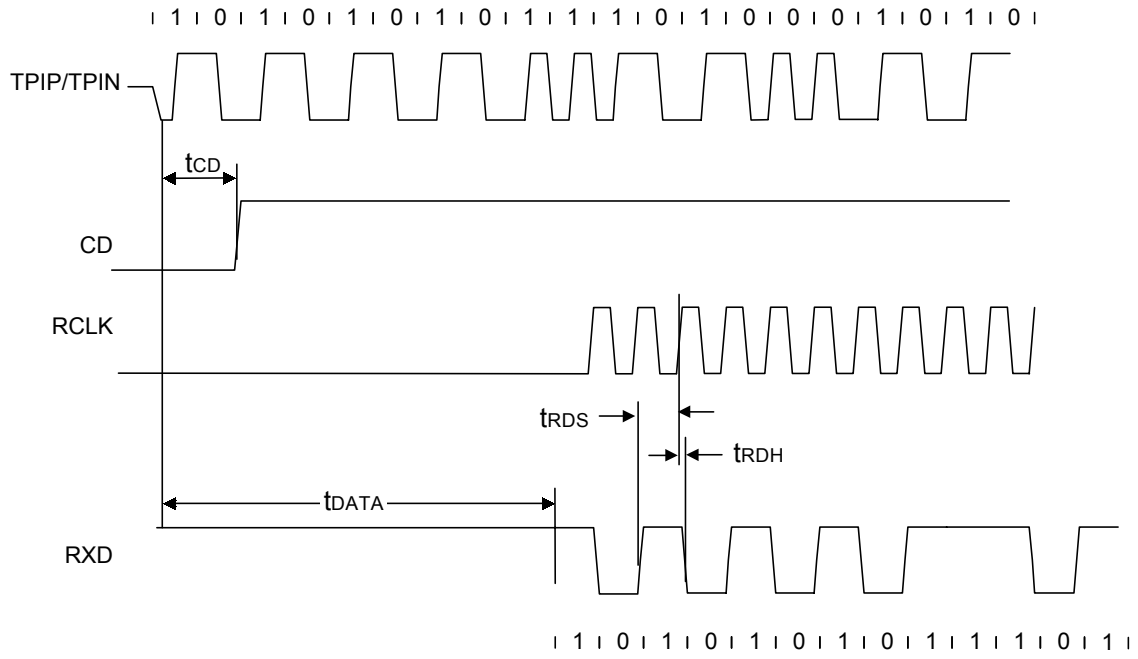
Table 17: Miscellaneous Timing (Over Recommended Range)

Parameter	Symbol	Minimum	Typical [1]	Maximum	Units
COL (SQE) Delay after TEN off	tSQED	0.65	-	1.6	µs
COL (SQE) Pulse Duration	tSQEP	500	-	1500	ns
Power Down recovery time	tPDR	-	TBD	-	ms

1. Typical values are at 25° C and are for design aid only; not guaranteed and not subject to production testing.

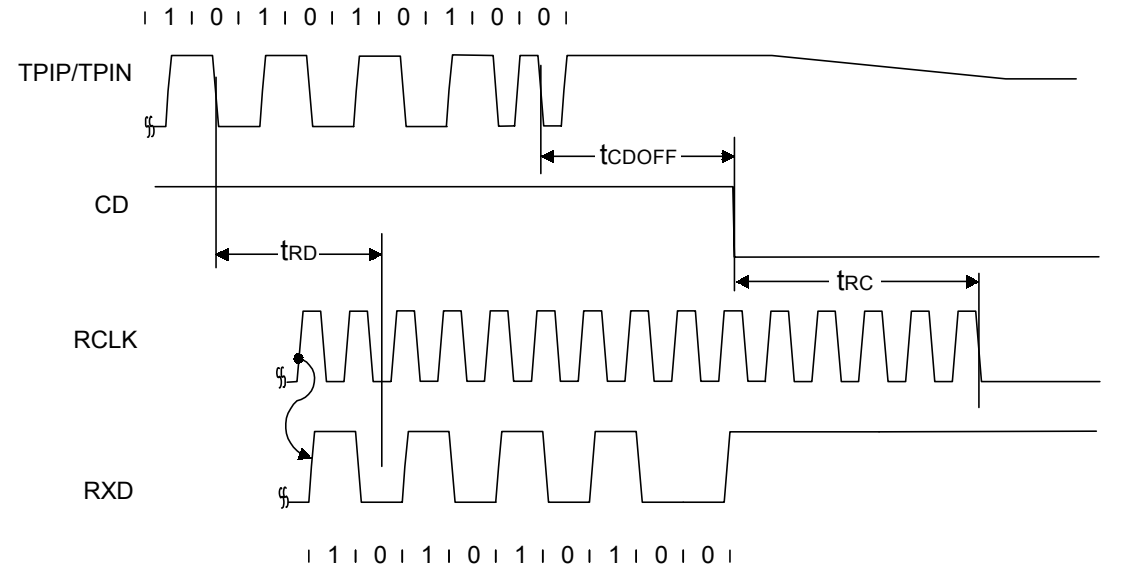
Timing Diagrams for Mode 1 *(MD1=Low, MD0=Low) Figures 10 through 13*

Figure 10: Mode 1 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK

Figure 11: Mode 1 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes 25 ns after the rising edge of RCLK

Figure 12: Mode 1 Transmit Timing

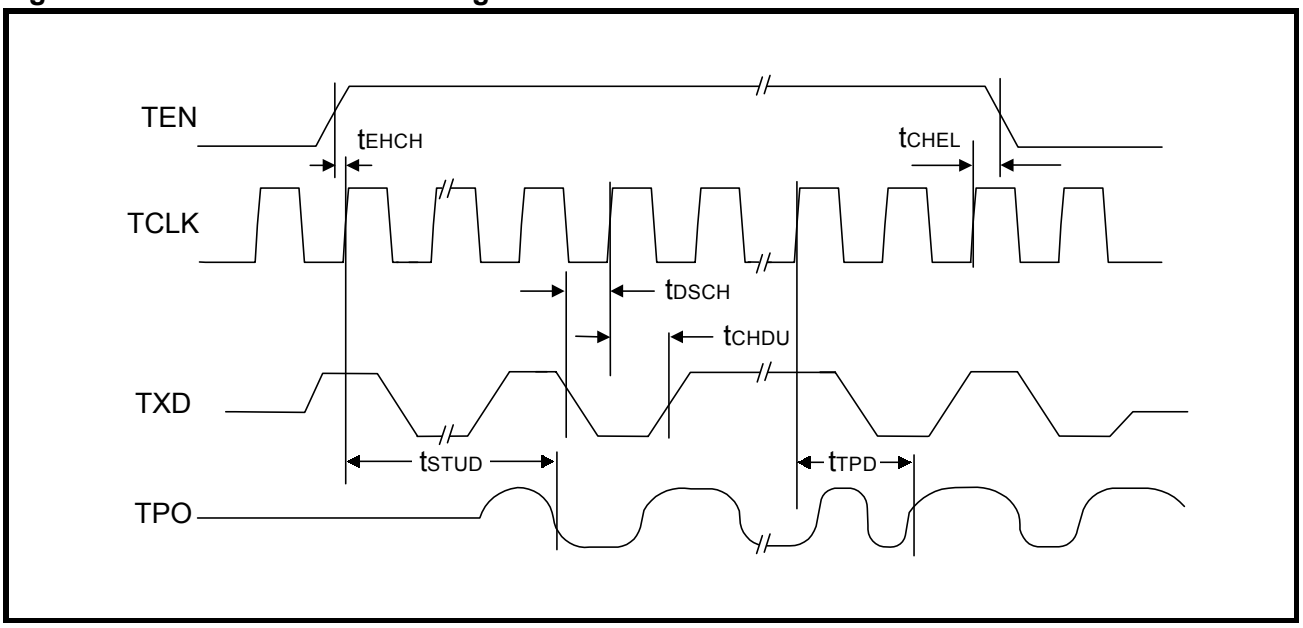
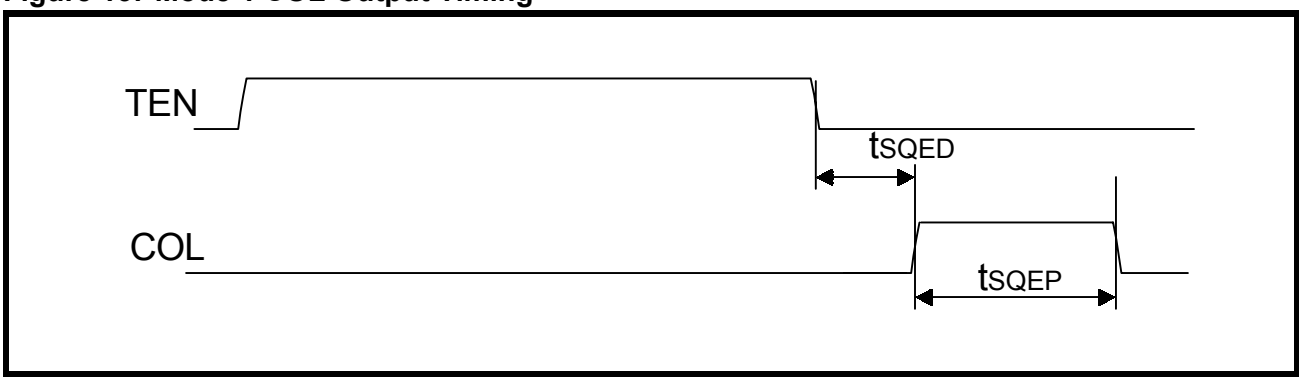
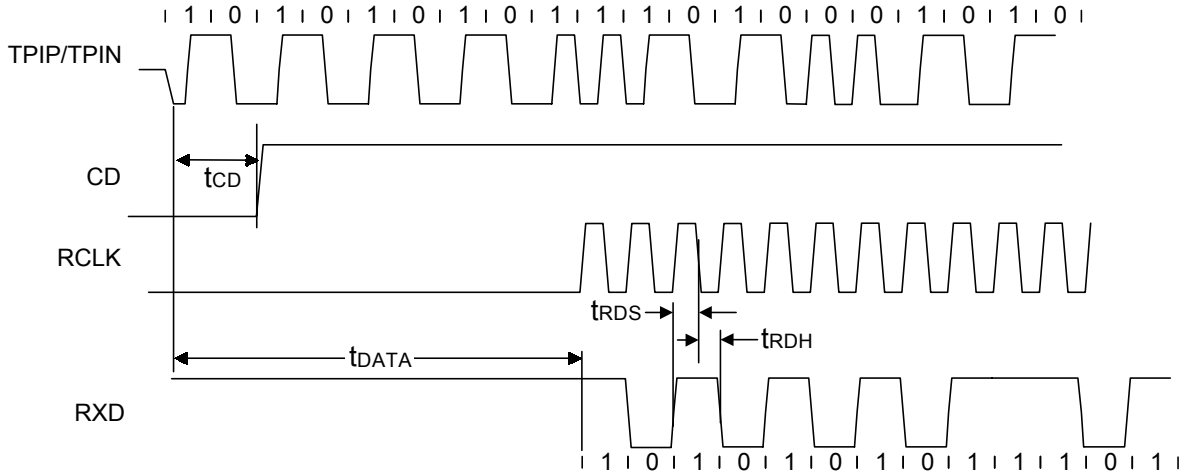


Figure 13: Mode 1 COL Output Timing



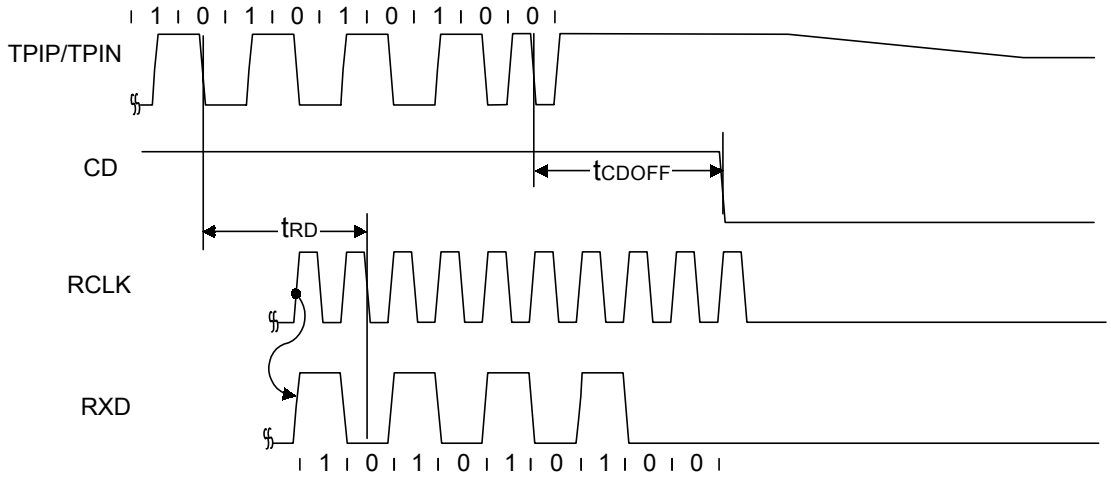
Timing Diagrams for Mode 2 *(MD1=Low, MD0=High) Figures 14 through 17*

Figure 14: Mode 2 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 15: Mode 2 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 16: Mode 2 Transmit Timing

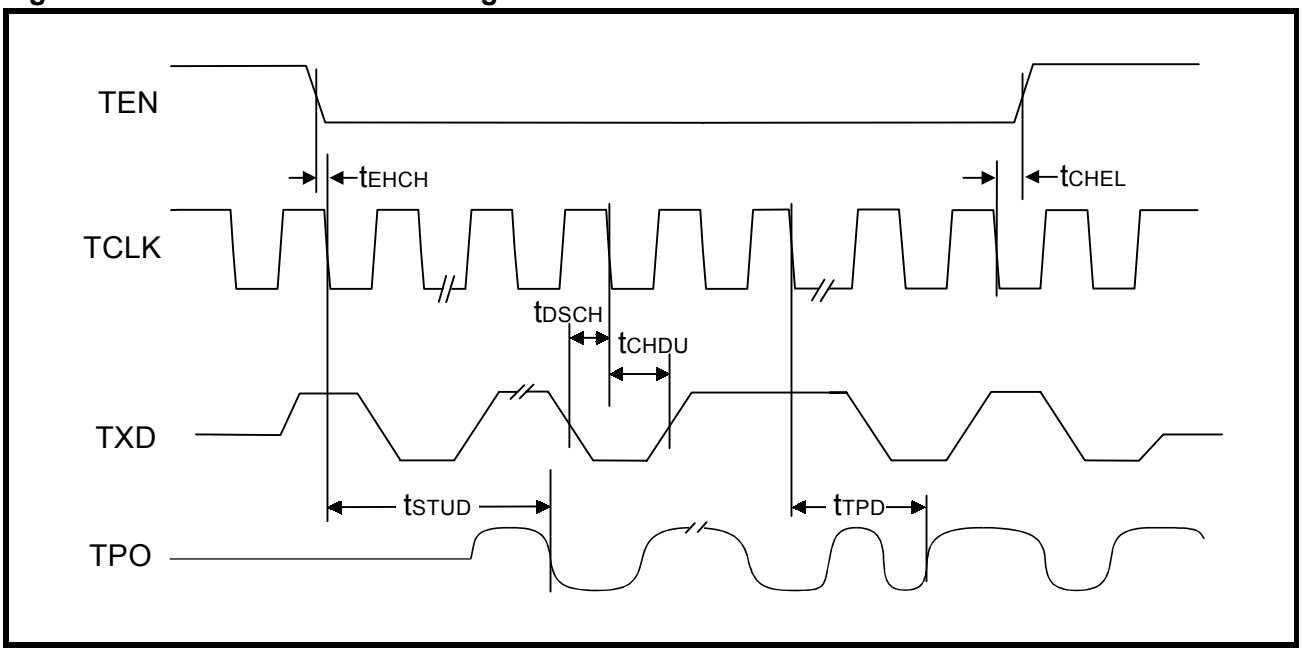
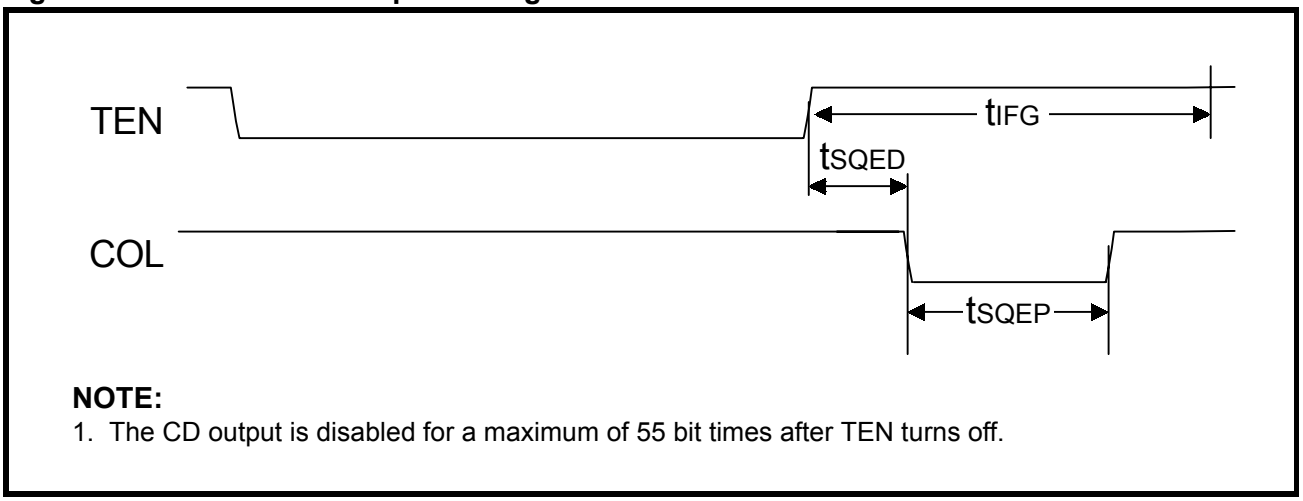


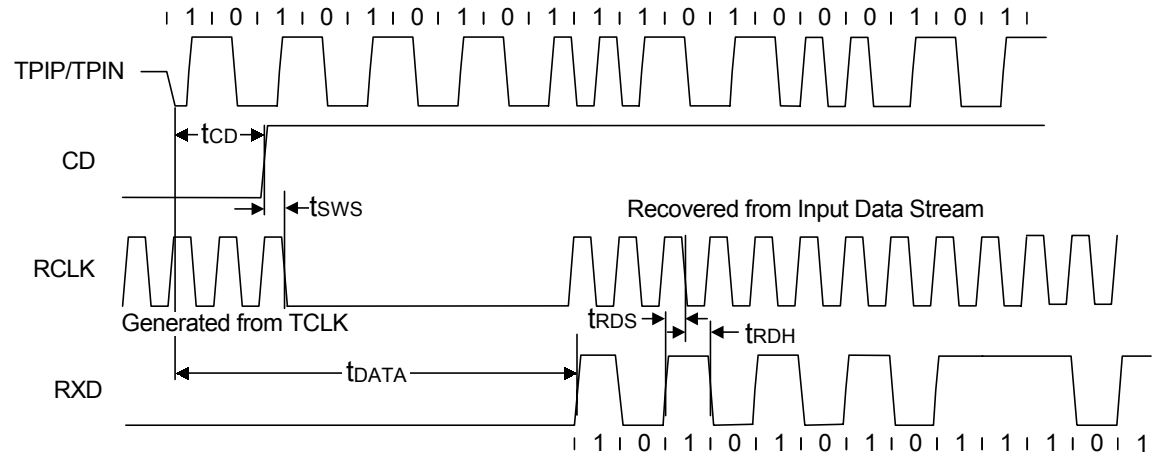
Figure 17: Mode 2 COL Output Timing



NOTE:
1. The CD output is disabled for a maximum of 55 bit times after TEN turns off.

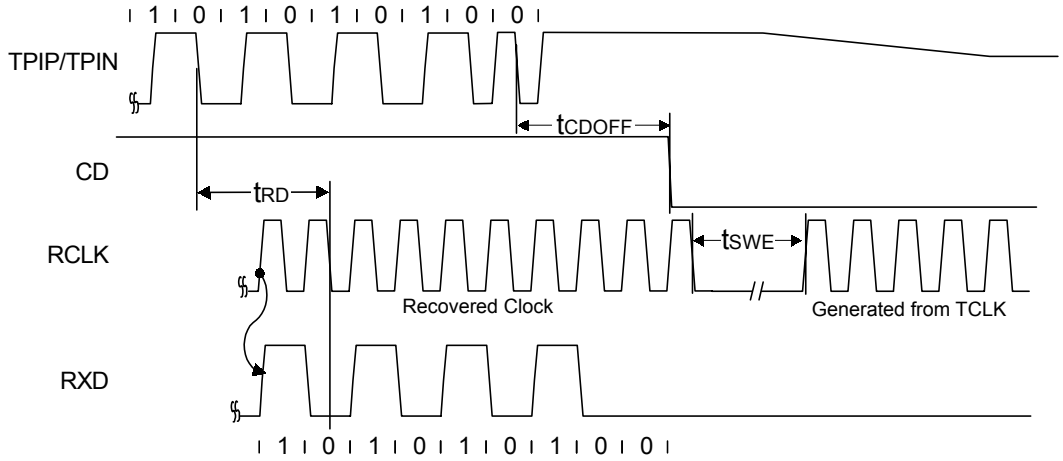
Timing Diagrams for Mode 3 *(MD1=High, MD0=Low) Figures 18 through 21*

Figure 18: Mode 3 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 19: Mode 3 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the rising edge of RCLK; the controller is sampled at the falling edge.

Figure 20: Mode 3 Transmit Timing

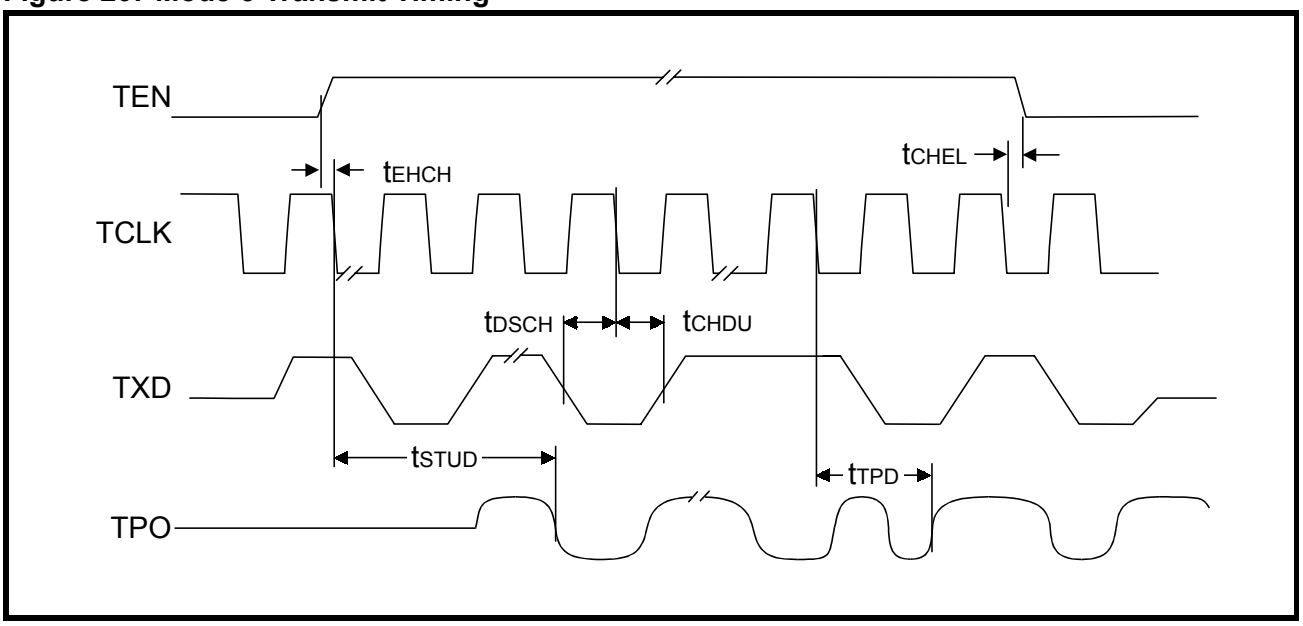
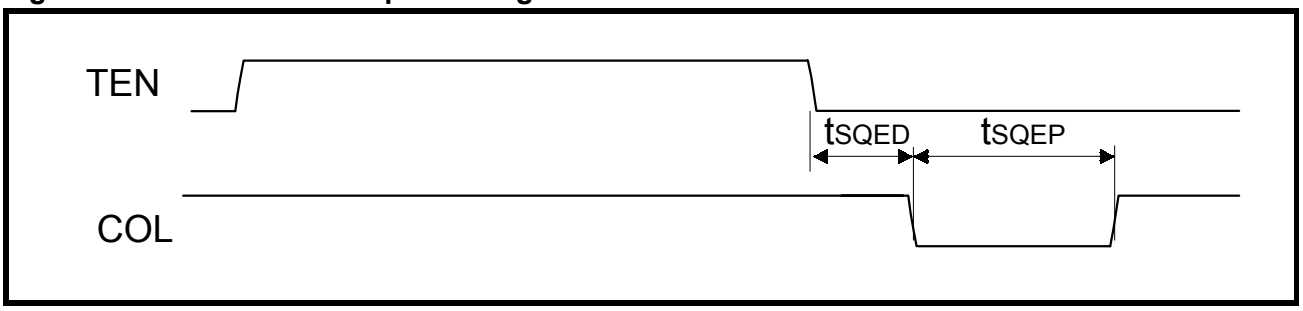
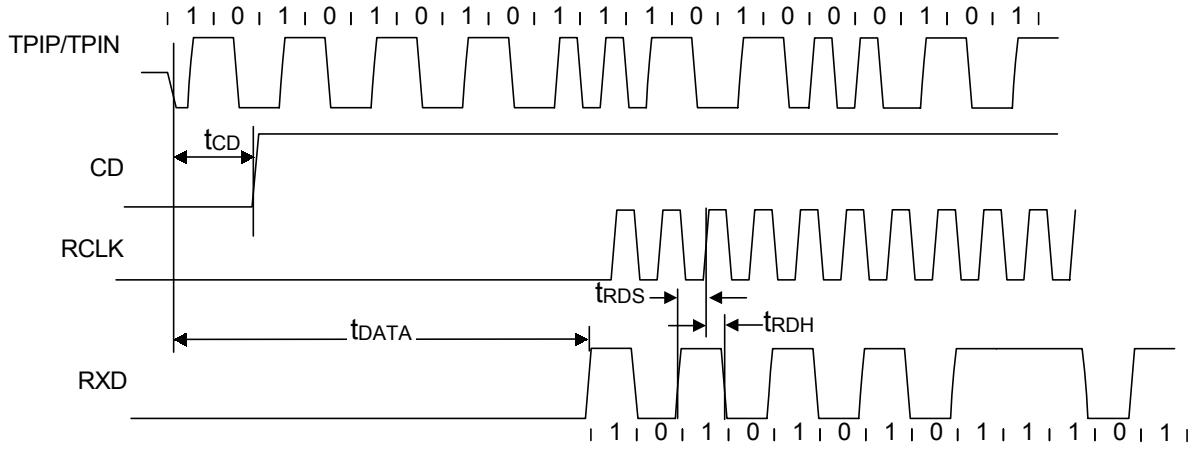


Figure 21: Mode 3 COL Output Timing



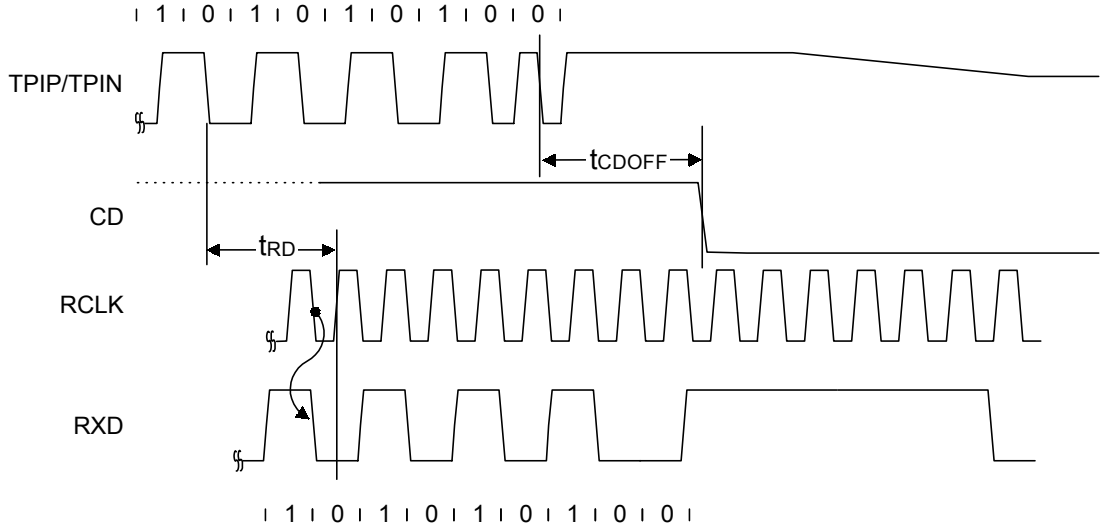
Timing Diagrams for Mode 4 *(MD1=High, MD0=High) Figures 22 through 25*

Figure 22: Mode 4 RCLK/Start-of-Frame Timing



NOTE:
1. RXD changes at the falling edge of RCLK; the controller is sampled at the rising edge.

Figure 23: Mode 4 RCLK/End-of-Frame Timing



NOTE:
1. RXD changes at the falling edge of RCLK; the controller is sampled at the rising edge.

Figure 24: Mode 4 Transmit Timing

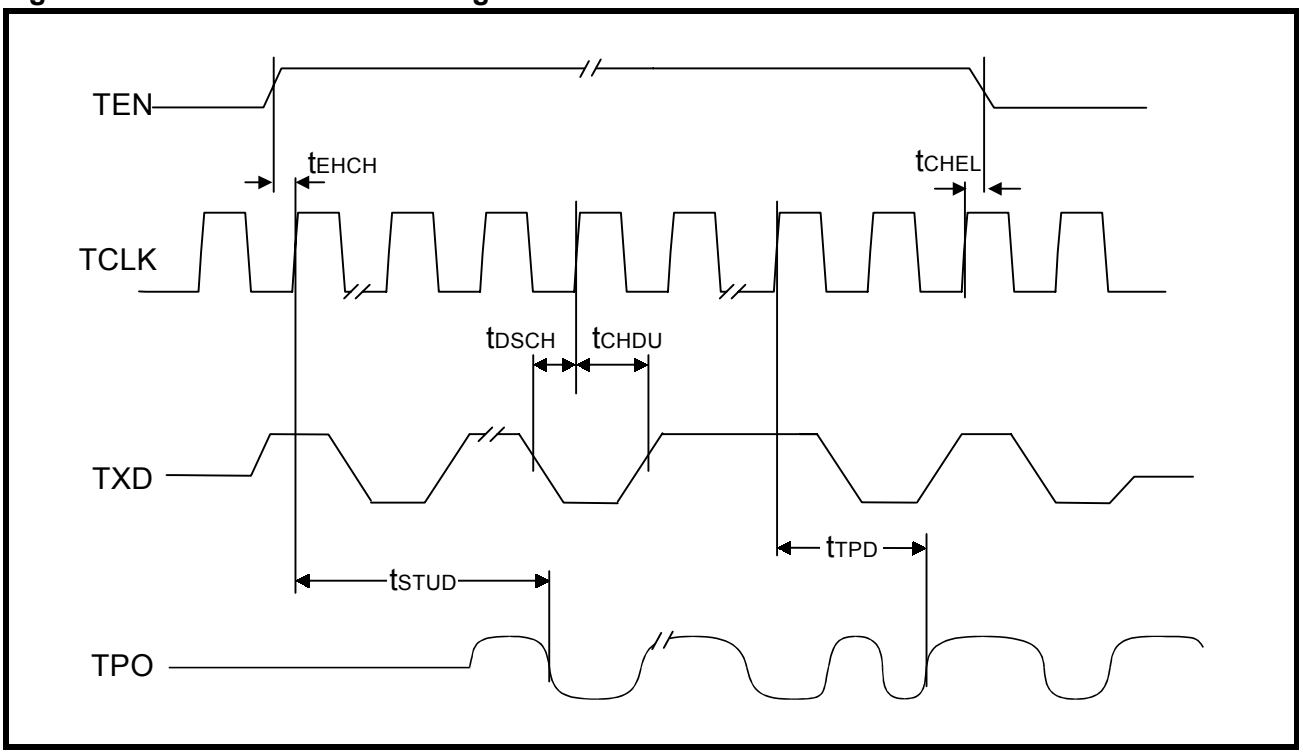
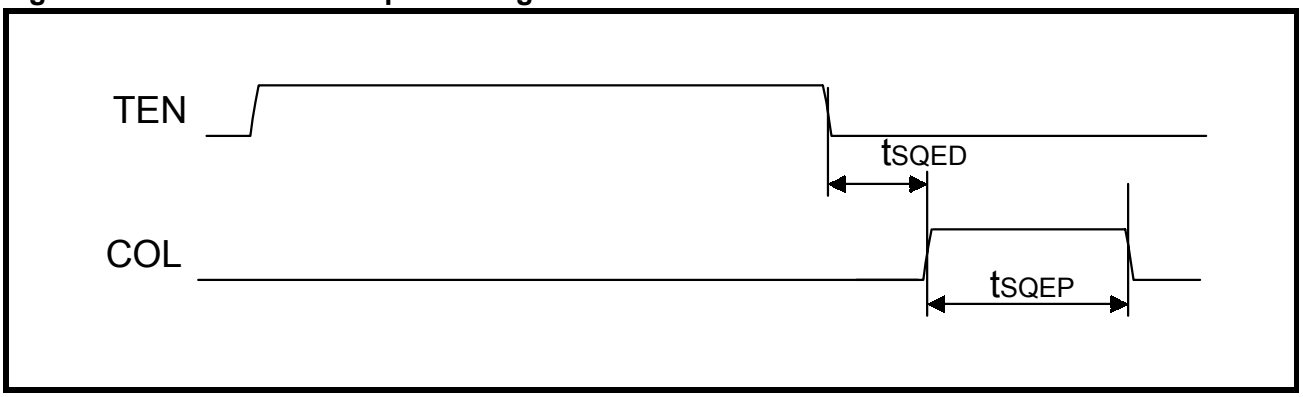


Figure 25: Mode 4 COL Output Timing



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