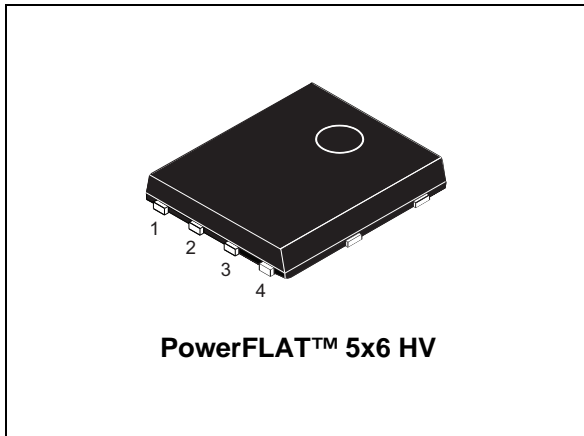
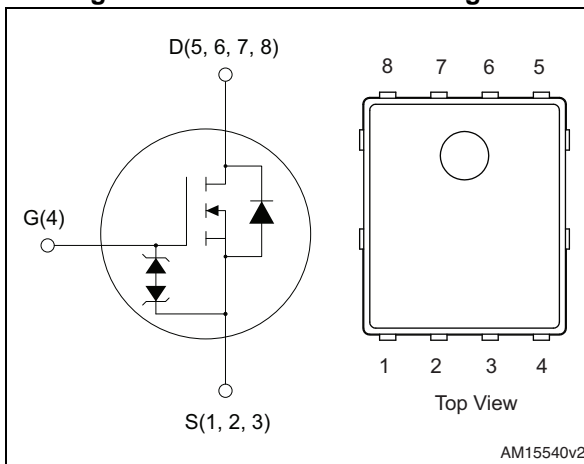


## N-channel 600 V, 0.39 $\Omega$ typ., 7 A MDmesh II Plus™ low $Q_g$ Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet – production data



**Figure 1. Internal schematic diagram**



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STL13N60M2	650 V	0.42 $\Omega$	7 A

- Extremely low gate charge
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL13N60M2	13N60M2	PowerFLAT™ 5x6 HV	Tape and reel

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	7 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	4.7	A
$I_{DM}^{(2)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	55	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_j$	Max. operating junction temperature	150	

1. The value is rated according to  $R_{thj-case}$  and limited by package
2. Pulse width limited by safe operating area.
3.  $I_{SD} \leq 7\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\ peak} < V_{(BR)DSS}$ ,  $V_{DD}=400\text{ V}$ .
4.  $V_{DS} \leq 480\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.27	°C/W
$R_{thj-pcb}$	Thermal resistance junction-pcb max <sup>(1)</sup>	59	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4, 2 Oz copper board

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	2.8	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ ; $V_{DD}=50$ )	125	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 4.5\text{ A}$		0.39	0.42	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0, V_{DS} = 100\text{ V}, f = 1\text{ MHz},$	-	580	-	pF
$C_{oss}$	Output capacitance		-	32	-	pF
$C_{riss}$	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	120	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	6.6	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 11\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	17	-	nC
$Q_{gs}$	Gate-source charge		-	2.5	-	nC
$Q_{gd}$	Gate-drain charge		-	9	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 5.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> and <a href="#">19</a> )	-	11	-	ns
$t_r$	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	41	-	ns
$t_f$	Fall time		-	9.5	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0$ , $I_{SD} = 7\text{ A}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 16</a> )	-	297		ns
$Q_{rr}$	Reverse recovery charge		-	2.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	18.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 11\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	394		ns
$Q_{rr}$	Reverse recovery charge		-	3.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	19		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

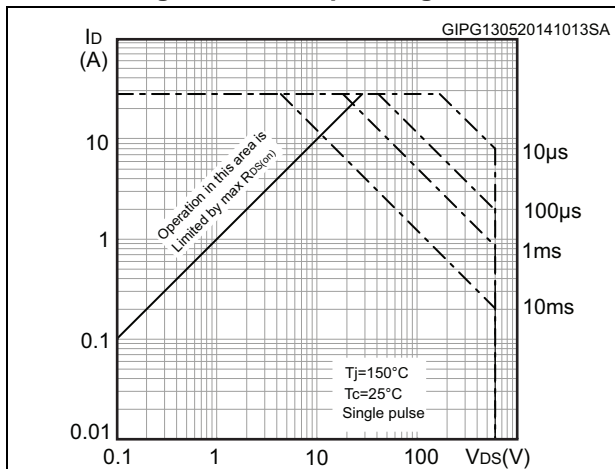


Figure 3. Thermal impedance

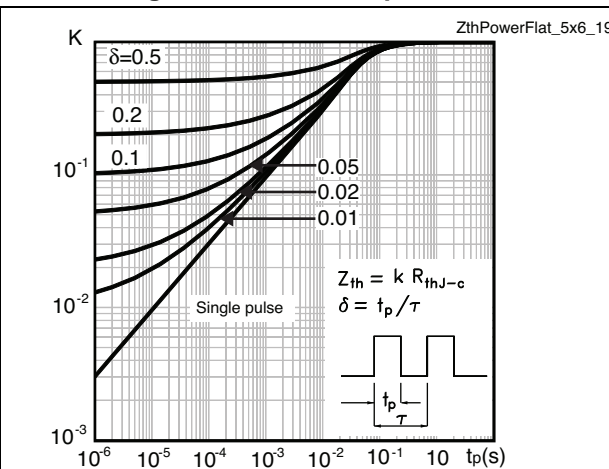


Figure 4. Output characteristics

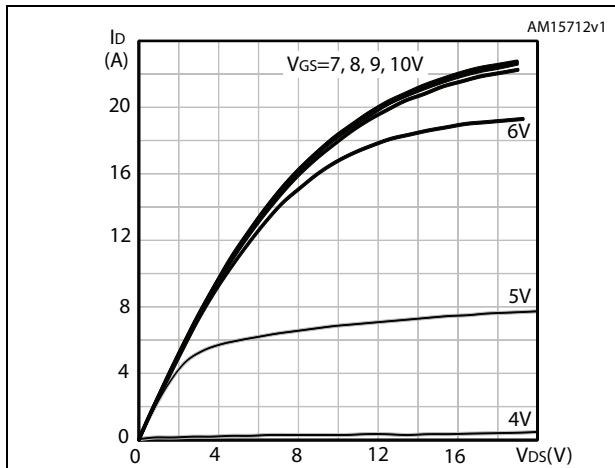


Figure 5. Transfer characteristics

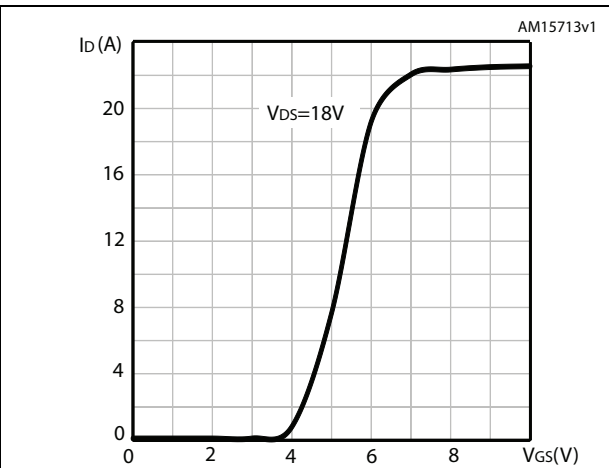


Figure 6. Normalized  $V_{BR(DSS)}$  vs temperature

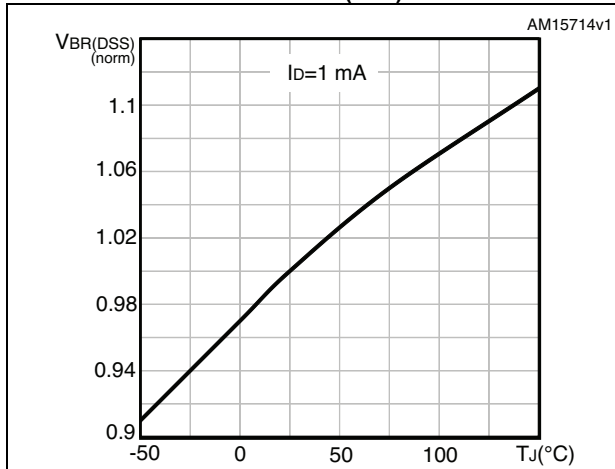


Figure 7. Static drain-source on-resistance

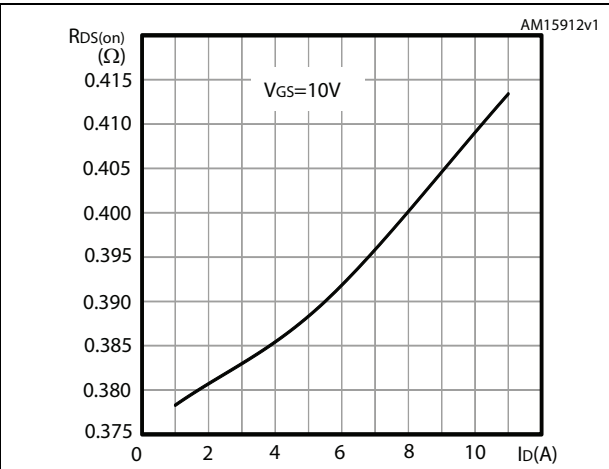


Figure 8. Gate charge vs gate-source voltage

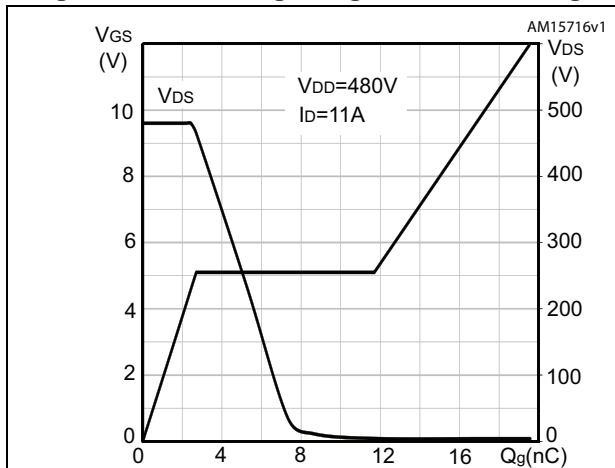


Figure 9. Capacitance variations

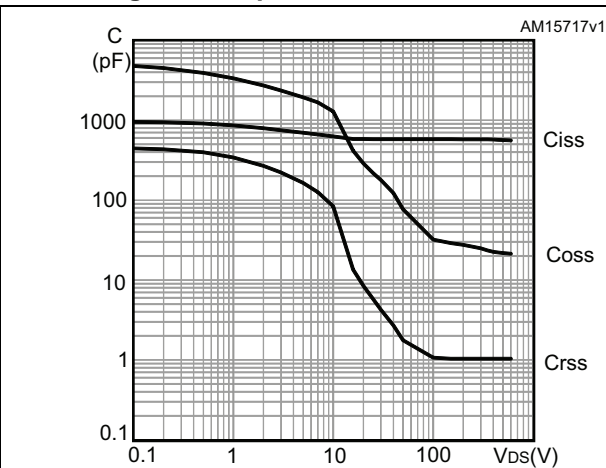


Figure 10. Normalized gate threshold voltage vs temperature

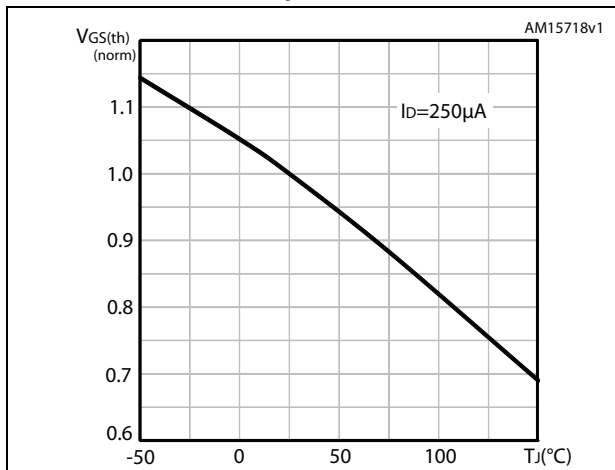


Figure 11. Normalized on-resistance vs temperature

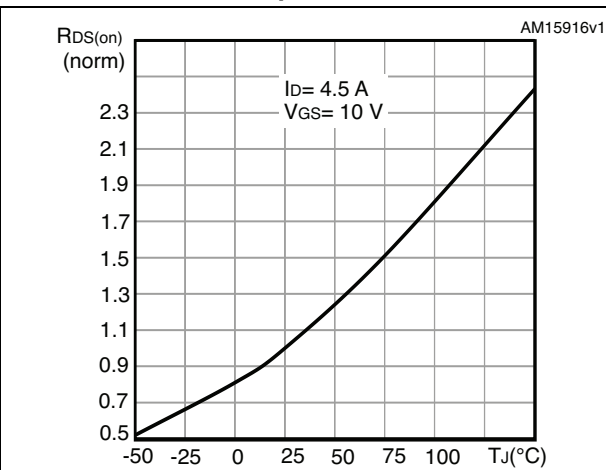


Figure 12. Source-drain diode forward characteristics

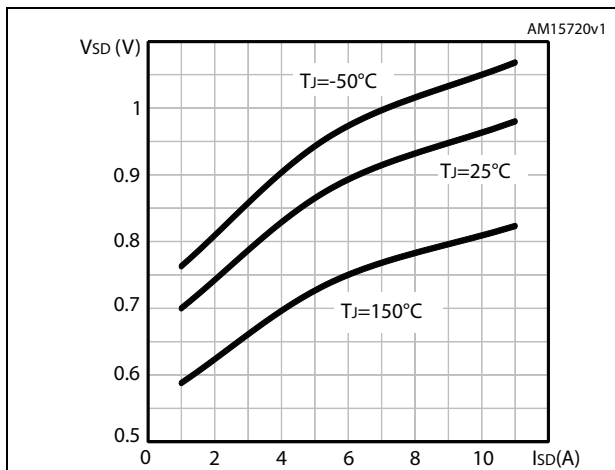
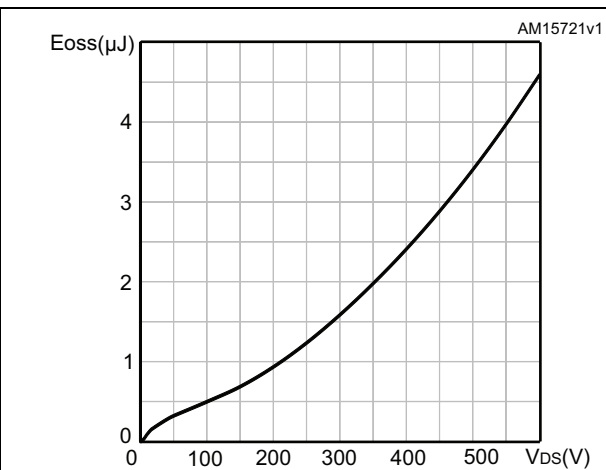


Figure 13. Output capacitance stored energy



### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



Figure 15. Gate charge test circuit



Figure 16. Test circuit for inductive load switching and diode recovery times

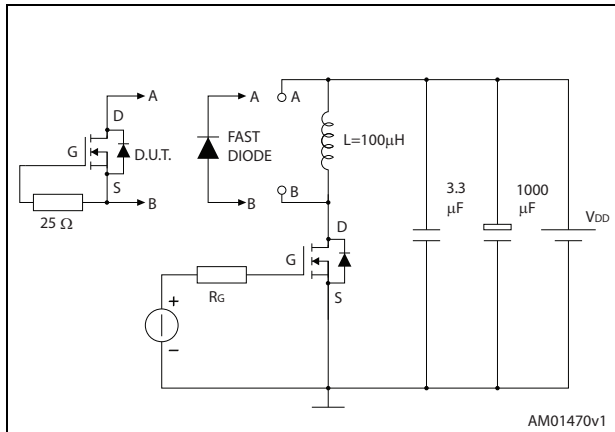


Figure 17. Unclamped inductive load test circuit



Figure 18. Unclamped inductive waveform

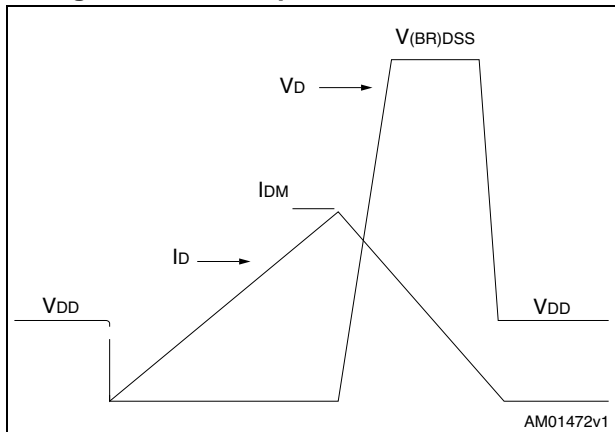


Figure 19. Switching time waveform





## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 20. PowerFLAT™ 5x6 HV drawing

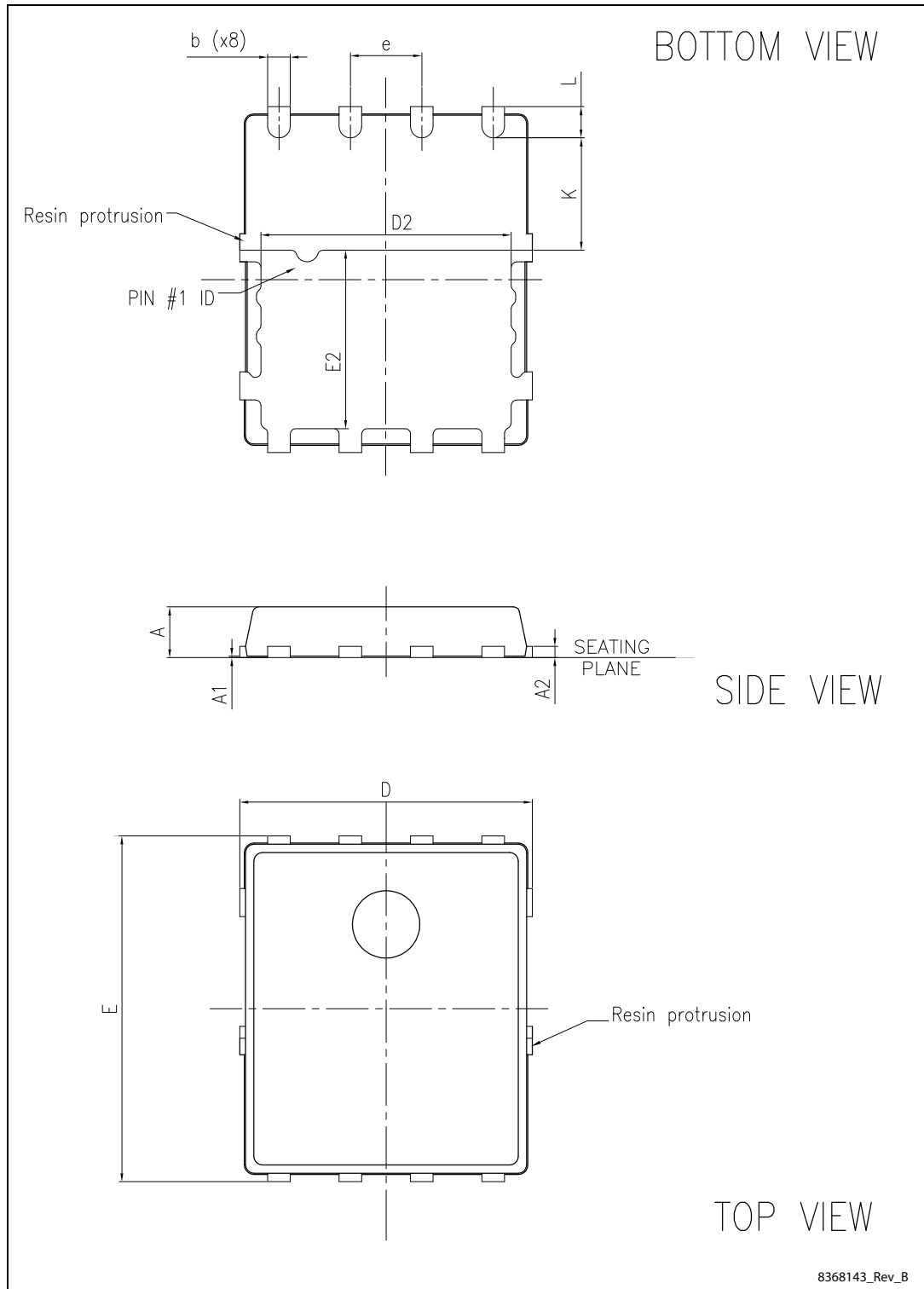


Figure 21. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)

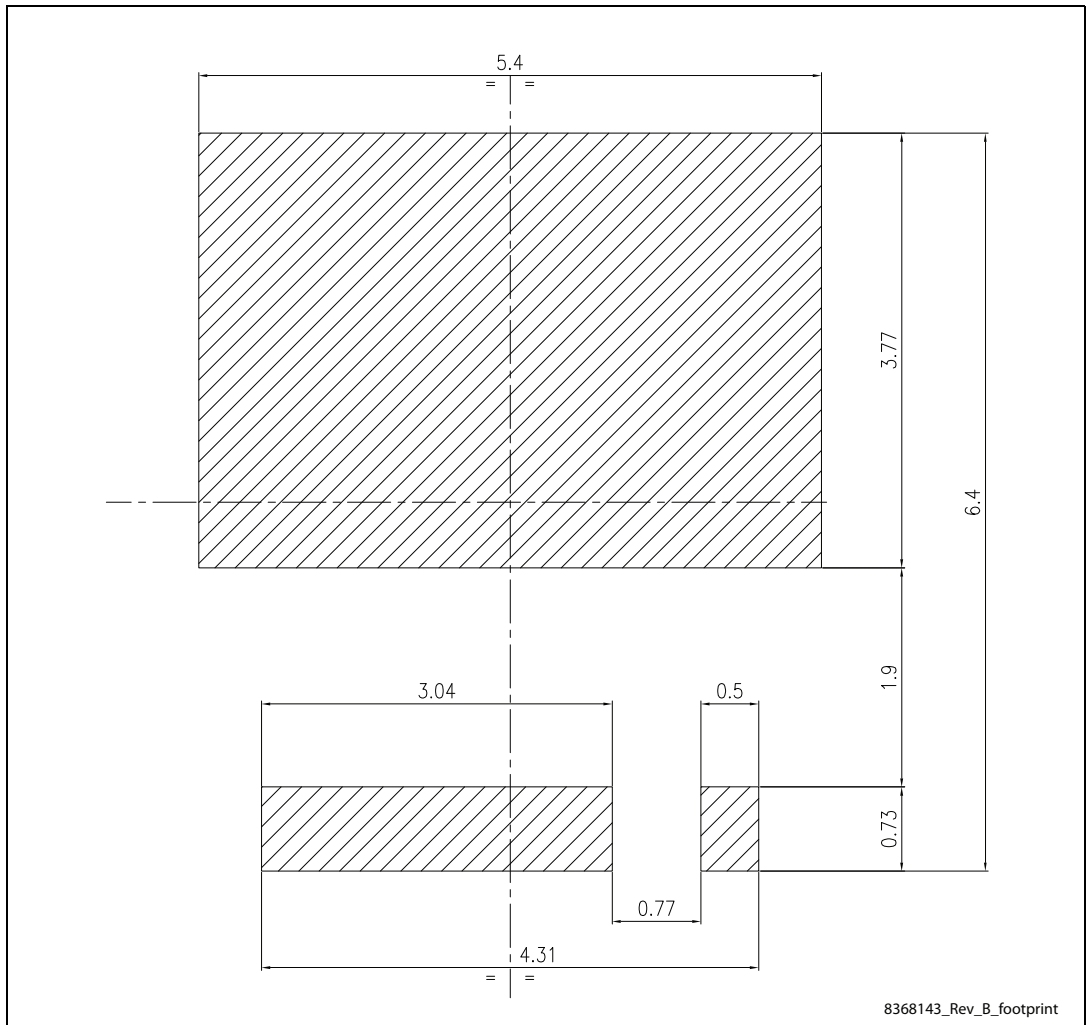
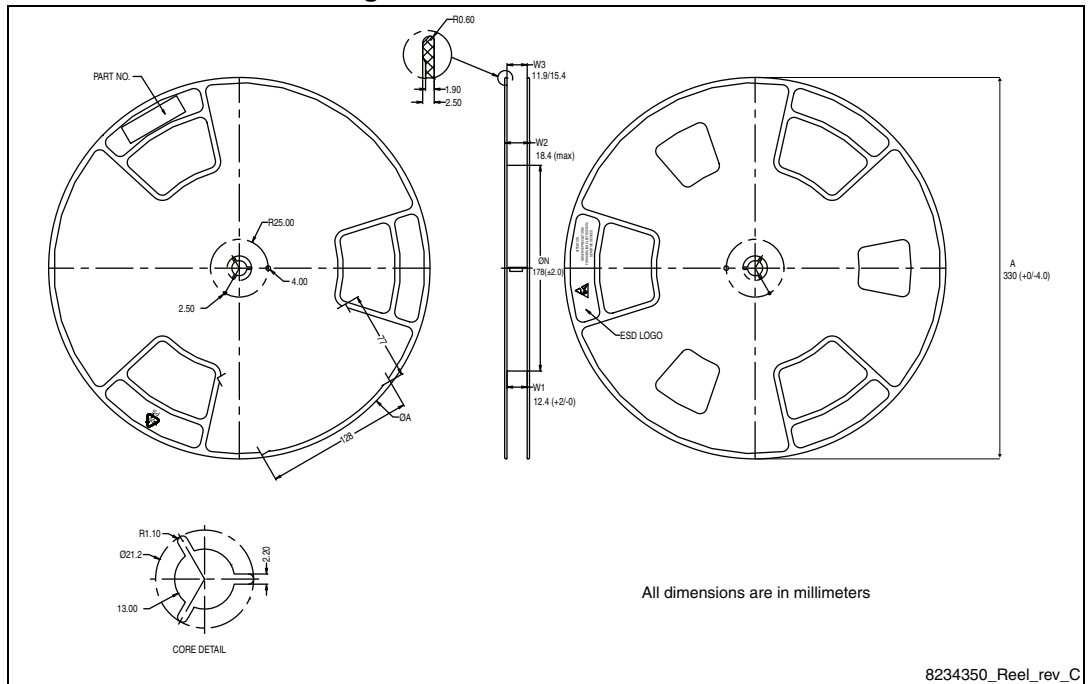


Table 9. PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10



Figure 24. PowerFLAT™ 5x6 reel



## 6 Revision history

Table 10. Document revision history

Date	Revision	Changes
15-May-2014	1	First release.
27-Jun-2014	2	– Updated: <a href="#">Figure 3</a> – Minor text changes

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