

The RF MOSFET Line 30W, to 400MHz, 28V

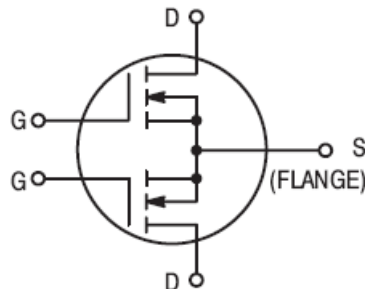
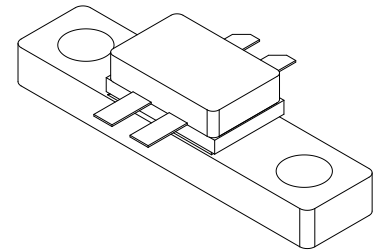
Rev. V2

Designed for wideband large signal amplifier and oscillator applications
Up to 400 MHz range, in either single-ended or push-pull configuration.

N-Channel enhancement mode

- Guaranteed 28 volt, 150 MHz performance
Output power = 30 Watts
Broadband gain = 14 dB (Typ.)
Efficiency = 54% (Typ.)
- Small- and large-signal characterization
- 100% tested for load mismatch at all phase angles with 30:1 VSWR
- Space saving package for push-pull circuit applications
- Excellent thermal stability, ideally suited for Class A operation
- Facilitates manual gain control, ALC and modulation techniques

Product Image



MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|-----------|--------------|------------------------------|
| Drain-Source Voltage | V_{DSS} | 65 | Vdc |
| Drain-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$) | V_{DGR} | 65 | Vdc |
| Gate-Source Voltage | V_{GS} | ± 40 | Vdc |
| Drain Current — Continuous | I_D | 5.0 | Adc |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 100 0.571 | Watts W/ $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -65 to +150 | $^\circ\text{C}$ |
| Operating Junction Temperature | T_J | 200 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--------------------------------------|-----------------|------|---------------------------|
| Thermal Resistance, Junction to Case | $R_{\theta JC}$ | 1.75 | $^\circ\text{C}/\text{W}$ |

Handling and Packaging — MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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Rev. V2

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS (1)

| | | | | | |
|--|---------------|----|---|-----|-----------------|
| Drain–Source Breakdown Voltage ($V_{GS} = 0, I_D = 5.0 \text{ mA}$) | $V_{(BR)DSS}$ | 65 | — | — | Vdc |
| Zero–Gate Voltage Drain Current ($V_{DS} = 28 \text{ V}, V_{GS} = 0$) | I_{DSS} | — | — | 2.0 | mAdc |
| Gate–Source Leakage Current ($V_{GS} = 40 \text{ V}, V_{DS} = 0$) | I_{GSS} | — | — | 1.0 | μAdc |

ON CHARACTERISTICS (1)

| | | | | | |
|---|--------------|-----|-----|-----|-------|
| Gate Threshold Voltage ($V_{DS} = 10 \text{ V}, I_D = 25 \text{ mA}$) | $V_{GS(th)}$ | 1.0 | 3.0 | 6.0 | Vdc |
| Forward Transconductance ($V_{DS} = 10 \text{ V}, I_D = 250 \text{ mA}$) | g_{fs} | 250 | 400 | — | mmhos |

DYNAMIC CHARACTERISTICS (1)

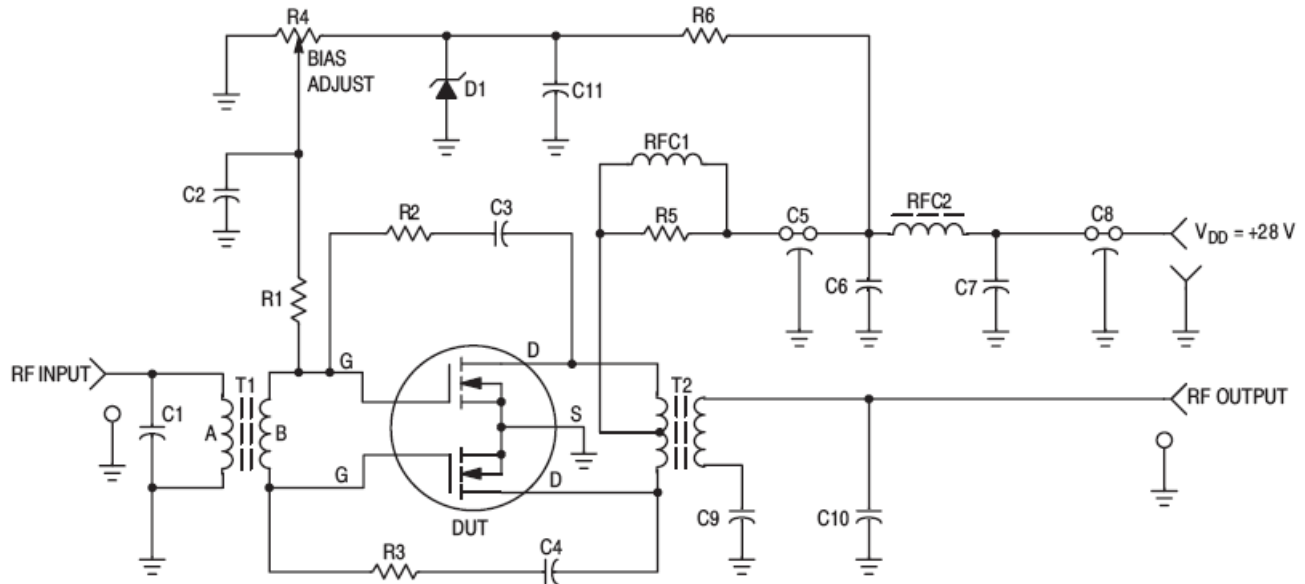
| | | | | | |
|--|-----------|---|-----|---|----|
| Input Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$) | C_{iss} | — | 24 | — | pF |
| Output Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$) | C_{oss} | — | 27 | — | pF |
| Reverse Transfer Capacitance ($V_{DS} = 28 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz}$) | C_{rss} | — | 5.5 | — | pF |

FUNCTIONAL CHARACTERISTICS (2)

| | | | | | |
|--|----------|--------------------------------|----|---|----|
| Common Source Power Gain (Figure 1) ($V_{DD} = 28 \text{ Vdc}, P_{out} = 30 \text{ W}, f = 150 \text{ MHz}, I_{DQ} = 100 \text{ mA}$) | G_{ps} | 12 | 14 | — | dB |
| Drain Efficiency (Figure 1) ($V_{DD} = 28 \text{ Vdc}, P_{out} = 30 \text{ W}, f = 150 \text{ MHz}, I_{DQ} = 100 \text{ mA}$) | η | 50 | 54 | — | % |
| Electrical Ruggedness (Figure 1) ($V_{DD} = 28 \text{ Vdc}, P_{out} = 30 \text{ W}, f = 150 \text{ MHz}, I_{DQ} = 100 \text{ mA},$ VSWR 30:1 at all Phase Angles) | ψ | No Degradation in Output Power | | | |

NOTES:

1. Each side measured separately.
2. Measured in push–pull configuration.



- C1 — 5.0 pF
- C2, C3, C4, C6, C7, C9, C11 — 0.1 μ F Ceramic
- C5, C8 — 680 pF Feedthru
- C10 — 15 pF
- D1 — 1N4740 Motorola Zener
- RFC1 — 17 Turns, #24 AWG Wound on R5
- RFC2 — Ferroxcube VK-200-19/4B or Equivalent
- R1 — 10 k Ω , 1/4 W
- R2, R3 — 560 Ω , 1/2 W
- R4 — 10 Turns, 10 k Ω

- R5 — 56 k Ω , 1 W
- R6 — 1.6 k Ω , 1/4 W
- T1 — Primary Winding — 3 Turns #28 Enameled Wire.
— Secondary Winding — 2 Turns #28 Enameled Wire.
Both windings wound through a Fair/Rite Balun 65 core.
Part #2865002402.
- T2 — 1:1 Transformer Wound Bifilar — 2 Turns Twisted Pair
#24 Enameled Wire through a Indiana General Balun Q1
core. Part #18006-1-Q1. Primary winding center tapped.
- Board Material — 0.062" G10, 1 oz. Cu Clad, Double Sided

Figure 1. 30–150 MHz Test Circuit

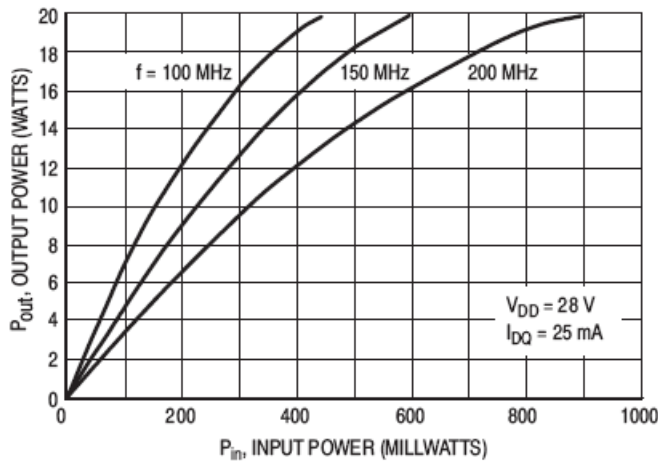


Figure 2. Output Power versus Input Power

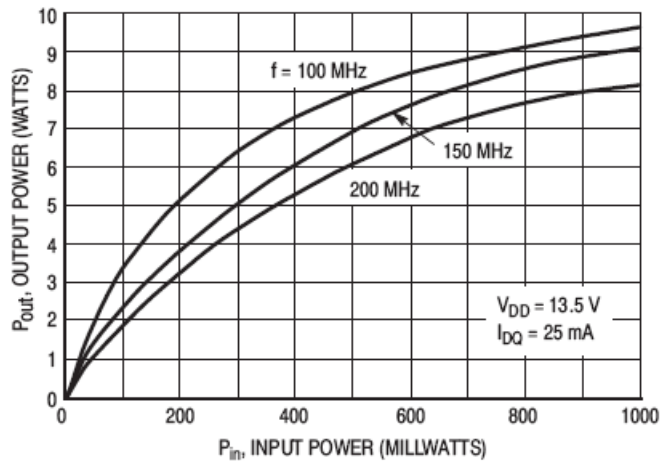


Figure 3. Output Power versus Input Power

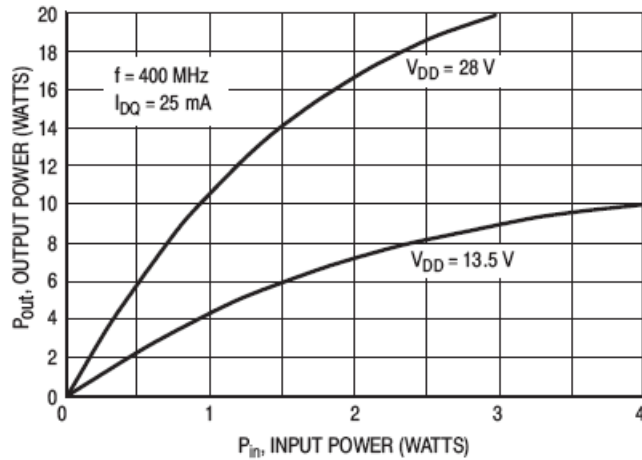


Figure 4. Output Power versus Input Power

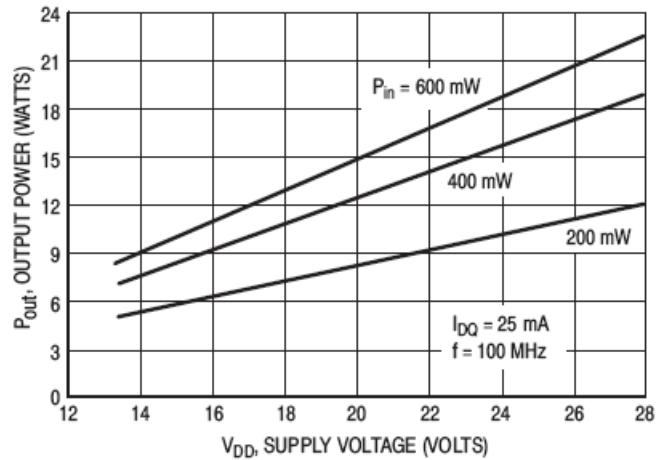


Figure 5. Output Power versus Supply Voltage

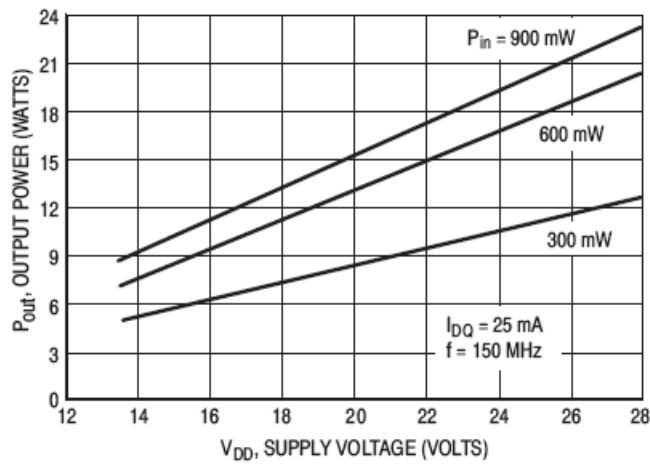


Figure 6. Output Power versus Supply Voltage

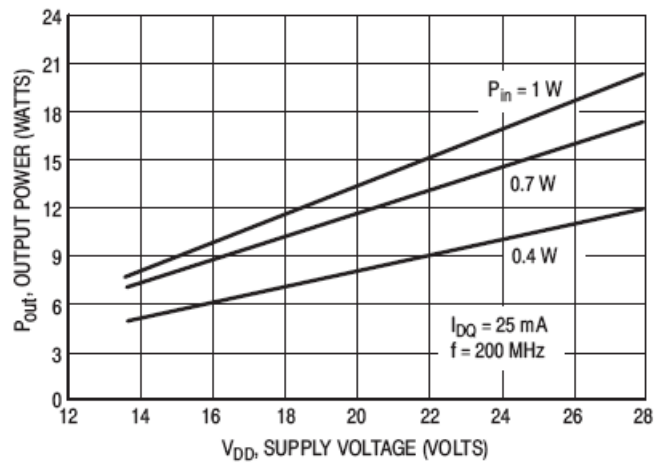


Figure 7. Output Power versus Supply Voltage

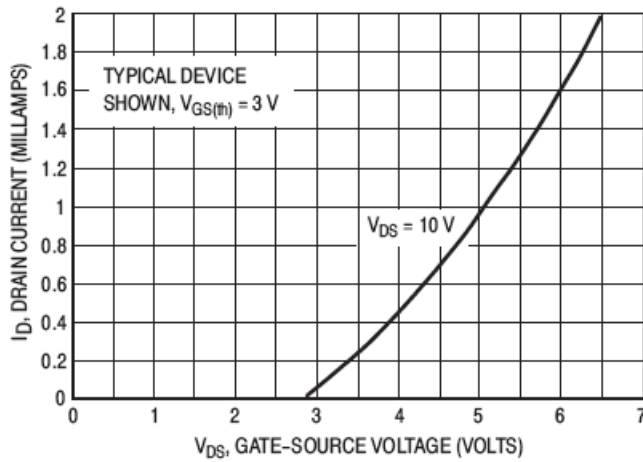


Figure 8. Drain Current versus Gate Voltage (Transfer Characteristics)*

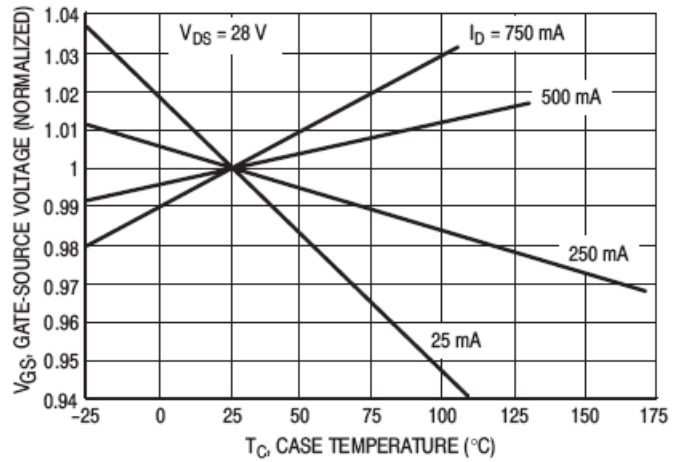


Figure 9. Gate-Source Voltage versus Case Temperature*

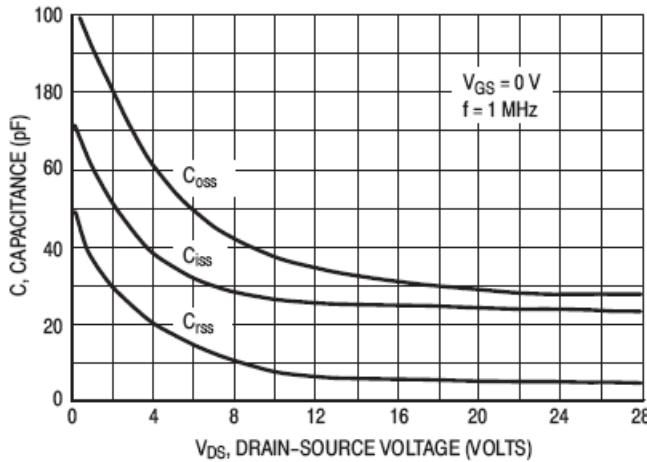


Figure 10. Capacitance versus Drain-Source Voltage

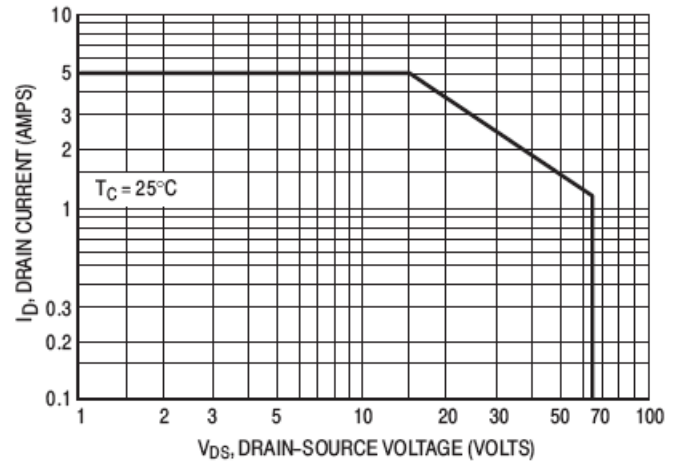


Figure 11. DC Safe Operating Area

TYPICAL PERFORMANCE IN BROADBAND TEST CIRCUIT
(Refer to Figure 1)

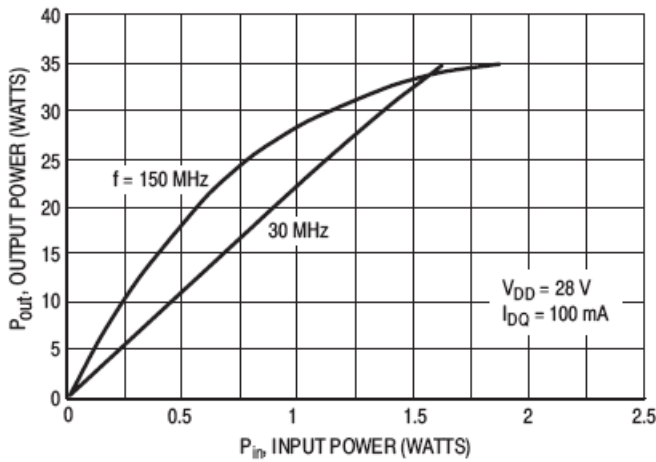


Figure 12. Output Power versus Input Power

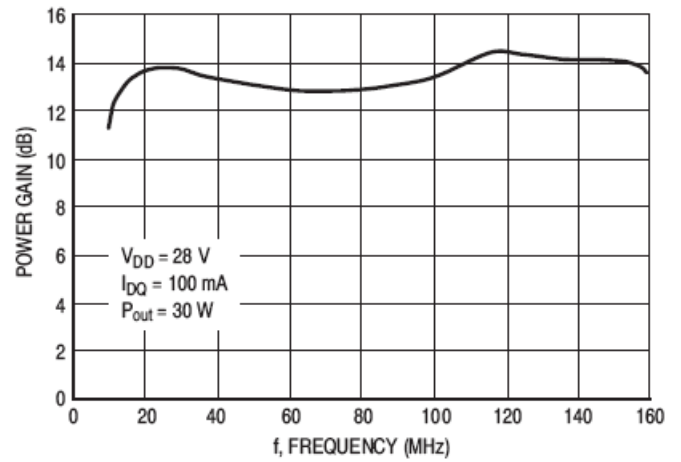


Figure 13. Power Gain versus Frequency

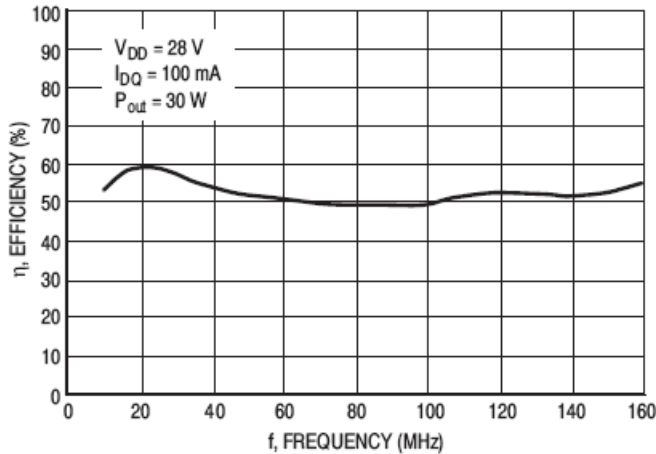


Figure 14. Drain Efficiency versus Frequency

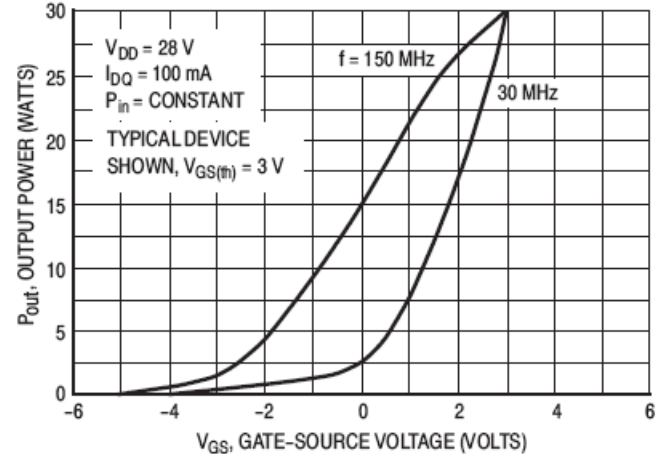


Figure 15. Output Power versus Gate Voltage

TYPICAL 400 MHz PERFORMANCE

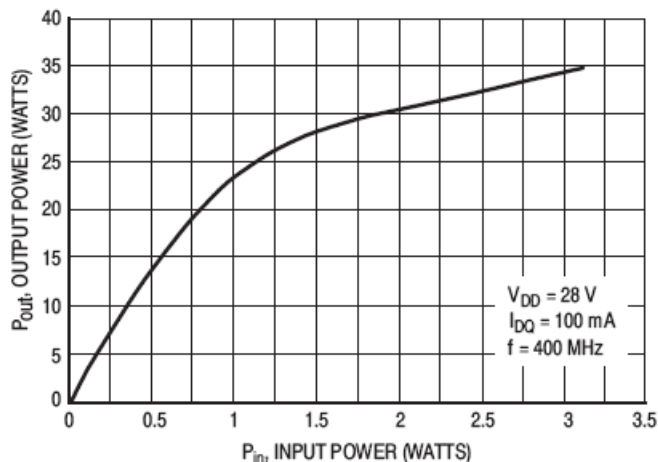


Figure 16. Output Power versus Input Power

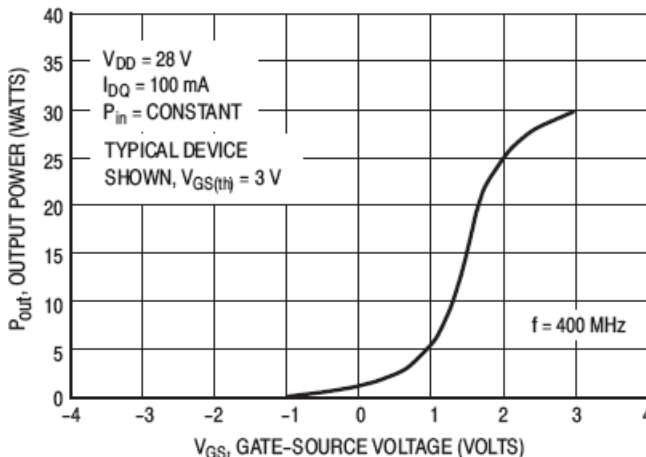


Figure 17. Output Power versus Gate Voltage

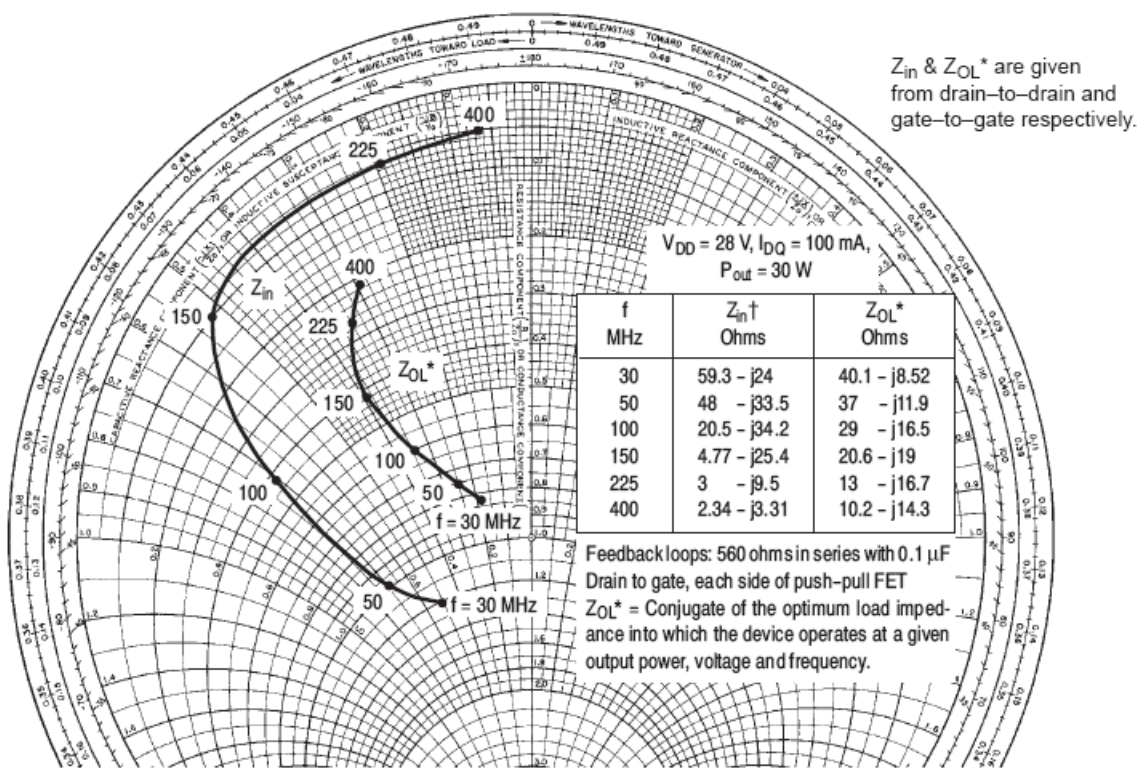


Figure 18. Input and Output Impedance

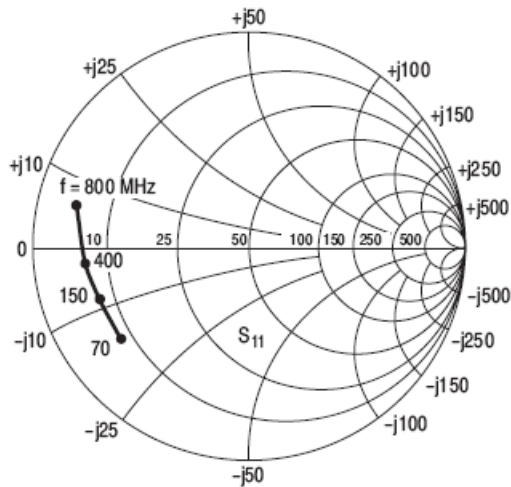


Figure 19. S_{11} , Input Reflection Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

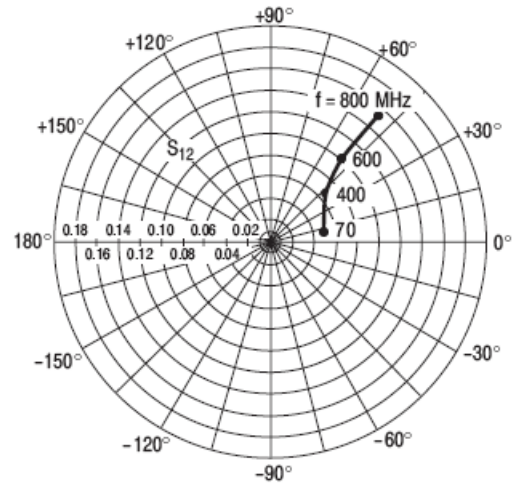


Figure 20. S_{12} , Reverse Transmission Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

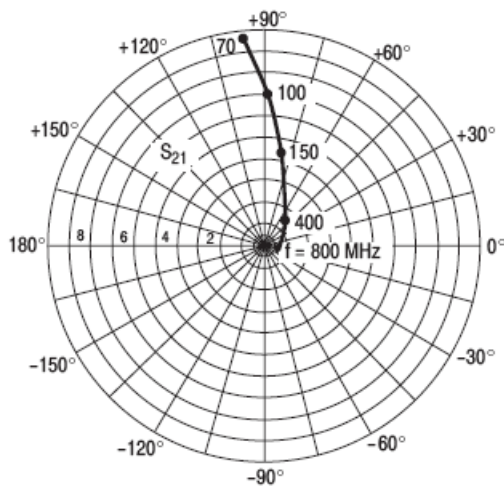


Figure 21. S_{21} , Forward Transmission Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

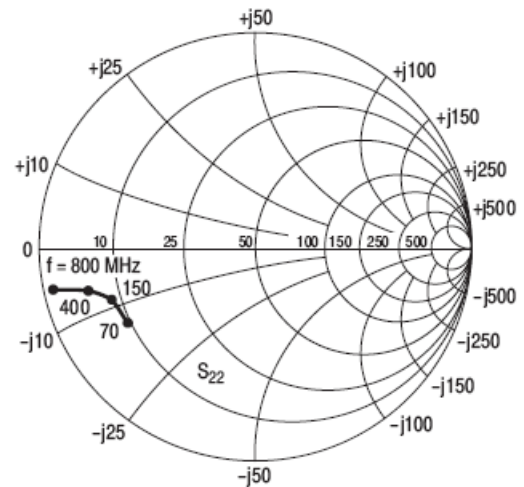


Figure 22. S_{22} , Output Reflection Coefficient versus Frequency
 $V_{DS} = 28\text{ V}$ $I_D = 0.5\text{ A}$

RF POWER MOSFET CONSIDERATIONS

DESIGN CONSIDERATIONS

The MRF136Y is a RF power N-Channel enhancement-mode field-effect transistor (FET) designed especially for VHF power amplifier applications. M/A-COM RF MOS FETs feature a vertical structure with a planar design, thus avoiding the processing difficulties associated with V-groove vertical power FETs.

M/A-COM Application Note AN211A, FETs in Theory and Practice, is suggested reading for those not familiar with the construction and characteristics of FETs.

The major advantages of RF power FETs include high gain, low noise, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage. Power output can be varied over a wide range with a low power dc control signal, thus facilitating manual gain control, ALC and modulation.

DC BIAS

The MRF136Y is an enhancement mode FET and, therefore, does not conduct when drain voltage is applied. Drain current flows when a positive voltage is applied to the gate. See Figure 10 for a typical plot of drain current versus gate voltage. RF power FETs require forward bias for optimum performance.

The value of quiescent drain current (I_{DQ}) is not critical for many applications. The MRF136Y was characterized at $I_{DQ} = 25$ mA, which is the suggested minimum value of I_{DQ} . For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple

resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of the MRF136Y may be controlled from its rated value down to zero (negative gain) by varying the dc gate voltage. This feature facilitates the design of manual gain control, AGC/ALC and modulation systems. (See Figure 9.)

AMPLIFIER DESIGN

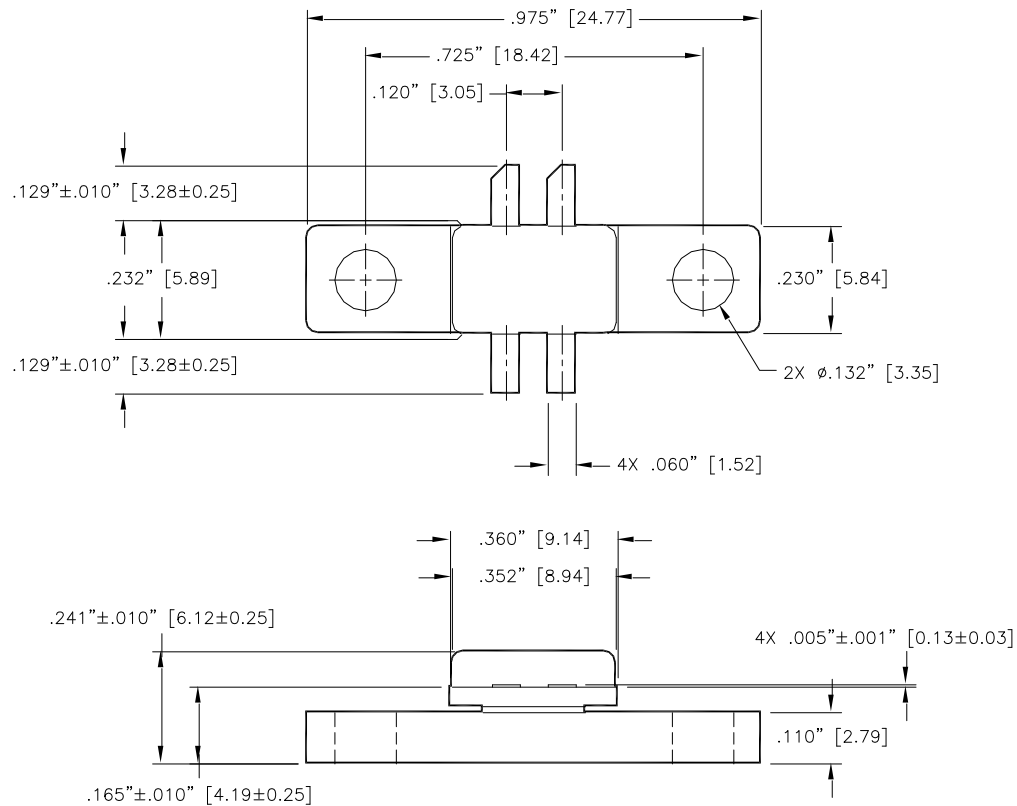
Impedance matching networks similar to those used with bipolar VHF transistors are suitable for MRF136Y. See M/A-COM Application Note AN721, Impedance Matching Networks Applied to RF Power Transistors. The higher input impedance of RF MOS FETs helps ease the task of broadband network design. Both small signal scattering parameters and large signal impedances are provided. While the s-parameters will not produce an exact design solution for high power operation, they do yield a good first approximation. This is an additional advantage of RF MOS power FETs.

RF power FETs are triode devices and, therefore, not unilateral. This, coupled with the very high gain of the MRF136Y, yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt resistive loading, or output to input feedback. Two port parameter stability analysis with the MRF136Y s-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See M/A-COM Application Note AN215A for a discussion of two port network theory and stability.

LOW NOISE OPERATION

Input resistive loading will degrade noise performance, and noise figure may vary significantly with gate driving impedance. A low loss input matching network with its gate impedance optimized for lowest noise is recommended.

Outline Drawing



Unless otherwise noted, tolerances are inches \pm .005" [millimeters \pm 0.13mm]

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