# 8-Ch, 24-Bit Simultaneous Sampling ADC

Preliminary Technical Data

# AD7771

## FEATURES

- 8 Channel 24-Bit Simultaneous Sampling ADCs
- Sample Rate Converter (SRC) for coherent sampling
- Adjustable Phase Synchronization
- PGA per Channel (gain 1, 2, 4, 8)
- Low Input Bias Current: 6nA
- Single Ended or True Differential Inputs
- 128ksps Output Data Rate/per channel
- Internal 2.5V reference
- Optimize Power Dissipation & Performance
- Two Power Modes:
  - High Resolution Mode
  - Low Power Mode
- Low Latency Sinc3 and Sinc5 Filter Paths
- Low Resolution SAR ADC for System and Chip Diagnostics

## POWER SUPPLY

- Bipolar (±1.65V Supply) or Unipolar (3.3V Supply) Supply
- Digital/IO Supply 1.8V to 3.6V
- Performance Temperature range: –40°C to +105°C
- Functional Temperature range: –40°C to +125°C

## PERFORMANCE

- Combined AC & DC Performance
- 112dB SNR/Dynamic Range at 8 kSPS
- -108dB THD
- ±15ppm INL, ±250 uV Offset Error, ±0.1% Gain Error
- ±5 ppm/°C typ Internal Reference TempCo

## APPLICATIONS

- Power quality and Measurement Applications
- General Purpose Data Acquisition Applications
- Industrial Process Control Applications

## FUNCTIONAL BLOCK DIAGRAM

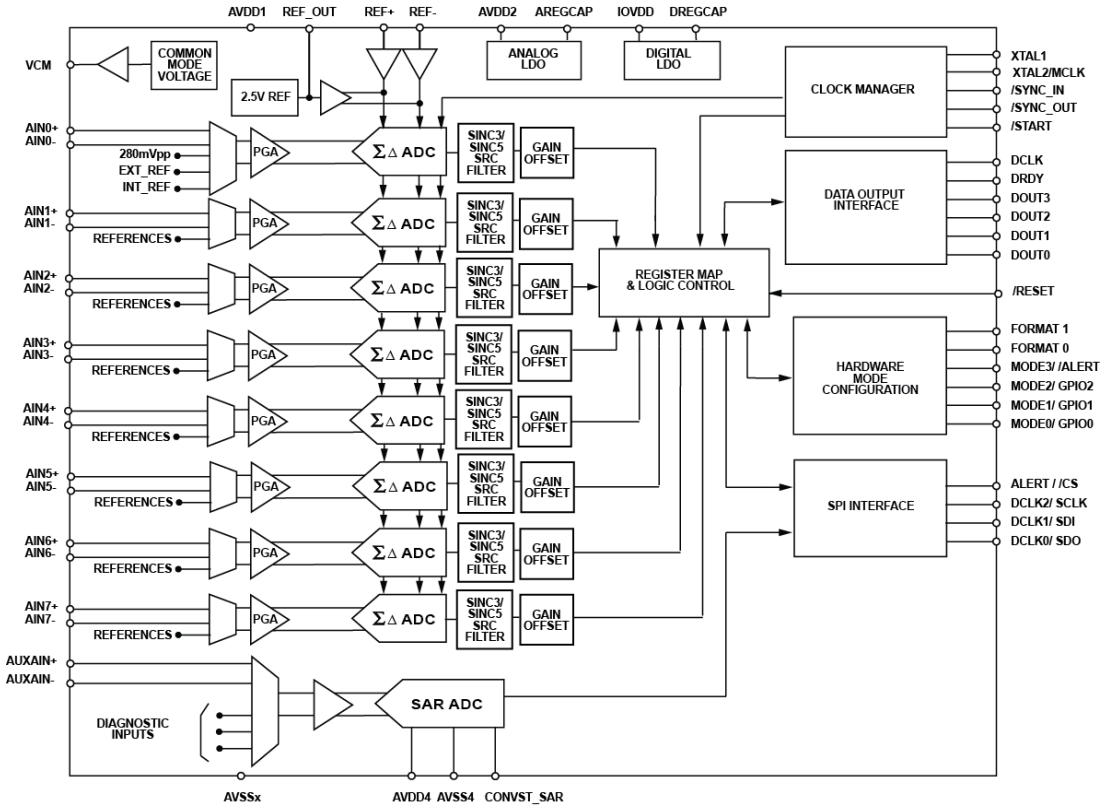


*Figure 1 AD7771 Functional Block Diagram*

**Rev. PrC**



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# AD7771* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD7771 Evaluation Board

## DOCUMENTATION

**Application Notes**

- AN-1388: Coherent Sampling for Power Quality Measurements Using the AD7779 24-Bit Simultaneous Sampling Sigma-Delta ADC
- AN-1392: How to Calculate Offset Errors and Input Impedance in ADC Converters with Chopped Amplifiers
- AN-1393: Translating System Level Protection and Measurement Requirements to ADC Specifications

**Data Sheet**

- AD7771: 8-Channel, 24-Bit Simultaneous Sampling ADCs Preliminary Data Sheet

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7770/AD7771/AD7779 - No-OS Driver

## TOOLS AND SIMULATIONS

- AD7770/AD7771/AD7779 Filter Model
- AD7771 CRC Calculator
- AD7770/AD7771/AD7779 IBIS Model

## REFERENCE MATERIALS

**Press**

- Analog Devices Improves Monitoring and Protection of Smart Grid Transmission and Distribution Equipment

## DESIGN RESOURCES

- AD7771 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD7771 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

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## GENERAL DESCRIPTION

The AD7771 is an 8-channel simultaneously sampled, Analog-to-Digital Converter. There are 8 full Sigma Delta ADCs on-chip. The AD7771 provides a high input impedance to allow for direct sensor connection. Each input channel has a programmable gain stage catering for gains of 1,2,4,8 to map lower amplitude sensor outputs into the Full Scale ADC input range to maximize the Dynamic Range of the signal chain. The Analog inputs can accept unipolar 0 to 2.4V or true bipolar ±1.25V analog input signals with 3.3V or ±1.65V Analog Supply voltages respectively. The Analog inputs can be configured to accept True Differential or Single-Ended signals to match different sensor output configurations.

Each channel contains an ADC modulator and Sinc 3/Sinc 5 low latency digital filters. A Sample Rate Converter (SRC) is provided to allow fine resolution control over the AD7771 Output Data Rate (ODR). This can be used in Power Quality Applications where the ODR resolution is required to maintain coherency with 0.01Hz changes in the line frequency. The SRC can be programmed through the SPI interface. The AD7771 implements two different interfaces, Data Output Interface and a SPI control Interface. The ADC Data Output interface is dedicated to transmitting the ADC conversion results from the AD7771 to the processor, acting as a master. The SPI interface is used to write to and read from the AD7771 configuration registers and for the control and reading of data from the SAR ADC. The SPI interface can also be configure to output the sigma delta conversion data.

The AD7771 includes a 12-Bit SAR ADC. This ADC can be used for AD7771 diagnostics without having to decommission one of the Sigma Delta ADC channels dedicated to system measurement functions. With the use of an external multiplexer and signal conditioning, the SAR ADC can be used to validate the Sigma Delta ADC measurements in applications where Functional Safety is required. In addition, the AD7771 offers three GPIOs that can be used to control an external multiplexer.

The AD7771 contains a 2.5V reference and reference buffer. The reference has a temperature co-efficient of 20 ppm/°C max.

The AD7771 offers two modes of operation: High Resolution Mode and Low Power Mode. The High Resolution mode provides higher dynamic range while consuming 13 mW/ch and the Low Power mode consumes just 5 mW/ch at a reduced dynamic range specification.

The specified operating temperature range is -40°C to +105°C while the part is operational up to +125°C.

Input referred noise for SINC 3 and SINC5 filters,

SINC5

| ODR | BW | Gain1(uVrms/uVpp) | Gain2(uVrms/uVpp) | Gain4(uVrms/uVpp) | Gain8(uVrms/uVpp) |
|---|---|---|---|---|---|
| 128k | 26098 | 30.20 | 22.80 | 19.20 | 17.20 |
| 64k | 14122 | 13.70 | 10.10 | 8.28 | 7.46 |
| 32k | 7215 | 7.40 | 4.79 | 3.63 | 3.14 |
| 16k | 3627.5 | 4.65 | 2.74 | 1.87 | 1.54 |
| 8k | 1816.2 | 3.17 | 1.79 | 1.17 | 0.93 |
| 4k | 908.5 | 2.23 | 1.25 | 0.79 | 0.63 |

SINC3

| ODR | BW | Gain1(uVrms/uVpp) | Gain2(uVrms/uVpp) | Gain4(uVrms/uVpp) | Gain8(uVrms/uVpp) |
|---|---|---|---|---|---|
| 32k | 10045 | 11.91 | 7.00 | 4.79 | 3.84 |
| 16k | 5076.2 | 5.60 | 3.35 | 2.37 | 1.99 |
| 8k | 2545 | 3.64 | 2.10 | 1.42 | 1.15 |
| 4k | 1273.5 | 2.51 | 1.42 | 0.93 | 0.74 |
| 2k | 636.75 | 1.77 | 0.99 | 0.64 | 0.51 |
| 1k | 318.5 | 1.25 | 0.71 | 0.45 | 0.36 |

## SPECIFICATIONS

AVDD1x/AVSSx = ±1.65V, 3.3V/AGND, AVDD2 - AVSSx = 2.2 V to 3.6V; IOVDD = 2.3V to 3.6V; DGND = 0V, REF = 2.5 V internal/external, MCLK = 8192 kHz for High Resolution Mode and 4096 kHz for Low Power Mode, ODR = 128 kHz High Resolution (HR) Mode, ODR = 32 kHz Low Power (LP) Mode; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

**Table 1. Specification Table**

| Parameter | Test Conditions Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ANALOG INPUTS | | | | | |
| Differential Input Voltage Range | VREF = (REF+ − REF−) | | | ±VREF/$PGA_{GAIN}$ | V |
| Single-Ended Input Voltage Range | | 0 | | 0to VREF/ $PGA_{GAIN}$ | V |
| Common-Mode Input Range | | AVSS +0.10 | (AVDD1−AVSS)/2 | AVDD1 – 0.10 | V |
| Absolute AIN Voltage Limits | | AVSS +0.10 | | AVDD1 – 0.10 | |
| DC Input Current | HR, MCLK=8192 kHz | | ±6 | | nA |
| | LP, MCLK=4096 kHz | | ±2.5 | | nA |
| Differential Bias current | HR | | ±3 | | nA |
| | LP | | ±1 | | nA |
| Input Current Drift | | | TBD | | µA/°C |
| Input Capacitance | | | 8pF | | pF |
| PGA | | | | | |
| Gain Settings | | | 1,2,4,8 | | |
| Gain drift | | | ±3 | | ppm/°C |
| Bandwidth | Small Signal | | | 32 | kHz |
| | Large Signal HR Mode | | | 10 | kHz |
| | Large Signal LP Mode | | | 3 | kHz |
| REFERENCE | | | | | |
| INTERNAL | | | | | |
| Output Voltage | REF_OUT | −0.2% | 2.5 | +0.2% | V |
| Initial Accuracy | $T_A$ = 25°C | −5mV | REF_OUT | +5mV | V |
| Temperature Coefficient | -40°C < $T_A$ <+105°C | | ±5 | | ppm/°C |
| Reference Load Current | $I_L$ | −10 | | +10 | mA |
| DC Power Supply Rejection | (Line Regulation) | | 95 | | dB |
| Load Regulation | $\Delta V_{OUT}/\Delta I_L$ | | 100 | | µV/mA |
| Voltage Noise | $e_{N\ p-p}$ , 0.1 Hz to 10 Hz | | 6.8 | | µVrms |
| Voltage Noise Density | $e_N$ 1kHz, 2.5V Reference | | 273.5 | | nV/√Hz |
| Turn-On Settling Time | 100nF | | 1.5 | | ms |
| Long-Term Stability | 1000 hours | | TBD | | ppm |
| EXTERNAL | | | | | |
| Input Voltage | REF_IN = (REF+) – (REF−) | 1 | 2.5V | AVDD1x | V |
| Buffer Headroom | | AVSS + 0.1 | | AVDD1x−0.1 | |
| REF− Input Voltage | | | AVSS | AVDD1x−REFx+ | V |
| Average REF Current | Current per channel | | | | |
| | REF BUF DISABLED, HR mode | | 18 | | µA/V |
| | REF BUF PRE-Q, HR mode | | 200 | | nA/V |
| | REF BUF DISABLED, LP mode | | 4.5 | | µA/V |
| | REF BUF PRE-Q, LP mode | | 100 | | nA/V |
| | REF BUF ENABLED | | 120 | | nA/V |
| TEMPERATURE RANGE | | | | | |
| Specified Performance | $T_{MIN}$ to $T_{MAX}$ | −40 | | +105 | °C |

| Parameter | Test Conditions Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Functional | $T_{MIN}$ to $T_{MAX}$ | −40 | | +125 | °C |
| TEMPERTAURE SENSOR | | | | | |
| Accuracy | | | ±2 | | °C |
| DIGITAL FILTER RESPONSE | | | | | |
| SINC 3 | | | | | |
| Group Delay | | | See SCR details | | |
| Settling Time | | | See CRC details | | |
| Pass-Band | -0.1 dB | | See CRC details | | |
| | -3 dB | | See CRC details | | |
| Decimation Rate | | 16 | | 4095.99 | |
| SINC 5 | | | | | |
| Group Delay | | | See CRC details | | |
| Settling Time | | | See CRC details | | |
| Pass-Band | -0.1 dB | | See CRC details | | |
| | -3 dB | | See CRC details | | |
| Decimation Rate | | 16 | | 2048 | |
| CLOCK SOURCE | | | | | |
| Frequency | High Resolution Mode | TBD | | 8.192 | MHz |
| | Low Power Mode | TBD | | 4.096 | |
| Input Low Voltage, $V_{IL}$ | XTAL1 | | | 0.4 | V |
| | XTAL2 | | | | |
| Input High Voltage, $V_{IH}$ | XTAL1 | TBD | | | V |
| | XTAL2 | | | | |
| Duty Cycle | | 45:55 | 50:50 | 55:45 | % |
| Input Current | | −10 | | +10 | µA |
| ΣΔ ADC | | | | | |
| SPEED & PERFORMANCE | | | | | |
| Resolution | | 24 | | | Bits |
| Output Data Rate (ODR) | High Resolution Mode | | | 128 | kSPS |
| | Low Power Mode | | | 32 | kSPS |
| No Missing Code | ODR < 25ksps | 24 | | | |
| Noise | Shorted input | | | | |
| | SINC5 | | | | |
| | High Resolution Mode | | 70 | | nV/√ Hz |
| | Low Power Mode | | 160 | | nV/√ Hz |
| | SINC3 | | | | |
| | High Resolution Mode | | 85 | | nV/√ Hz |
| | Low Power Mode | | 190 | | nV/√ Hz |
| AC ACCURACY | | | | | |
| Dynamic Range | Shorted inputs | | | | dB |
| | SINC5 | | | | |
| | 128 kSPS, HR Mode | | 96 | | |
| | 32 kSPS, HR Mode, | | 103 | | |
| | 32 kSPS, LP Mode | | 96 | | |
| | 8 kSPS, LP Mode | | 104 | | |
| | SINC3 | | | | |
| | 16 kSPS, HR Mode | | 103 | | |
| | 4 kSPS, HR Mode | | 115 | | |

| Parameter | Test Conditions Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | 8 KSPS, LP Mode | | 110 | | |
| | 2 KSPS, LP Mode, | | 118 | | |
| THD | HR | | -109 | | dB |
| | LP | | -106 | | |
| SINAD | | | 106 | | |
| SFDR | | | 107 | | dB |
| IMD | $f_A$ = 50 Hz, $f_B$ = 51 Hz, HR | | 125 | | dB |
| | $f_A$ = 50 Hz, $f_B$ = 51 Hz, LP | | 105 | | |
| DC Power Supply Rejection | AVDD1x = 3.3V | | -90 | | dB |
| DC Common Mode Rejection Ratio | | 80 | | | dB |
| Crosstalk | Up to 2 kHz input. Reference Buffer Full mode | | -110 | | dB |
| DC ACCURACY | | | | | |
| Integral Nonlinearity | End Point Method | | ±7 | ±15 | ppm/FSR |
| Offset Error | | | ±40 | ±250 | µV |
| Offset Error Drift | | | ±0.5 | | µV/°C |
| | Versus Time | | TBD | | nV/1000 hrs |
| Offset Matching | | | 30 | | µV |
| Gain Error | $PGA_{GAIN}$ = 1 | | | ±0.1% | FS |
| Gain Drift vs. Temperature | | | 150 | | ppm/°C |
| Gain Matching | | | ±0.1 | | % |
| SAR ADC | | | | | |
| SPEED & PERFORMANCE | | | | | |
| Resolution | | | 12 | | Bits |
| Analog Input Range | | AVSS4+0.1 | | AVDD4-0.1 | V |
| Analog Input Common Mode Range | | AVSS4+0.1 | (AVDD4-AVSS4)/2 | AVDD4-0.1 | V |
| Analog Input Leakage Current | | | ±10 | | nA |
| Throughput | | | 256 | | kSPS |
| TUE | | | | | |
| DC ACCURACY | Differential Mode | | | | |
| INL | | | | | LSB |
| DNL | No Missing codes (12 bit) | | 1.5 | | LSB |
| Offset | | | 1 | | LSB |
| Gain | | | 0.6 | | LSB |
| TUE | | | TBD | | LSB |
| AC PERFORMANCE | | | | | |
| SNR | 1 kHz | | 66 | | dB |
| THD | 1 kHz | | -83 | | dB |
| VCM PIN | | | | | |
| Output | | | (AVDD1−AVSS)/2 | | V |
| Load Current | $I_L$ | | 1 | | mA |
| Load Regulation | $\Delta V_{OUT}/\Delta I_L$ | | 12 | | µV/mA |
| Short Circuit Current | | | 5 | | mA |
| LOGIC INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | 1.65V≤ IOVDD ≤1.95V | 0.65×IOVDD | | | V |

| Parameter | Test Conditions Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| | 2.3V≤ IOVDD ≤3.6V | 0.7× IOVDD | | | V |
| Input Low Voltage, $V_{INL}$ | 1.65V≤ IOVDD ≤1.95V | | | 0.35× IOVDD | V |
| | 2.3V≤ IOVDD ≤3.6V | | | 0.4 | V |
| Hysteresis[2] | | | 0.2 | | % |
| | IOVDD <2.7V | | 0.1 | | % |
| Input Currents | | -10 | | +10 | µA |
| LOGIC OUTPUT (DOUT/$\overline{RDY}$, DCLK, SDOUT, GPIO) | | | | | |
| Output High Voltage, $V_{OH}$ | IOVDD ≥ 3V, $I_{SOURCE}$ = 1mA | 0.8× IOVDD | | | V |
| | 2.3≤IOVDD< 3V, $I_{SOURCE}$ 500µA | 0.8× IOVDD | | | V |
| | IOVDD <2.3V, $I_{SOURCE}$ = 200µA | 0.8× IOVDD | | | V |
| Output Low Voltage, $V_{OL}$ | IOVDD ≥3V, $I_{SINK}$ 2mA | | | 0.4 | V |
| | 2.3≤IOVDD <3V, $I_{SINK}$ 1mA | | | 0.4 | V |
| | IOVDD < 2.3V, $I_{SINK}$ 100µA | | | 0.4 | V |
| Leakage Current | Floating State | -10 | | +10 | µA |
| Output Capacitance | Floating State | | 10 | | pF |
| ΣΔ Data Output Coding | | | 2s Comp | | |
| SAR Data Output Coding | | | Binary | | |
| | | | | | |
| POWER SUPPLIES | All ΣΔ Channels Enabled CMOS clock, AVDD1x/AVDD2x/AVDD4 = 3.3v, IOVDD = 1.8v | | | | |
| AVDD1x – AVSS | | 3.0 | | 3.6 | V |
| I_AVDD1x[1 2] | Reference Buffer Pre-Q , VCM Enable, Internal reference Enable | | | | |
| | HR | | 17 | | |
| | LP | | 4.5 | | mA |
| | Reference Buffer Enable, VCM Enabled, Internal reference Enabled | | | | mA |
| | HR | | 19 | | |
| | LP | | 5 | | mA |
| | Reference Buffer Disable, VCM disabled, Internal reference Disabled | | | | mA |
| | HR | | 13 | | |
| | LP | | 3.5 | | mA |
| AVDD2 – AVSS | | 2.2 | | 3.6 | V |
| I_AVDD2x | HR | | 9 | | mA |
| | LP | | 3.5 | | mA |
| AVDD4 – AVSS4 | | AVDD1x | | 3.6 | |
| IAVDD4 | SAR enable, 256ksps | | 1.6 | | mA |
| | SAR disable | | 0.05 | | uA |
| AVSS-DGND | | -1.8 | | 0 | V |

| Parameter | Test Conditions Comment | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| IOVDD – DGND | | 2 | | 3.6 | V |
| I_IOVDD | CMOS clock, HR | | 7.5 | | mA |
| | CMOS clock, LP | | 2.5 | | |
| Power Dissipation | Reference Buffers PreQ, VCM Enabled, Internal reference Disabled, Osc Enabled, SAR Disabled | | | | |
| | HR | | 99 | | mW |
| | LP | | 31.5 | | mW |
| | Reference Buffers Off, VCM Disabled, Internal reference Disabled, Osc Disabled, SAR Disabled | | | | |
| | HR | | 85.5 | | mW |
| | LP | | 27.5 | | mW |
| Power Down | All ADC's disable | | TBD | | Mw |

[1] AVDDx = 3.3V, AVSSx = GND, IOVDD = 1.8V, CMOS clock
[2] Disabling either VCM or Internal Reference would lead to a 40uA current consumption reduction

## ABSOLUTE MAXIMUM RATINGS

**Table 2. Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| AVDDx to AVSSx | −0.3 V to +3.96V |
| AVSSx to DGND | −1.98 V to +0.3 V |
| ARegxCap to AVSSx | −0.3 V to +1.98V |
| DRegCap to DGND | −0.3 V to +1.98V |
| IOVDD to DGND | −0.3 V to +3.96V |
| IOVDD to AVSSx | −0.3 V to +5.94 V |
| AVSS4 to AVSSx | AVDD1x −0.3 V to +3.96V |
| Analog Input Voltage | AVSSx− 0.3 V to AVDD1x+0.3 V or +3.96V (whichever is less) |
| Refx Input Voltage | AVSSx− 0.3 V to AVDD1x+0.3 V or +3.96V (whichever is less) |
| AUXIN+/AUXIN- | AVSSx− 0.3 V to AVDD4+0.3 V or +3.96V (whichever is less) |
| Digital Input Voltage to DGND | DGND − 0.3 V to IOVDD + 0.3 V or +3.96V (whichever is less) |
| Digital Output Voltage to DGND | DGND− 0.3 V to IOVDD + 0.3 V or +3.96V (whichever is less) |
| XTAL1 to DGND | DGND −0.3 V to DRegCap +0. 3V or +1.98V (whichever is less) |
| Ain/Digital Input Current | TBD mA |
| Operating Temperature Range | −40°C to +125°C |
| Junction Temperature, ($T_J$ maximum) | +150°C |
| Storage temperature Range | −65°C to +150°C |
| Reflow soldering | 260°C |
| ESD | 2kV |
| FICDM | |
| Corner pins (1, 16, 17, 32, 33, 48, 49, 64) | +750V |
| Others | +500V |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

**Table 3. Thermal Resistance**

| Package Type | $\theta_{ja}$ | $\theta_{Jb}$ | $\Psi_{jt}$ | $\Psi_{jb}$ | UNITS |
|---|---|---|---|---|---|
| 64-CP-15[1] | 30.43 | | 0.13 | 6.59 | °C/W |
| 64-CP-15[2] | 22.62 | 3.17 | 0.09 | 3.19 | °C/W |

1- Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no thermal vias. See JEDEC JESD51.
2- Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with 49 thermal vias. See JEDEC JESD51.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

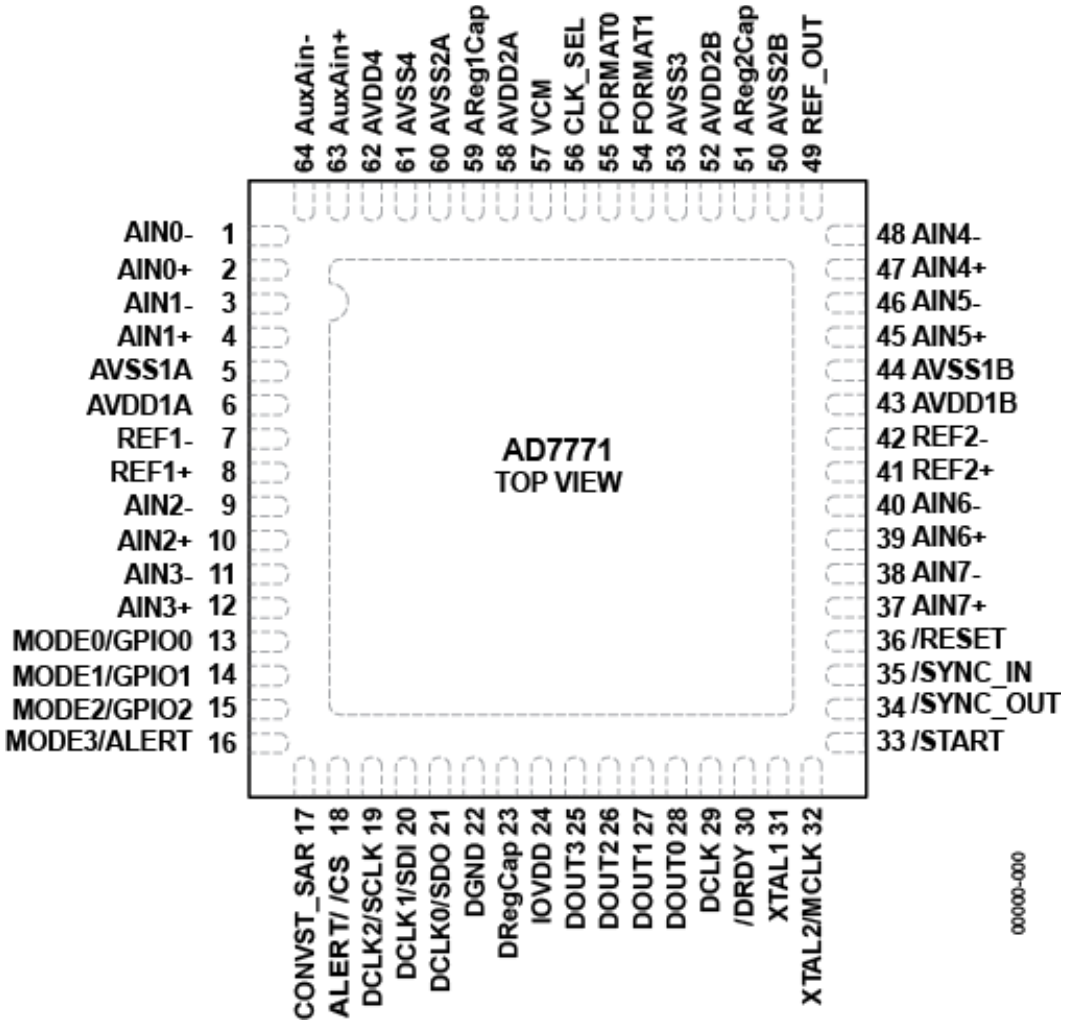


*Figure 2. Pin Description*

**Table 4. Pin Description**

| Pin No. | Mnemonic | Type | Direction | Description |
|---|---|---|---|---|
| 1 | AIN0- | Analog Input | Input | Analog Input Channel 0 |
| 2 | AIN0+ | Analog Input | Input | Analog Input Channel 0 |
| 3 | AIN1− | Analog Input | Input | Analog Input Channel 1 |
| 4 | AIN1+ | Analog Input | Input | Analog Input Channel 1 |
| 5 | AVSS1A | Supply | Supply | Negative Front End Analog Supply for Channels 0 to 3, typical −1.65V(Dual Supply), and AGND (Single Supply). Connect all AVSSx pins to the same potential |
| 6 | AVDD1A | Supply | Supply | Positive Front End Analog Supply for Channels 0 to 3, typical AVSSx + 3.3V. This pin should be connected together with AVDD1B. |
| 7 | REF1− | Reference | Input | Negative Reference Input for Channels 0 to 3, typical AVSSx. Connect all REFx− pins to the same potential |
| 8 | REF1+ | Reference | Input | Positive Reference Input 1 for Channels 0 to 3, typical REF1− +2.5V |
| 9 | AIN2− | Analog Input | Input | Analog Input Channel 2 |
| 10 | AIN2+ | Analog Input | Input | Analog Input Channel 2 |
| 11 | AIN3− | Analog Input | Input | Analog Input Channel 3 |
| 12 | AIN3+ | Analog Input | Input | Analog Input Channel 3 |
| 13 | MODE0/GPIO0 | Digital I/O | IO | PIN Control Mode: MODE0 input pin,<br>SPI Control Mode: Configurable GPIO0. If this pin is not used, connect to DGND or IOVDD. |
| 14 | MODE1/GPIO1 | Digital I/O | IO | PIN Control Mode: MODE1 input pin<br>SPI Control Mode: Configurable GPIO1. If this pin is not used, connect to DGND or IOVDD. |
| 15 | MODE2/GPIO2 | Digital I/O | IO | PIN Control Mode: MODE2 input pin,<br>SPI Control Mode: Configurable GPIO2. If this pin is not used, connect to DGND or IOVDD. |
| 16 | MODE3/ALERT | Digital I/O | IO | PIN Control Mode: MODE3 input pin,<br>SPI Control Mode: Alert Output Pin |
| 17 | CONVST_SAR | Digital Input | Input | Pin Control Mode – ΣΔ output interface selection<br>SPI Control Mode - SAR Convert Start |
| 18 | ALERT/$\overline{CS}$ | Digital Input | Input | PIN Control Mode: Alert Output Pin<br>SPI Control Mode: Chip Select |
| 19 | DCLK2 / SCLK | Digital Input | Input | PIN Control Mode: DCLK frequency selection,<br>SPI Control Mode: SPI Clock. |
| 20 | DCLK1 / SDI | Digital Input | Input | PIN Control Mode: DCLK frequency selection<br>SPI Control Mode: SPI Data In. Connect this pin to DGND if the part is configured in Pin Contro Mode with SPI as data output interface |
| 21 | DCLK0 / SDO | Digital Output | Output | PIN Control Mode: DCLK frequency selection<br>SPI Control Mode: SPI Data Out |
| 22 | DGND | Supply | Supply | Digital ground |
| 23 | DREGCAP | Supply | Output | Digital LDO output. Decouple to DGND with 1uF cap |
| 24 | IOVDD | Supply | Supply | IO Digital levels and DLDO supply, from 1.8V to 3.6V. IOVDD should not be lower than DRegCap. |
| 25 | DOUT3 | Digital Output | IO | Data output pin 3. If the part is configured in daisy-chain mode, this pin acts as an input pin. |

| Pin No. | Mnemonic | Type | Direction | Description |
|---|---|---|---|---|
| 26 | DOUT2 | Digital Output | IO | Data output pin 2. If the part is configured in daisy-chain mode, this pin acts as an input pin. |
| 27 | DOUT1 | Digital Output | Output | Data output pin 1 |
| 28 | DOUT0 | Digital Output | Output | Data output pin 0 |
| 29 | DCLK | Digital Output | Output | Data Output Clock |
| 30 | $\overline{\text{DRDY}}$ | Digital Output | Output | Data Output Ready |
| 31 | XTAL1 | Clock | Input | XTAL1 input connection, If CMOS is used as a clock source, connect tie this pin to DGND. |
| 32 | XTAL2/MCLK | Clock | Input | XTAL2 input connection or CMOS clock |
| 33 | $\overline{\text{START}}$ | Digital Input | Input | Synchronization pulse. This pin is used to synchronize internally an external $\overline{\text{START}}$ asynchronous pulse with MCLK. The synchronize signal is shift out by $\overline{\text{SYNC\_OUT}}$ pin.Tie to DGND is not used. |
| 34 | $\overline{\text{SYNC\_OUT}}$ | Digital Output | Input | Synchronization signal. This pin generates a synchronous pulse |
| 35 | $\overline{\text{SYNC\_IN}}$ | Digital Input | Input | $\overline{\text{SYNC\_IN}}$ reset the internal SINC filters. |
| 36 | $\overline{\text{RESET}}$ | Digital Input | Input | Asynchronous Reset Pin. Resets all registers to default value. I |
| 37 | AIN7+ | Analog Input | Input | Analog Input Channel 7 |
| 38 | AIN7– | Analog Input | Input | Analog Input Channel 7 |
| 39 | AIN6+ | Analog Input | Input | Analog Input Channel 6 |
| 40 | AIN6– | Analog Input | Input | Analog Input Channel 6 |
| 41 | REF2+ | Reference | Input | Positive Reference Input 1 for Channels 4 to 7, recommended value REF2– + 2.5V |
| 42 | REF2– | Reference | Input | Negative Reference Input for Channels 4 to 7, typically AVSSx. Connect all REFx– pins to the same potential |
| 43 | AVDD1B | Supply | Supply | Positive Front End Analog Supply for Channels 4 to 7. This pin should be connected together with AVDD1A |
| 44 | AVSS1B | Supply | Supply | Negative Front End Analog Supply for Channels 4 to 7, typical -1.65V(Dual Supply) or AGND (Single Supply). Connect all AVSSx pins together |
| 45 | AIN5+ | Analog Input | Input | Analog Input Channel 5 |
| 46 | AIN5– | Analog Input | Input | Analog Input Channel 5 |
| 47 | AIN4+ | Analog Input | Input | Analog Input Channel 4 |
| 48 | AIN4– | Analog Input | Input | Analog Input Channel 4 |
| 49 | REF_OUT | Reference | Output | 2.5V Reference Output |
| 50 | AVSS2B | Supply | Supply | Negative Analog supply. Connect all AVSSx pins together. |
| 51 | AReg2Cap | Supply | Output | Analog LDO output. Decouple to AVSS2 with 1uF cap |
| 52 | AVDD2B | Supply | Supply | Positive Analog supply, this pin should be connected together with AVDD2A |
| 53 | AVSS3 | Supply | Supply | Negative Analog Ground. Connect all AVSSx pins together |
| 54 | FORMAT1 | Digital Input | Input | Output data frame, |
| 55 | FORMAT0 | Digital Input | Input | Output data frame, |
| 56 | CLK_SEL | Digital Input | Input | Select Clock Source, |
| 57 | VCM | Analog Output | Output | Common Mode Voltage Output, $(AVDD1-AVSS)/2$ |
| 58 | AVDD2A | Supply | Input | Analog supply, from 2.2V to 3.6V. AVSS2x should not be lower than ARegxCap. AVSS2x should not be lower than ARegxCap.Connected This pin should be connected together with AVDD2B |
| 59 | AReg1Cap | Supply | Output | Analog LDO output. Decouple to AVSS with 1uF cap. |

| Pin No. | Mnemonic | Type | Direction | Description |
|---|---|---|---|---|
| 60 | AVSS2B | Supply | Input | Negative Analog supply. Connect all AVSSx together |
| 61 | AVSS4 | Supply | Supply | Negative SAR Analog Supply and reference. Connect all AVSSx together |
| 62 | AVDD4 | Supply | Supply | Positive SAR Analog Supply and Reference source, supply range from AVDD1x to 3.6V |
| 63 | AuxAin+ | Analog Input | Input | SAR Analog Input Channel |
| 64 | AuxAin- | Analog Input | Input | SAR Analog Input Channel |



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