

# FDD6N50/FDU6N50

## 500V N-Channel MOSFET

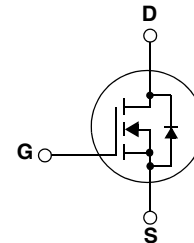
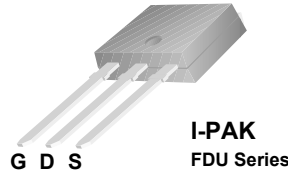
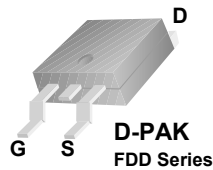
### Features

- 6A, 500V,  $R_{DS(on)} = 0.9\Omega$  @  $V_{GS} = 10$  V
- Low gate charge ( typical 12.8 nC)
- Low  $C_{rss}$  ( typical 9 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies and active power factor correction.



### Absolute Maximum Ratings

Symbol	Parameter	FDD6N50/FDU6N50	Unit
$V_{DSS}$	Drain-Source Voltage	500	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	6
		- Continuous ( $T_C = 100^\circ\text{C}$ )	3.8
$I_{DM}$	Drain Current - Pulsed (Note 1)	24	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	270	mJ
$I_{AR}$	Avalanche Current (Note 1)	6	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	8.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	- Derate above $25^\circ\text{C}$	89
			0.71
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Min.	Max.	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	83	$^\circ\text{C}/\text{W}$

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD6N50	FDD6N50TM	D-PAK	380mm	16mm	2500
FDD6N50	FDD6N50TF	D-PAK	380mm	16mm	2000
FDU6N50	FDU6N50TU	I-PAK	-	-	70

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted

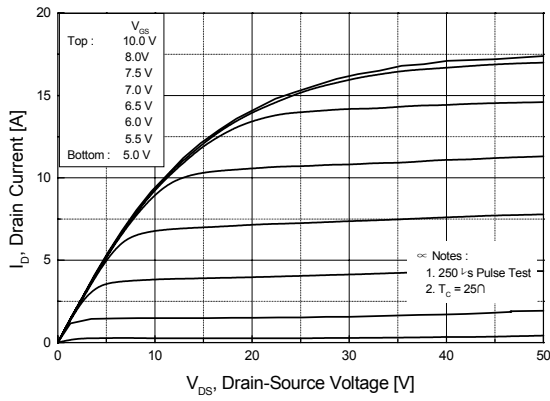
Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	500	--	--	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu A$ , Referenced to 25°C	--	0.5	--	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500V, V_{GS} = 0V$ $V_{DS} = 400V, T_C = 125^\circ C$	--	--	1 10	$\mu A$ $\mu A$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30V, V_{DS} = 0V$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30V, V_{DS} = 0V$	--	--	-100	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10V, I_D = 3A$	--	0.76	0.9	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40V, I_D = 3A$ (Note 4)	--	2.5	--	S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	--	720	940	pF
$C_{oss}$	Output Capacitance		--	95	190	pF
$C_{rss}$	Reverse Transfer Capacitance		--	9	13.5	pF
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250V, I_D = 6A$ $R_G = 25\Omega$	--	6	20	ns
$t_r$	Turn-On Rise Time		--	55	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	25	60	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	35	80
$Q_g$	Total Gate Charge	$V_{DS} = 400V, I_D = 6A$ $V_{GS} = 10V$	--	12.8	16.6	nC
$Q_{gs}$	Gate-Source Charge		--	3.7	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	5.8	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain-Source Diode Forward Current		--	--	6	A
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current		--	--	24	A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 6A$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0V, I_S = 6A$ $di_f/dt = 100A/\mu s$	--	275	--	ns
$Q_{rr}$	Reverse Recovery Charge		(Note 4)	--	1.7	--

### NOTES:

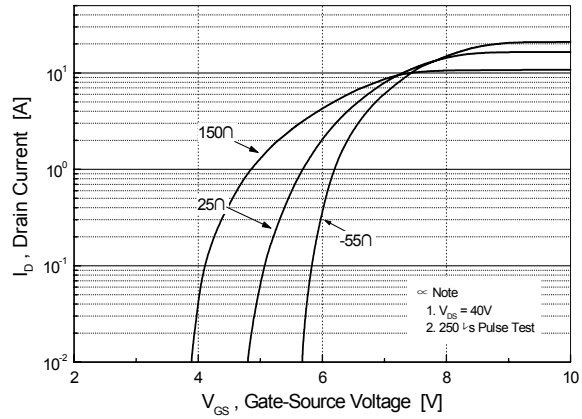
1. Repetitive Rating: Pulse width limited by maximum junction temperature
2.  $I_{AS} = 6A, V_{DD} = 50V, L = 13.5mH, R_G = 25\Omega$ , Starting  $T_J = 25^\circ C$
3.  $I_{SD} \leq 6A, di/dt \leq 200A/\mu s, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ C$
4. Pulse Test: Pulse width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$
5. Essentially Independent of Operating Temperature Typical Characteristics

## Typical Performance Characteristics

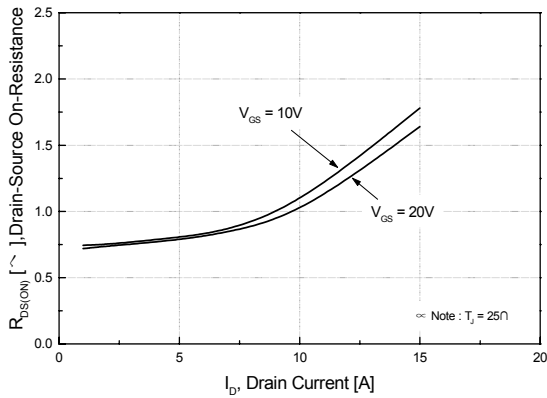
**Figure 1. On-Region Characteristics**



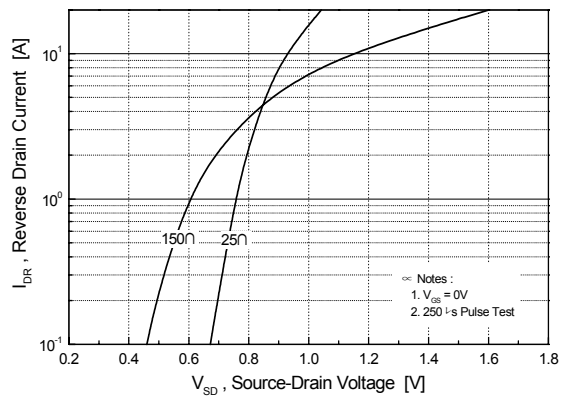
**Figure 2. Transfer Characteristics**



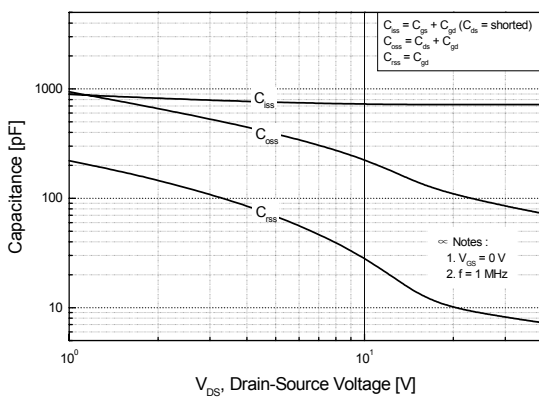
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



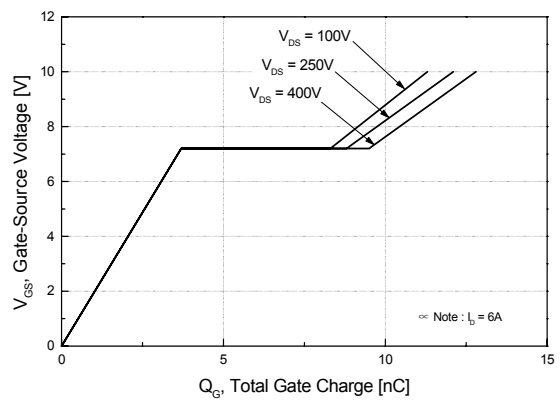
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**

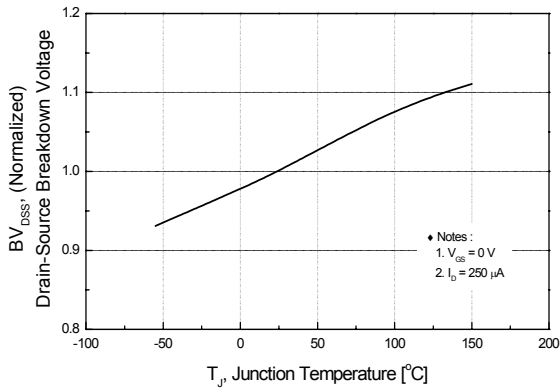


**Figure 6. Gate Charge Characteristics**

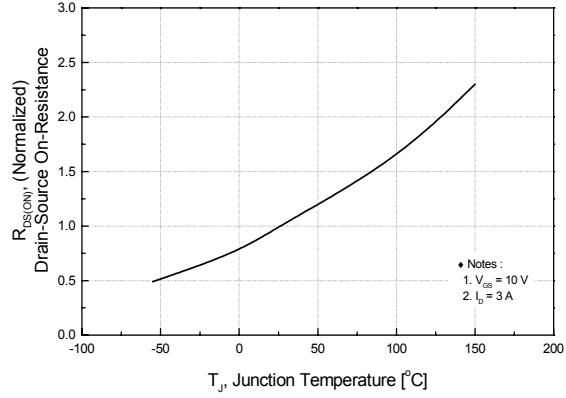


## Typical Performance Characteristics (Continued)

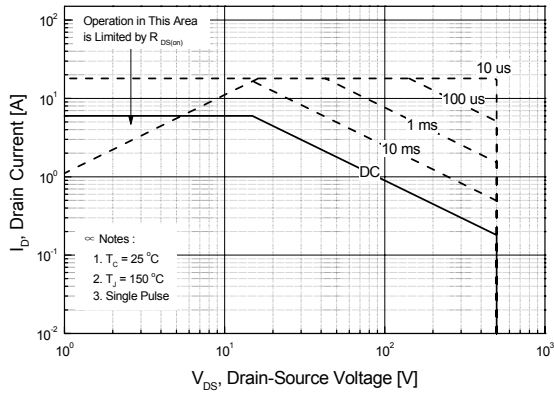
**Figure 7. Breakdown Voltage Variation vs. Temperature**



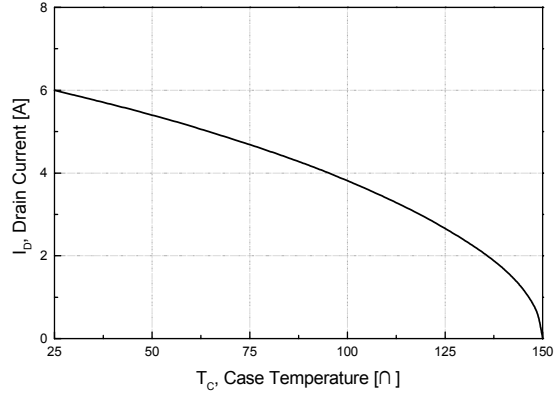
**Figure 8. On-Resistance Variation vs. Temperature**



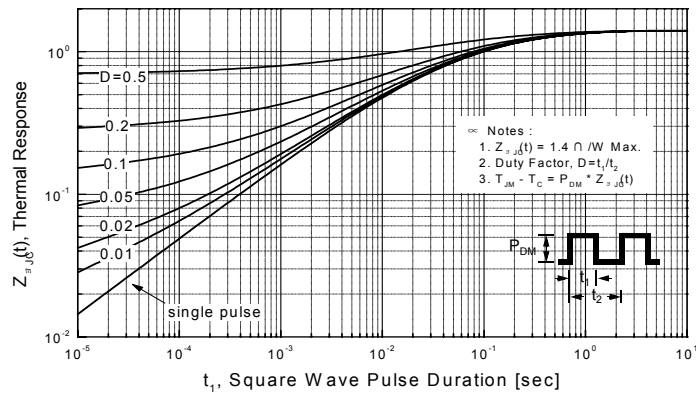
**Figure 9. Maximum Safe Operating Area**



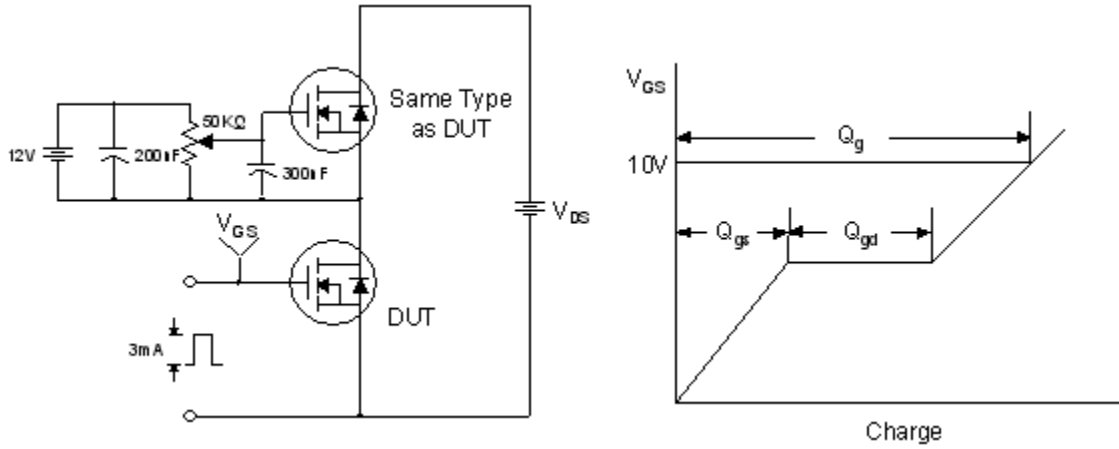
**Figure 10. Maximum Drain Current vs. Case Temperature**



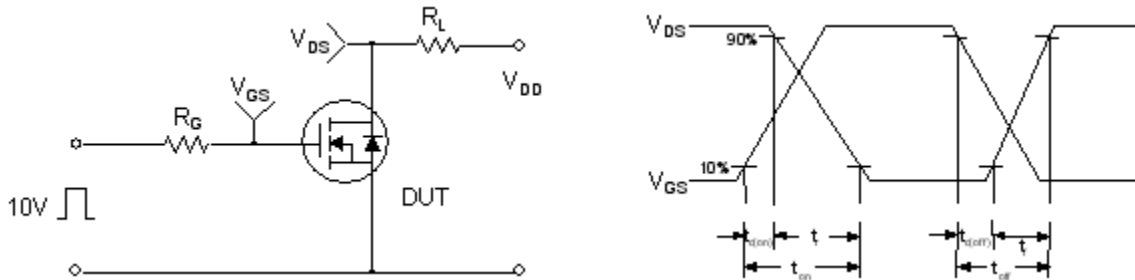
**Figure 11. Transient Thermal Response Curve**



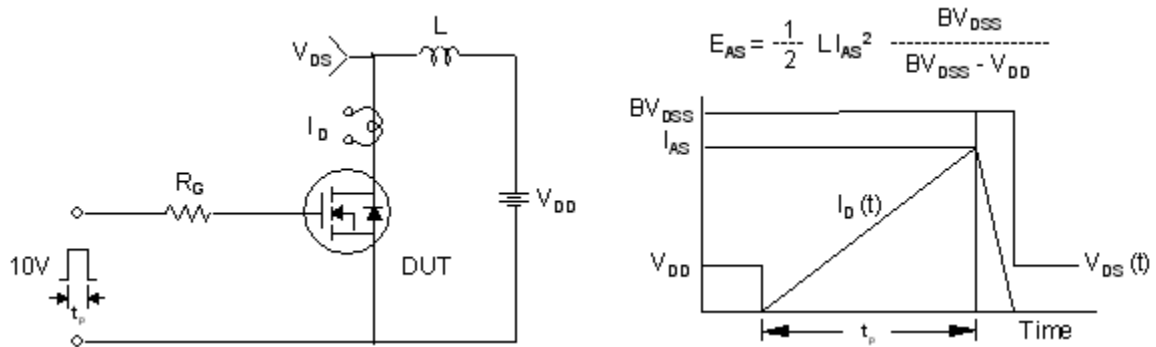
**Gate Charge Test Circuit & Waveform**



**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**

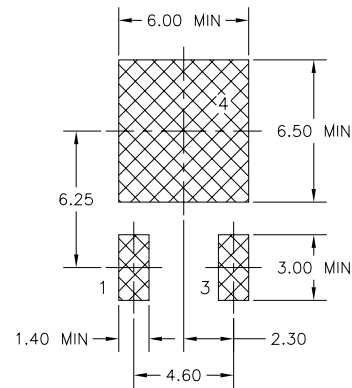
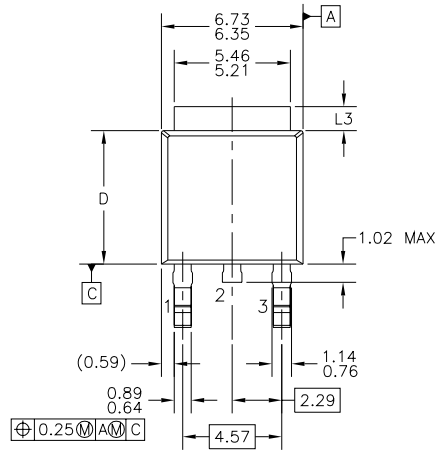


**Peak Diode Recovery dv/dt Test Circuit & Waveforms**

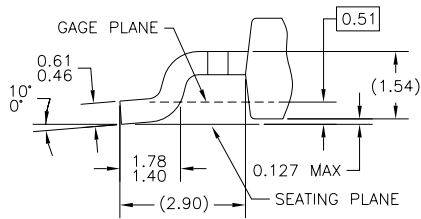
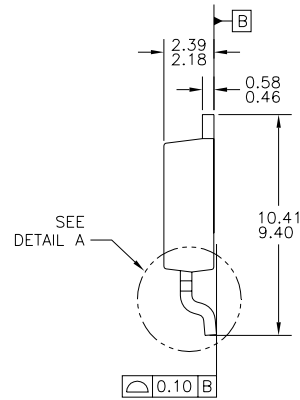
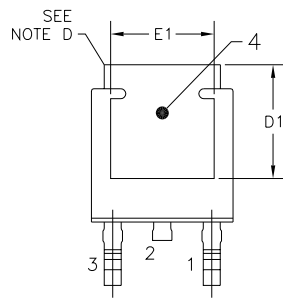


# Mechanical Dimensions

## D-PAK



LAND PATTERN RECOMMENDATION



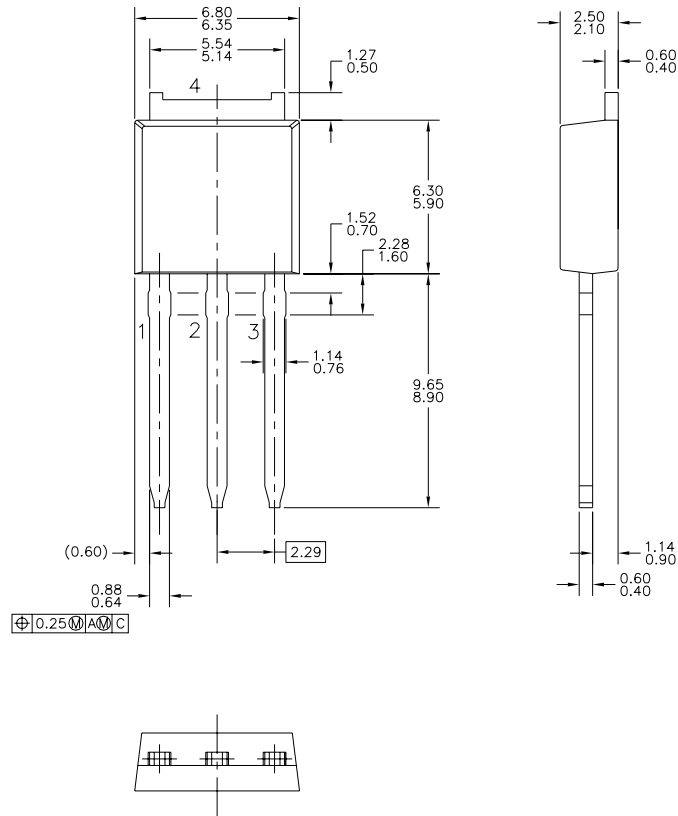
DETAIL A  
(ROTATED -90°)  
SCALE: 12X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
  - B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
  - C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
  - D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
  - E) DIMENSIONS L3,D,E1&D1 TABLE:
- |    | OPTION AA | OPTION AB |
|----|-----------|-----------|
| L3 | 0.89-1.27 | 1.52-2.03 |
| D  | 5.97-6.22 | 5.33-5.59 |
| E1 | 4.32 MIN  | 3.81 MIN  |
| D1 | 5.21 MIN  | 4.57 MIN  |
- F) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

Dimensions in Millimeters

Mechanical Dimensions (Continued)

I-PAK



Dimensions in Millimeters



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Build it Now™	FRFET™	MicroFET™	QS™	TCM™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TinyLogic®
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	TINYOPTO™
DOME™	HiSeC™	MSX™	RapidConfigure™	TruTranslation™
EcoSPARK™	I <sup>2</sup> C™	MSXPro™	RapidConnect™	UHC™
E <sup>2</sup> C MOS™	i-Lo™	OCX™	μSerDes™	UltraFET®
EnSigna™	ImpliedDisconnect™	OCXPro™	ScalarPump™	UniFET™
FACT™	IntelliMAX™	OPTOLOGIC®	SILENT SWITCHER®	VCX™
FACT Quiet Series™		OPTOPLANAR™	SMART START™	Wire™
Across the board. Around the world.™		PACMAN™	SPM™	
The Power Franchise®		POP™	Stealth™	
Programmable Active Droop™		Power247™	SuperFET™	
		PowerEdge™	SuperSOT™-3	

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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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