

AK4384

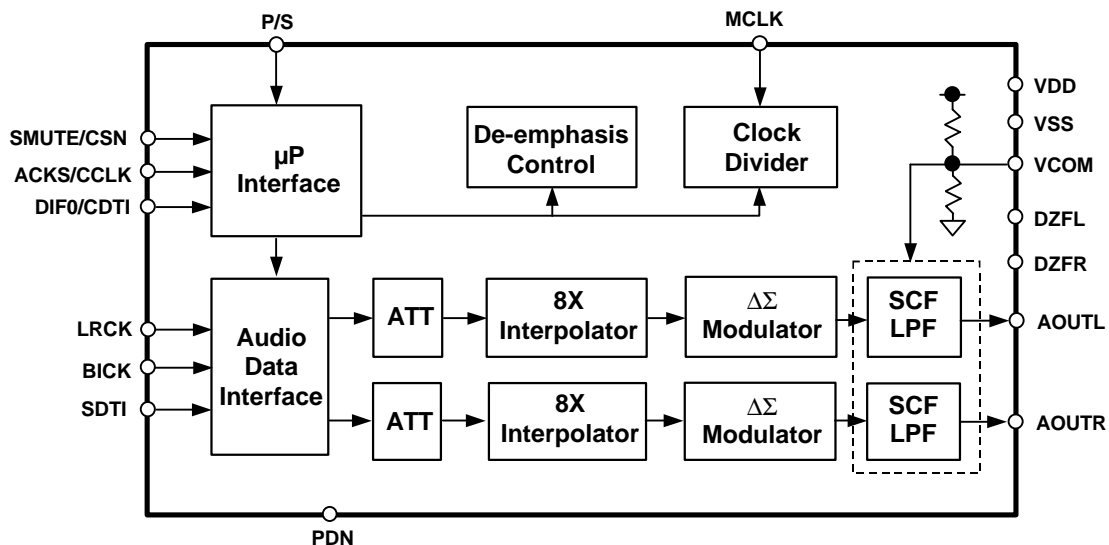
106dB 192kHz 24-Bit 2ch $\Delta\Sigma$ DAC

GENERAL DESCRIPTION

The AK4384 offers the perfect mix for cost and performance based audio systems. Using AKM's multi bit architecture for its modulator the AK4384 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4384 integrates a combination of SCF and CTF filters increasing performance for systems with excessive clock jitter. The 24 Bit word length and 192kHz sampling rate make this part ideal for a wide range of applications including DVD-Audio. The AK4384 is offered in a space saving 16pin TSSOP package.

FEATURES

- Sampling Rate Ranging from 8kHz to 192kHz
- 128 times Oversampling (Normal Speed Mode)
- 64 times Oversampling (Double Speed Mode)
- 32 times Oversampling (Quad Speed Mode)
- 24-Bit 8 times FIR Digital Filter
- SCF with High Tolerance to Clock Jitter
- 2nd order Analog LPF
- Single Ended Output Buffer
- Digital de-emphasis for 32k, 44.1k and 48kHz sampling
- Soft mute
- Digital Attenuator (Linear 256 steps)
- I/F format: 24-Bit MSB justified, 24/20/16-Bit LSB justified or I²S
- Master clock: 256fs, 384fs, 512fs, 768fs or 1152fs (Normal Speed Mode)
128fs, 192fs, 256fs or 384fs (Double Speed Mode)
128fs, 192fs (Quad Speed Mode)
- THD+N: -94dB
- Dynamic Range: 106dB
- Power supply: 4.5 to 5.5V
- Very Small Package: 16pin TSSOP (6.4mm x 5.0mm)



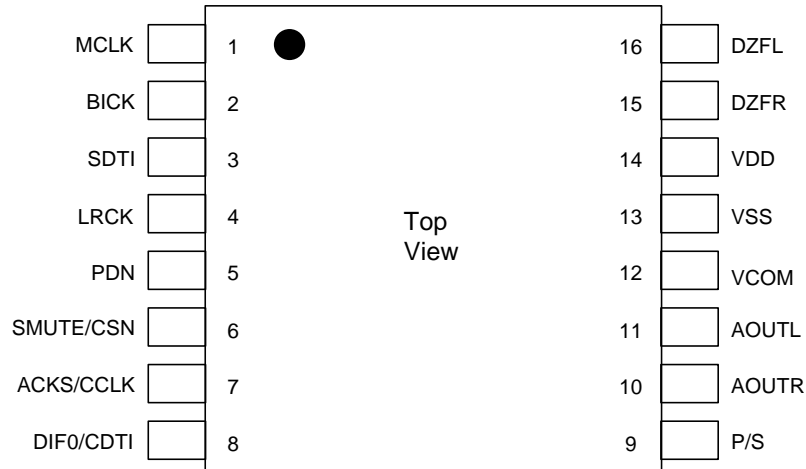
■ Ordering Guide

AK4384VT
AKD4384

-40 ~ +85°C

16pin TSSOP (0.65mm pitch)
Evaluation Board for AK4384

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.
2	BICK	I	Audio Serial Data Clock Pin
3	SDTI	I	Audio Serial Data Input Pin
4	LRCK	I	L/R Clock Pin
5	PDN	I	Power-Down Mode Pin When at “L”, the AK4384 is in the power-down mode and is held in reset. The AK4384 should always be reset upon power-up.
6	SMUTE	I	Soft Mute Pin in parallel mode “H”: Enable, “L”: Disable
	CSN	I	Chip Select Pin in serial mode
7	ACKS	I	Auto Setting Mode Pin in parallel mode “L”: Manual Setting Mode, “H”: Auto Setting Mode
	CCLK	I	Control Data Clock Pin in serial mode
8	DIF0	I	Audio Data Interface Format Pin in parallel mode
	CDTI	I	Control Data Input Pin in serial mode
9	P/S	I	Parallel/Serial Select Pin (Internal pull-up pin) “L”: Serial control mode, “H”: Parallel control mode
10	AOUTR	O	Rch Analog Output Pin
11	AOUTL	O	Lch Analog Output Pin
12	VCOM	O	Common Voltage Pin, VDD/2 Normally connected to VSS with a 0.1μF ceramic capacitor in parallel with a 10μF electrolytic cap.
13	VSS	-	Ground Pin
14	VDD	-	Power Supply Pin
15	DZFR	O	Rch Data Zero Input Detect Pin
16	DZFL	O	Lch Data Zero Input Detect Pin

Note: All input pins except pull-up pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supply	VDD	-0.3	6.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Input Voltage	VIND	-0.3	VDD+0.3	V
Ambient Operating Temperature	Ta	-40	85	°C
Storage Temperature	Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.

WARNING: Operation at or beyond these limits may results in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS=0V; Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supply	VDD	4.5	5.0	5.5	V

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VDD=5.0V; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data;
Measurement frequency=20Hz ~ 20kHz; R_L ≥5kΩ; unless otherwise specified)

Parameter		min	typ	max	Units	
Resolution				24	Bits	
Dynamic Characteristics (Note 3)						
THD+N	fs=44.1kHz	0dBFS		-94	-84	dB
	BW=20kHz	-60dBFS		-42	-	dB
	fs=96kHz	0dBFS		-92	-	dB
	BW=40kHz	-60dBFS		-39	-	dB
	fs=192kHz	0dBFS		-92	-	dB
	BW=40kHz	-60dBFS		-39	-	dB
Dynamic Range (-60dBFS with A-weighted)	(Note 4)	100	106		dB	
S/N (A-weighted)	(Note 5)	100	106		dB	
Interchannel Isolation (1kHz)		90	100		dB	
Interchannel Gain Mismatch			0.2	0.5	dB	
DC Accuracy						
Gain Drift			100	-	ppm/°C	
Output Voltage	(Note 6)	3.15	3.40	3.65	V _{pp}	
Load Resistance	(Note 7)	5			kΩ	
Power Supplies						
Power Supply Current (VDD)						
Normal Operation (PDN = "H", fs≤96kHz)			17	27	mA	
Normal Operation (PDN = "H", fs=192kHz)			20	32	mA	
Power-Down Mode (PDN = "L")	(Note 8)		10	100	μA	

Notes: 3. Measured by Audio Precision (System Two). Refer to the evaluation board manual.

4. 100dB at 16bit data.

5. S/N does not depend on input bit length.

6. Full-scale voltage (0dB). Output voltage scales with the voltage of VREF,
AOUT (typ.@0dB) = 3.4V_{pp} × VDD/5.

7. For AC-load.

8. All digital inputs including clock pins (MCLK, BICK and LRCK) are held VDD or VSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.5 ~ 5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "0")

Parameter	Symbol	min	typ	max	Units		
Digital filter							
Passband	±0.05dB (Note 9) -6.0dB	PB	0	22.05	20.0	kHz	
			-		-	kHz	
Stopband	(Note 9)	SB	24.1			kHz	
Passband Ripple		PR		± 0.02		dB	
Stopband Attenuation		SA	54			dB	
Group Delay	(Note 10)	GD	-	19.3	-	1/fs	
Digital Filter + LPF							
Frequency Response	20.0kHz	fs=44.1kHz	FR	-	± 0.03	-	dB
	40.0kHz	fs=96kHz	FR	-	± 0.03	-	dB
	80.0kHz	fs=192kHz	FR	-	± 0.03	-	dB

Notes: 9. The passband and stopband frequencies scale with fs(system sampling rate).

For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

10. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; VDD = 4.5 ~ 5.5V; fs = 44.1kHz; DEM = OFF; SLOW = "1")

Parameter	Symbol	min	typ	max	Units		
Digital Filter							
Passband	±0.04dB (Note 11) -3.0dB	PB	0	18.2	8.1	kHz	
			-		-	kHz	
Stopband	(Note 11)	SB	39.2			kHz	
Passband Ripple		PR		± 0.005		dB	
Stopband Attenuation		SA	72			dB	
Group Delay	(Note 10)	GD	-	19.3	-	1/fs	
Digital Filter + LPF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0.02/-5	-	dB
	40.0kHz	fs=96kHz	FR	-	+0.02/-4	-	dB
	80.0kHz	fs=192kHz	FR	-	+0.02/-5	-	dB

Note: 11. The passband and stopband frequencies scale with fs.

For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta=25°C; VDD=4.5 ~ 5.5V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout=-80μA)	VOH	VDD-0.4	-	-	V
Low-Level Output Voltage (Iout=80μA)	VOL	-	-	0.4	V
Input Leakage Current (Note 12)	Iin	-	-	± 10	μA

Note: 12. P/S pin has internal pull-up device, normally 100kΩ.

SWITCHING CHARACTERISTICS

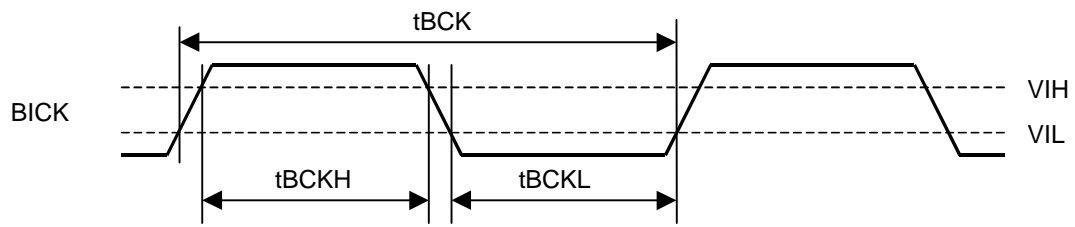
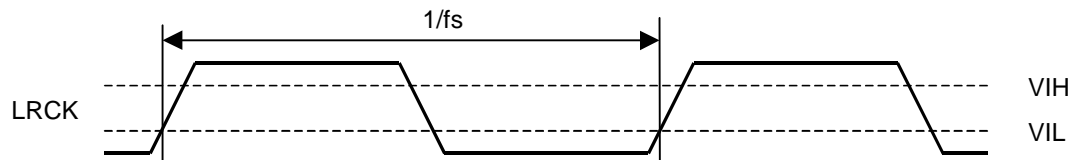
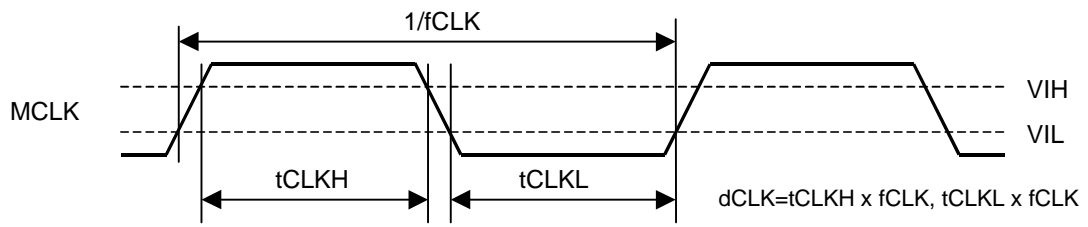
(Ta=25°C; VDD=4.5 ~ 5.5V; CL=20pF)

Parameter	Symbol	min	typ	max	Units
Master Clock Frequency	fCLK	2.048	11.2896	36.864	MHz
Duty Cycle	dCLK	40		60	%
LRCK Frequency					
Normal Speed Mode	f _{sn}	8		48	kHz
Double Speed Mode	f _{sd}	60		96	kHz
Quad Speed Mode	f _{sq}	120		192	kHz
Duty Cycle	Duty	45		55	%
Audio Interface Timing					
BICK Period					
Normal Speed Mode	t _{BCK}	1/128fs			ns
Double/Quad Speed Mode	t _{BCK}	1/64fs			ns
BICK Pulse Width Low	t _{BCKL}	30			ns
Pulse Width High	t _{BCKH}	30			ns
BICK rising to LRCK Edge (Note 13)	t _{BLR}	20			ns
LRCK Edge to BICK rising (Note 13)	t _{LRB}	20			ns
SDTI Hold Time	t _{SDH}	20			ns
SDTI Setup Time	t _{SDS}	20			ns
Control Interface Timing					
CCLK Period	t _{CCK}	200			ns
CCLK Pulse Width Low	t _{CCKL}	80			ns
Pulse Width High	t _{CCKH}	80			ns
CDTI Setup Time	t _{CDS}	40			ns
CDTI Hold Time	t _{CDH}	40			ns
CSN "H" Time	t _{CSW}	150			ns
CSN "↓" to CCLK "↑"	t _{CSS}	50			ns
CCLK "↑" to CSN "↑"	t _{CSH}	50			ns
Reset Timing					
PDN Pulse Width (Note 14)	t _{PD}	150			ns

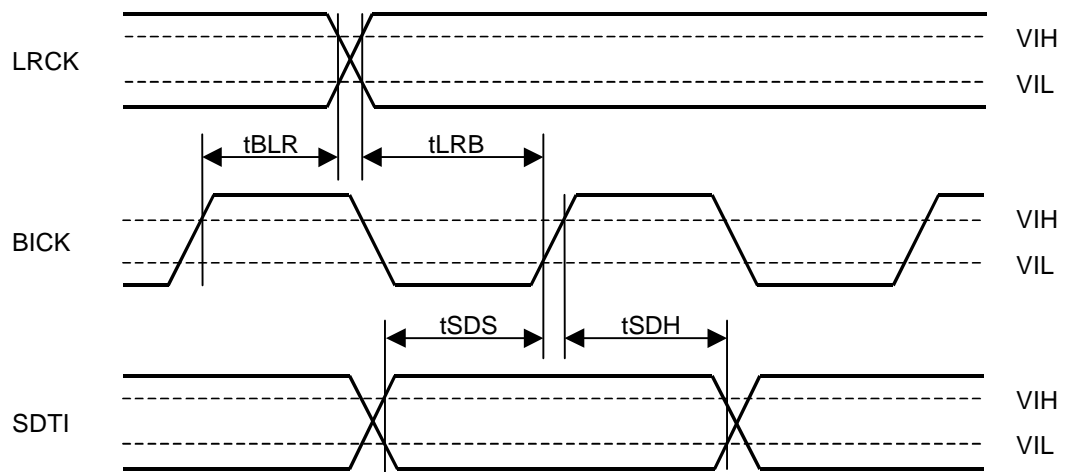
Notes: 13. BICK rising edge must not occur at the same time as LRCK edge.

14. The AK4384 can be reset by bringing PDN= "L".

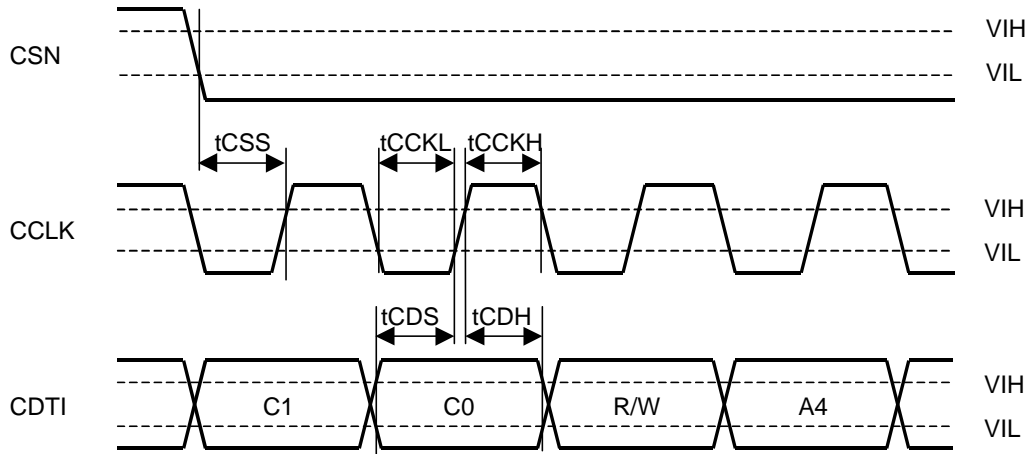
■ Timing Diagram



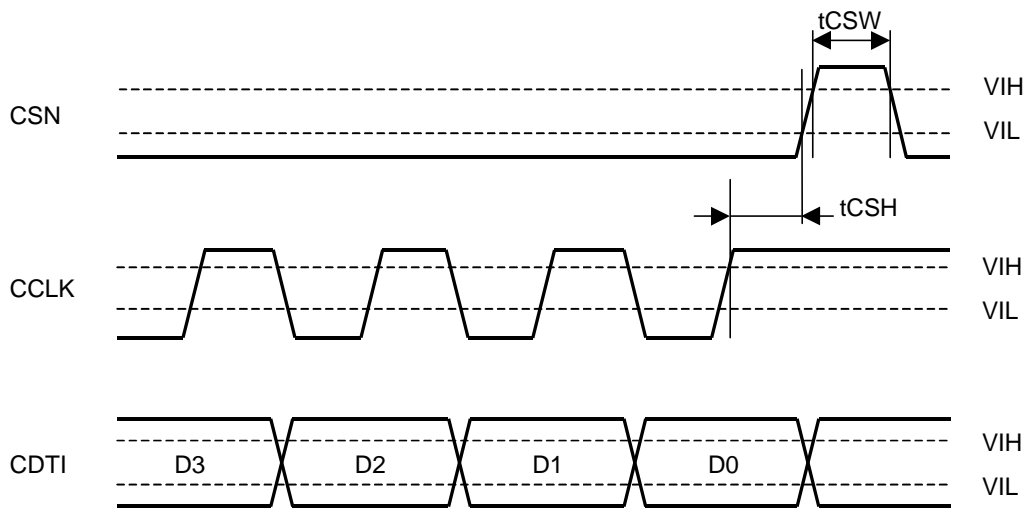
Clock Timing



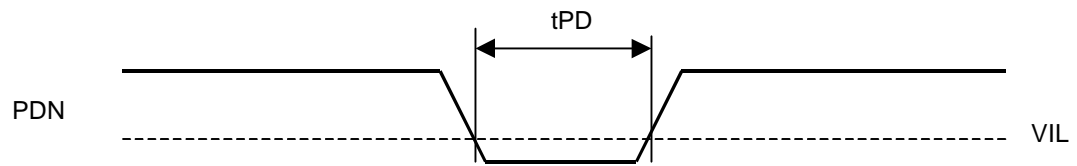
Serial Interface Timing



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4384, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1 (Table 1). The frequency of MCLK at each sampling speed is set automatically. (Table 2~4). After exiting reset (PDN = "↑"), the AK4384 is in Auto Setting Mode. In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 5), and the internal master clock becomes the appropriate frequency (Table 6), it is not necessary to set DFS0/1.

In parallel mode, the sampling speed can be set by only ACKS pin. The internal DFS0 and DFS1 bits are fixed to "0". Therefore, when ACKS pin is "L", the AK4384 operates in Normal Speed Mode. The AK4384 operates in Auto Setting Mode at ACKS = "H". In parallel mode, the AK4384 does not support 128fs and 192fs of Double Speed Mode.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4384 is in the normal operation mode (PDN = "H"). If these clocks are not provided, the AK4384 may draw excess current and may fall into unpredictable operation. This is because the device utilizes dynamic refreshed logic internally. The AK4384 should be reset by PDN = "L" after these clocks are provided. If the external clocks are not present, the AK4384 should be in the power-down mode (PDN = "L"). After exiting reset at power-up etc., the AK4384 is in the power-down mode until MCLK and LRCK are input.

DFS1	DFS0	Sampling Rate (fs)		Default
0	0	Normal Speed Mode	8kHz~48kHz	
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 1. Sampling Speed (Manual Setting Mode)

LRCK fs	MCLK					BICK 64fs
	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	36.8640MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	N/A	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	N/A	3.0720MHz

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK fs	MCLK				BICK 64fs
	128fs	192fs	256fs	384fs	
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
	fs	128fs	192fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 5. Sampling Speed (Auto Setting Mode: Default)

LRCK	MCLK (MHz)							Sampling Speed
	fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
88.2kHz	-	-	22.5792	33.8688	-	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Serial Interface Format

Data is shifted in via the SDTI pin using BICK and LRCK inputs. The DIF0-2 as shown in Table 7 can select five serial data modes. In all modes the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure
0	0	0	0	16bit LSB Justified	≥32fs	Figure 1
1	0	0	1	20bit LSB Justified	≥40fs	Figure 2
2	0	1	0	24bit MSB Justified	≥48fs	Figure 3
3	0	1	1	24bit I ² S Compatible	≥48fs	Figure 4
4	1	0	0	24bit LSB Justified	≥48fs	Figure 2

Default

Table 7. Audio Data Formats (Serial mode)

Mode	DIF0	SDTI Format	BICK	Figure
2	0	24bit MSB Justified	≥48fs	Figure 3
3	1	24bit I ² S Compatible	≥48fs	Figure 4

Table 8. Audio Data Formats (Parallel mode)

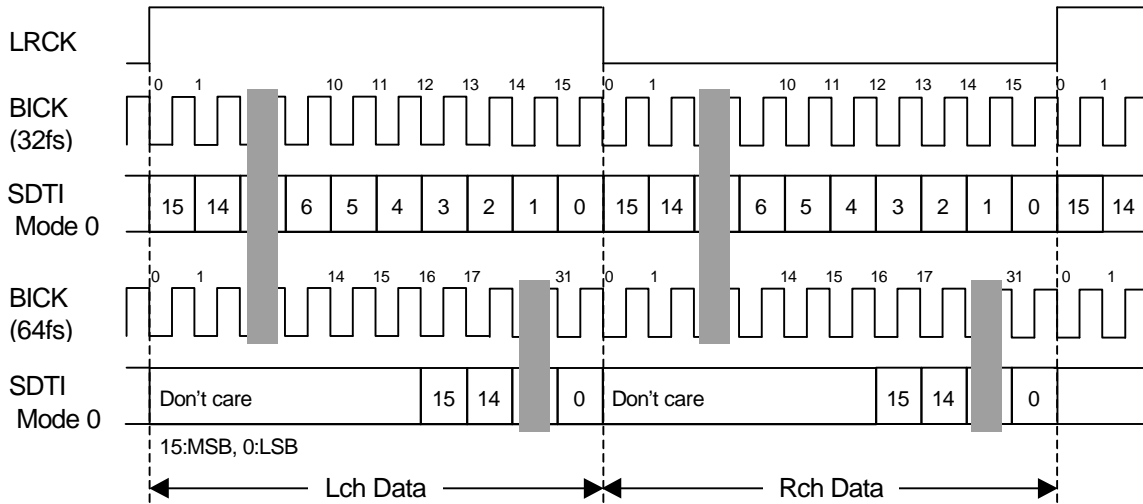


Figure 1. Mode 0 Timing

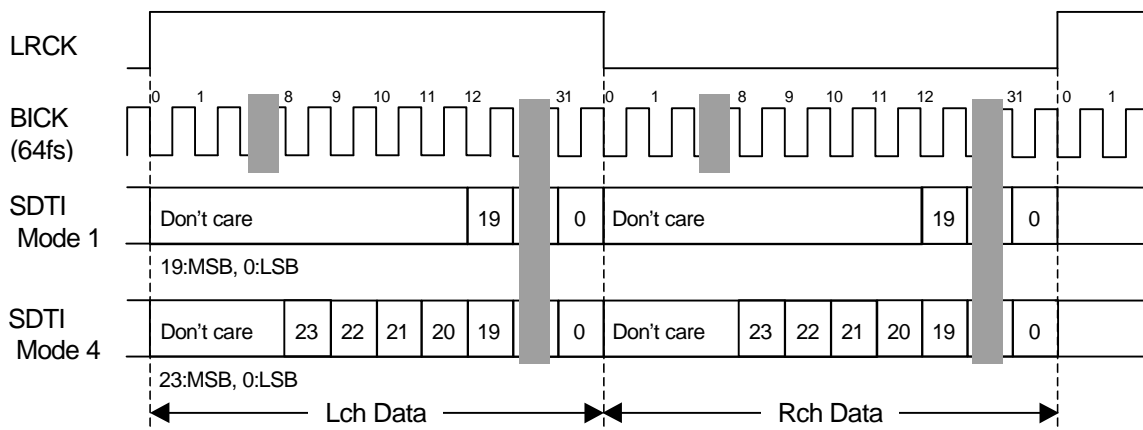


Figure 2. Mode 1,4 Timing

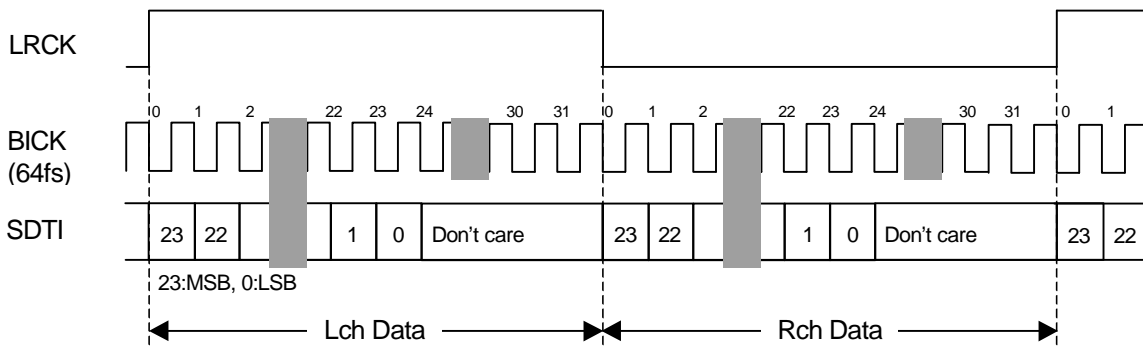


Figure 3. Mode 2 Timing

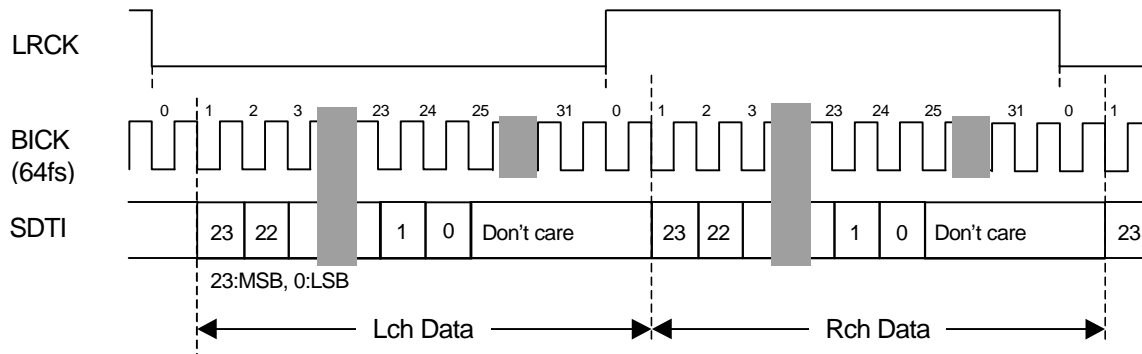


Figure 4. Mode 3 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates ($t_c = 50/15\mu s$) and is enabled or disabled with DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always off.

DEM1	DEM0	Mode
0	0	44.1kHz
0	1	OFF
1	0	48kHz
1	1	32kHz

Default

Table 9. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4384 includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to -48dB and mute. When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions. The transition time of 1 level and all 256 levels is shown in Table 10.

Sampling Speed	Transition Time	
	1 Level	255 to 0
Normal Speed Mode	4LRCK	1020LRCK
Double Speed Mode	8LRCK	2040LRCK
Quad Speed Mode	16LRCK	4080LRCK

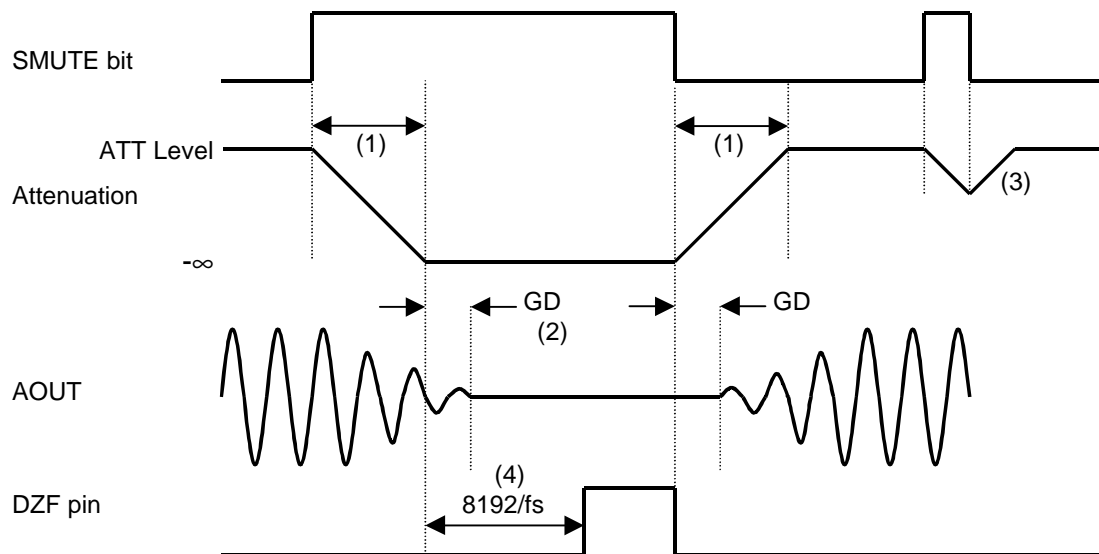
Table 10. ATT Transition Time

■ Zero Detection

The AK4384 has channel-independent zeros detect function. When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to “H”. DZF pin of each channel immediately goes to “L” if input data of each channel is not zero after going DZF “H”. If RSTN bit is “0”, DZF pins of both channels go to “H”. DZF pin of both channels go to “L” at $2\sim 3/f_s$ after RSTN bit returns to “1”. If DZFM bit is set to “1”, DZF pins of both channels go to “H” only when the input data at both channels are continuously zeros for 8192 LRCK cycles. Zero detect function can be disabled by DZFE bit. In this case, DZF pins of both channels are always “L”. DZFB bit can invert the polarity of DZF pin.

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When the SMUTE bit goes to “1”, the output signal is attenuated by $-\infty$ during $ATT_DATA \times ATT$ transition time (Table 10) from the current ATT level. When the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during $ATT_DATA \times ATT$ transition time. If the soft mute is cancelled before attenuating to $-\infty$ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

- (1) $ATT_DATA \times ATT$ transition time (Table 10). For example, in Normal Speed Mode, this time is 1020LRCK cycles ($1020/f_s$) at $ATT_DATA=255$.
- (2) The analog output corresponding to the digital input has a group delay, GD.
- (3) If the soft mute is cancelled before attenuating to $-\infty$ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.
- (4) When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to “H”. DZF pin immediately goes to “L” if input data are not zero after going DZF “H”.

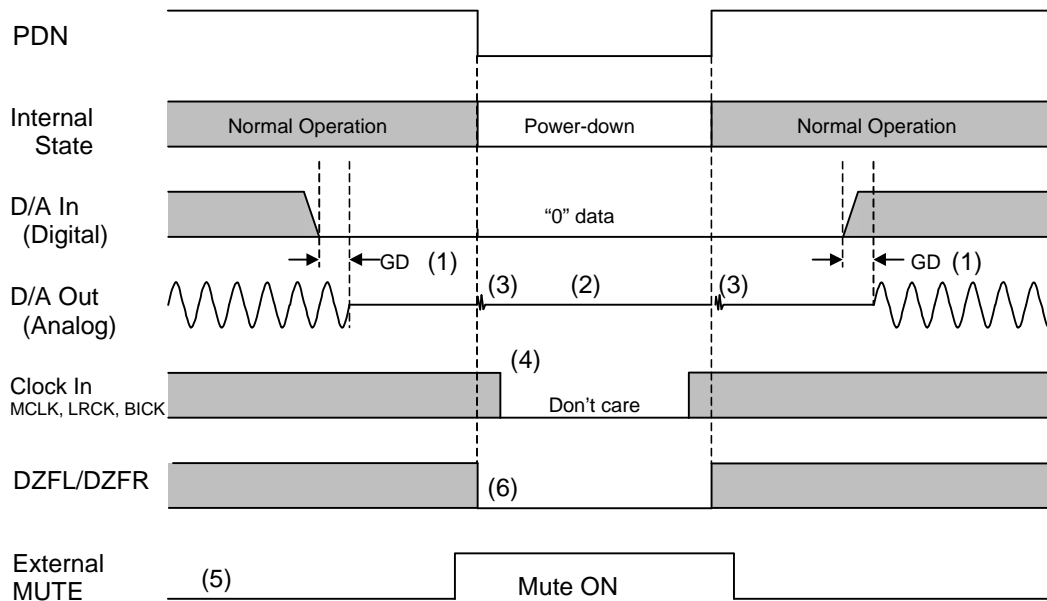
Figure 5. Soft Mute and Zero Detection

■ System Reset

The AK4384 should be reset once by bringing PDN=“L” upon power-up. The AK4384 is powered up and the internal timing starts clocking by LRCK “↑” after exiting reset and power down state by MCLK. The AK4384 is in the power-down mode until MCLK and LRCK are input.

■ Power-down

The AK4384 is placed in the power-down mode by bringing PDN pin “L” and the analog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.



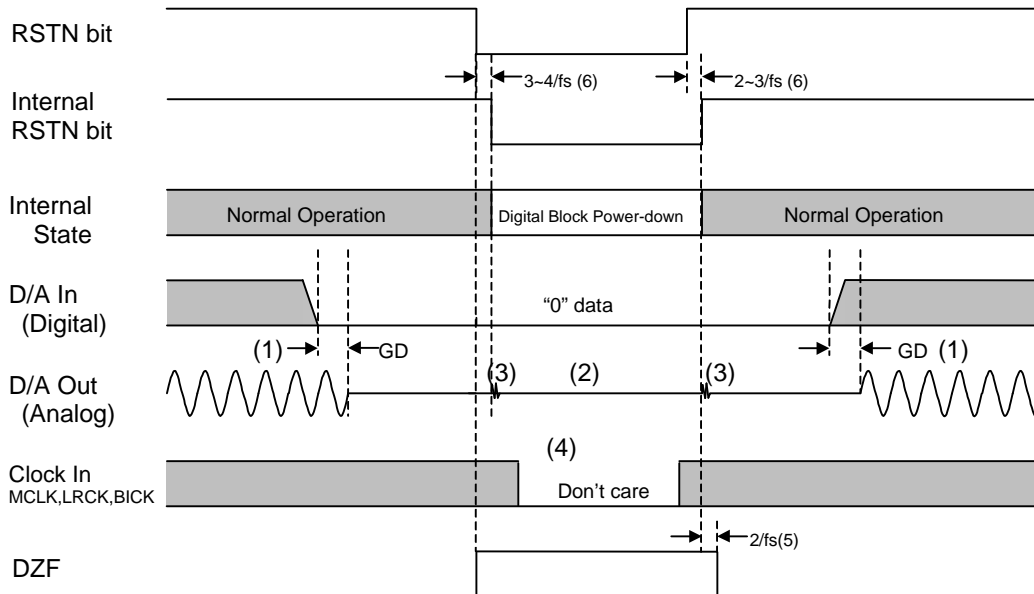
Notes:

- (1) The analog output corresponding to digital input has the group delay (GD).
- (2) Analog outputs are floating (Hi-Z) at the power-down mode.
- (3) Click noise occurs at the edge of PDN signal. This noise is output even if “0” data is input.
- (4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = “L”).
- (5) Please mute the analog output externally if the click noise (3) influences system application. The timing example is shown in this figure.
- (6) DZF pins are “L” in the power-down mode (PDN = “L”).

Figure 6. Power-down/up Sequence Example

Reset Function

When RSTN=0, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZFL/DZFR pins go to “H”. Figure 7 shows the example of reset by RSTN bit.



Notes:

- (1) The analog output corresponding to digital input has the group delay (GD).
- (2) Analog outputs go to VCOM voltage ($V_{DD}/2$).
- (3) Click noise occurs at the edges (“↑ ↓”) of the internal timing of RSTN bit. This noise is output even if “0” data is input.
- (4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode ($RSTN = “L”$).
- (5) DZF pins go to “H” when the RSTN bit becomes “0”, and go to “L” at $2/f_s$ after RSTN bit becomes “1”.
- (6) There is a delay, $3\sim 4/f_s$ from RSTN bit “0” to the internal RSTN bit “0”, and $2\sim 3/f_s$ from RSTN bit “1” to the internal RSTN “1”.

Figure 7. Reset Sequence Example

■ Mode Control Interface

Some function of the AK4384 can be controlled by pins (parallel control mode) shown in Table 11. The serial control interface is enabled by the P/S pin = “L”. Internal registers may be written by 3-wire μP interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to “01”), Read/Write (1bit; fixed to “1”, Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). AK4384 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by CSN “↑”. The clock speed of CCLK is 5MHz (max).

Function	Parallel mode	Serial mode
Double sampling mode at 128/192fs	X	O
De-emphasis	X	O
SMUTE	O	O
Zero Detection	O	O
16/20/24bit LSB justified format	X	O

Table 11. . Function list (O: available, X: not available)

PDN = “L” resets the registers to their default values. When the state of P/S pin is changed, the AK4384 should be reset by PDN= “L”. The internal timing circuit is reset by RSTN bit, but the registers are not initialized.

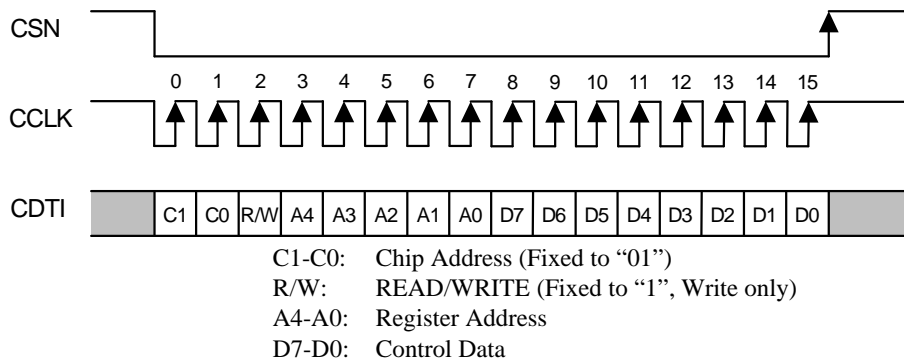


Figure 8. Control I/F Timing

*The AK4384 does not support the read command and chip address. C1/0 and R/W are fixed to “011”

*When the AK4384 is in the power down mode (PDN = “L”) or the MCLK is not provided, writing into the control register is inhibited.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	0	0	0	INVL	INVR	DZFB	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

For addresses from 05H to 1FH, data must not be written.

When PDN pin goes “L”, the registers are initialized to their default values.

When RSTN bit goes “0”, the only internal timing is reset and the registers are not initialized to their default values.

All data can be written to the register even if PW or RSTN bit is “0”.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	0	0	DIF2	DIF1	DIF0	PW	RSTN
	default	1	0	0	0	1	0	1	1

RSTN: Internal timing reset control

0: Reset. All registers are not initialized.

1: Normal Operation

When MCLK frequency or DFS changes, the AK4384 should be reset by PDN pin or RSTN bit.

PW: Power down control

0: Power down. All registers are not initialized.

1: Normal Operation

DIF2-0: Audio data interface formats (see Table 7)

Initial: "010", Mode 2

ACKS: Master Clock Frequency Auto Setting Mode Enable

0: Disable, Manual Setting Mode

1: Enable, Auto Setting Mode

Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SLOW	DFS1	DFS0	DEM1	DEM0	SMUTE
	default	0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable

0: Normal operation

1: DAC outputs soft-muted

DEM1-0: De-emphasis Response (see Table 9)

Initial: "01", OFF

DFS1-0: Sampling speed control

00: Normal speed

01: Double speed

10: Quad speed

When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

SLOW: Slow Roll-off Filter Enable

0: Sharp Roll-off Filter

1: Slow Roll-off Filter

DZFE: Data Zero Detect Enable

0: Disable

1: Enable

Zero detect function can be disabled by DZFE bit "0". In this case, the DZF pins of both channels are always "L".

DZFM: Data Zero Detect Mode

0: Channel Separated Mode

1: Channel ANDed Mode

If the DZFM bit is set to "1", the DZF pins of both channels go to "H" only when the input data at both channels are continuously zeros for 8192 LRCK cycles.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	0	0	0	INVL	INVR	DZFB	0	0
	default	0	0	0	0	0	0	0	0

DZFB: Inverting Enable of DZF

0: DZF goes "H" at Zero Detection

1: DZF goes "L" at Zero Detection

INVR: Inverting Lch Output Polarity

0: Normal Output

1: Inverted Output

INVL: Inverting Rch Output Polarity

0: Normal Output

1: Inverted Output

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	default	1	1	1	1	1	1	1	1

$$ATT = 20 \log_{10} (ATT_DATA / 255) \text{ [dB]}$$

00H: Mute

SYSTEM DESIGN

Figure 9 and 10 show the system connection diagram. An evaluation board (AKD4384) is available in order to allow an easy study on the layout of a surrounding circuit.

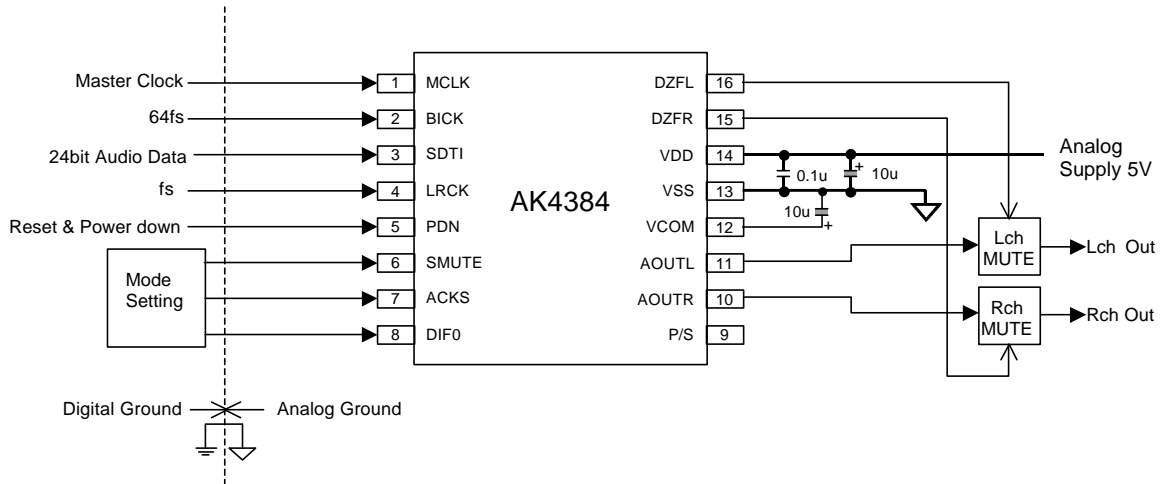


Figure 9. Typical Connection Diagram (Parallel Mode)

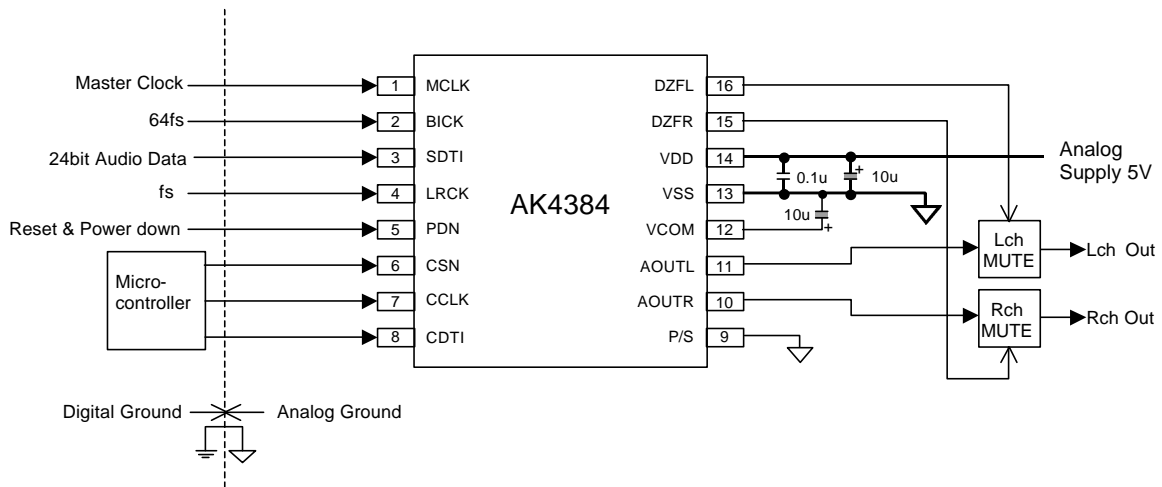


Figure 10. Typical Connection Diagram (Serial Mode)

Notes:

- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-up pin should not be left floating.

1. Grounding and Power Supply Decoupling

VDD and VSS are supplied from analog supply and should be separated from system digital supply. Decoupling capacitor, especially 0.1 μ F ceramic capacitor for high frequency should be placed as near to VDD as possible. The differential Voltage between VDD and VSS pins set the analog output range.

2. Analog Outputs

The analog outputs are single-ended and centered around the VCOM voltage. The output signal range is typically 3.40Vpp (typ@VDD=5V). The phase of the analog outputs can be inverted channel independently by INVL/INVR bits. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. The output voltage is a positive full scale for 7FFFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is VCOM voltage for 000000H (@24bit).

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of VCOM + a few mV. Figure 11 shows an example of the external LPF with 2Vrms output.

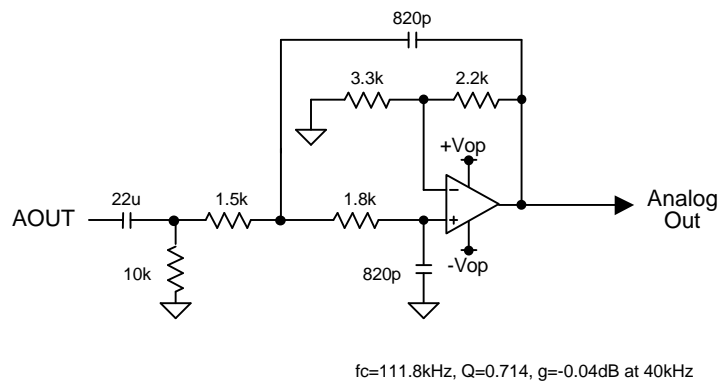
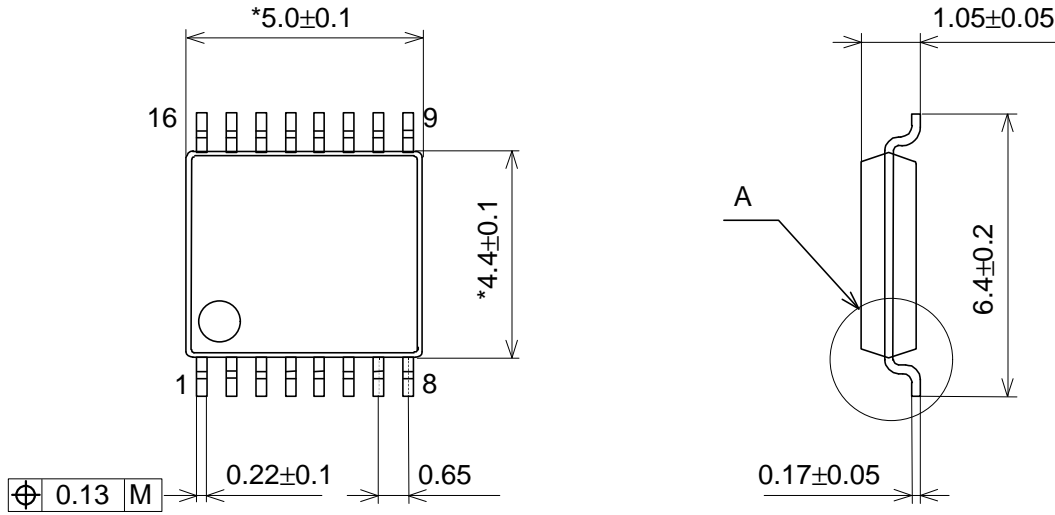


Figure 11. External 2nd order LPF Circuit Example (using op-amp with dual power supplies)

PACKAGE

16pin TSSOP (Unit: mm)

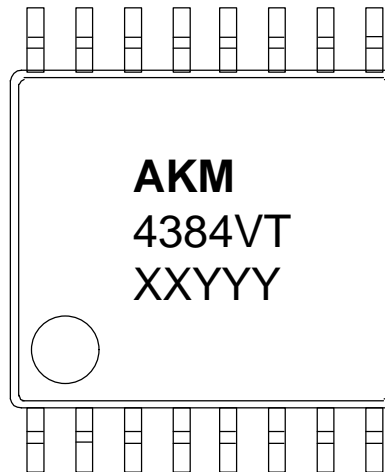


NOTE: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder(Pb free) plate

MARKING



- 1) Pin #1 indication
- 2) Date Code : XXYYYY (5 digits)
 XX: Lot#
 YYY: Date Code
- 3) Marketing Code : 4384VT
- 4) Asahi Kasei Logo

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