High-Performance, High-Current DrMOS Power Module

Features

- 4.5V ~ 5.5V Input Range for VCC & PVCC
- 4.5V ~ 25V Input Range for VIN
- Power-On-Reset Monitoring on VCC Pin
- Up to 10A (peak), 8A (continuous) output current scale
- Adjustable Over-Current Protection Threshold
- Up to 1.5MHz PWM operation
- Built-in Tri-State PWM input Function
- Built in EN Timing Control function
- Build in N-CH MOSFET for high side, N-CH MOSFET for low side
- Skip Mode Operation
- Over-Temperature Protection
- TQFN 4x4-23 package
- Lead Free and Green Devices Available (RoHS Compliant)

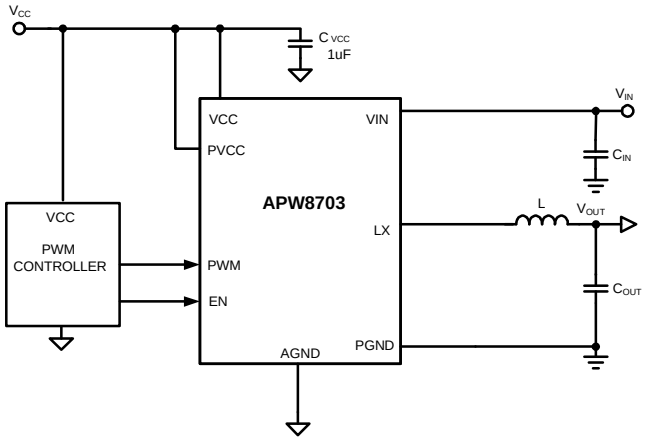
General Description

The APW8703 integrates a high-side N-channel MOSFET and a low-side N-channel MOSFET with adaptive dead-time control. The APW8703 have a built-in tri-state PWM input function which can support a number of PWM controllers. When the PWM input signal stays tri-state, the tri-state function shuts off the high-side MOSFET and turns on the low-side MOSFET without consider ZC function. The device is also equipped with Power-On-Reset(POR) and enable control functions into a single package and accurate current limit. The device over-current protection monitors the output current by using the voltage drop across the $R_{DS(ON)}$ of low-side MOSFET, eliminating the need for a current sensing resistor that features high efficiency and low cost. The POR circuit with hysteresis monitors VCC supply voltage to start up/shut-down the IC at power-on/off. The APW8703 also can be enabled or disabled by other power system. Pulling the EN pin high or low will turn on or shut off the device.

Applications

- Desktops
- Graphics Cards
- Severs
- Portable/Notebook Regulators

Simplified Application Circuit

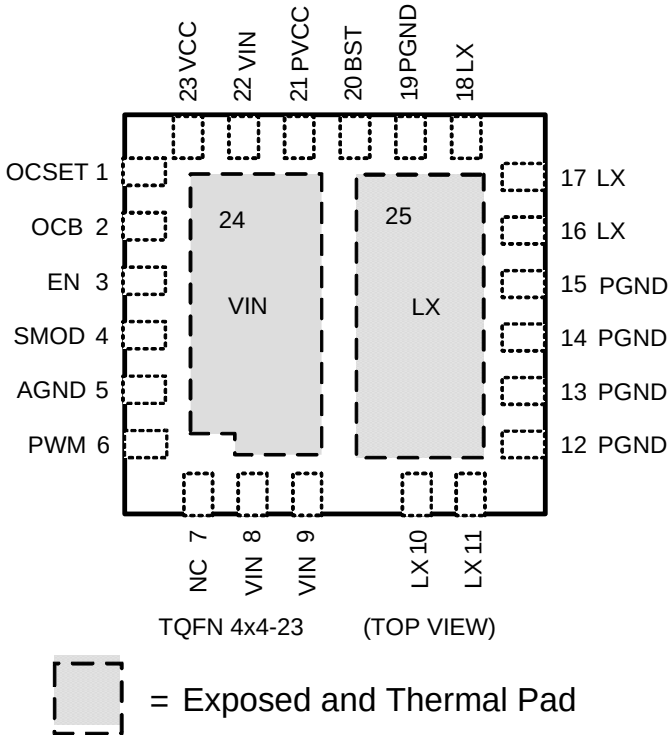


Ordering and Marking Information

APW8703 □□□-□□□ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN 4x4-23 Operating Ambient Temperature Range I : -40 to 85°C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APW8703 QB:  X - Date Code	

Note:ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN 4x4-23 (TOP VIEW)

= Exposed and Thermal Pad

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC} & V_{PVCC}	VCC & PVCC to GND Voltage	-0.3 ~ 7	V
V_{IN}	VIN to PGND Voltage	-0.3 ~ 30	V
V_{LX}	LX to PGND Voltage >20ns Pulse Width <20ns Pulse Width	 -0.3 ~ 30 -5 ~ 38	V
V_{BST}	BST to GND Voltage	-0.3 ~ 37	V
V_{BST}-V_{LX}	BST to LX Voltage	-0.3 ~ 7	V
Other Pins	EN,SMOD, OCSET and PWM to AGND Voltage	-0.3 ~ V_{CC}+0.3	V
	AGND to PGND Voltage	-0.3 ~0.3	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature(10 Seconds)	300	°C

Note1: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TQFN4x4-23	50	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{CC}&V_{PVCC}	VCC and PVCC to AGND Voltage	4.5 ~ 5.5	V
V_{IN}	VIN to PGND Voltage	4.5 ~ 25	V
I_{OUT}	Maximum Continuous Output Current	8	A
	Maximum Peak Output Current	10	A
F_{PWM}	PWM Operation Frequency	0.1 ~ 1.5	MHz
t_{PWM_OFF}	PWM Input Minimum Off Time	200 ~	ns
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC} = V_{PVCC} = V_{EN} = 5V, V_{IN} =12V and T_A = 25°C.

Symbol	Parameter	Test Conditions	APW8703			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
I_{VCC}	VCC Supply Current	EN = High, PWM = High, SMOD=L	-	90	120	uA
		EN = High, PWM = Low, SMOD=L	-	90	120	uA
		EN = Low	-	-	1.0	uA
POWER-ON-RESET(POR)						
	VCC Rising POR Thresold		3.7	4.0	4.3	V
	VCC POR Hysteresis		-	120	-	mV
BOOTSTRAP						
R_{BST}	BST Switch on Resistance	BST Source 10mA	-	33	-	Ω
	BST Leakage Current	$V_{BOOT-PGND}$=30V, V_{LX}=25V	-	-	1	uA
POWER STAGE						
R_{ON_H}	High-side switch on resistance		-	25	-	mΩ
R_{ON_L}	Low-side switch on resistance		-	7	-	mΩ
	High side MOSFET Leakage Current	V_{IN}=25V, V_{EN}= V_{LX}=GND	-1	-	1	uA
	Low side MOSFET Leakage Current	V_{IN}=V_{LX}=V_{BST}=25V, V_{EN}=GND	-1	-	1	uA
ZERO CURRENT DETECT						
V_{ZC}	Zero Current Detect	V_{LX} - PGND	-5	-	5	mV
Over-Current Protection(OCP)						
I_{OCSET}	OCSET Current Source		9	10	11	μA
V_{OCP}	OCP Threshold		-	190	-	mV
	OCB Output Low Voltage	Sink Current=5mA	-	0.5	0.7	V
	OCB Leakage Current	V_{OCB}=5V	-	-	1	uA
$t_{D(OCB)}$	OCB Deglitch TIme	OCB go low	-	0.6	-	ms
Over-Temperature Protection (OTP)						
T_{OTP}	OTP Rising Threshold		-	145	-	°C
	OTP Hysteresis		-	45	-	°C
PWM INPUT PIN						
V_{PWM_H}	PWM Logic High Threshold	V_{PWM} Rising	3.6	3.9	4.2	V
		Hysteresis	-	150	-	mV
V_{TRI_H}	Tri-state Input Rising Logic Threshold	V_{PWM} Rising	1.2	1.5	1.8	V
		hysteresis	300	400	550	mV
V_{TRI_L}	Tri-state Input Falling Logic Threshold	V_{PWM} Falling	2.8	3.1	3.4	V
		hysteresis	300	400	500	mV
I_{PWM}	PWM Pin input current	Source/ Sink , V_{PWM} = 0V to 5V	-1	-	1	uA

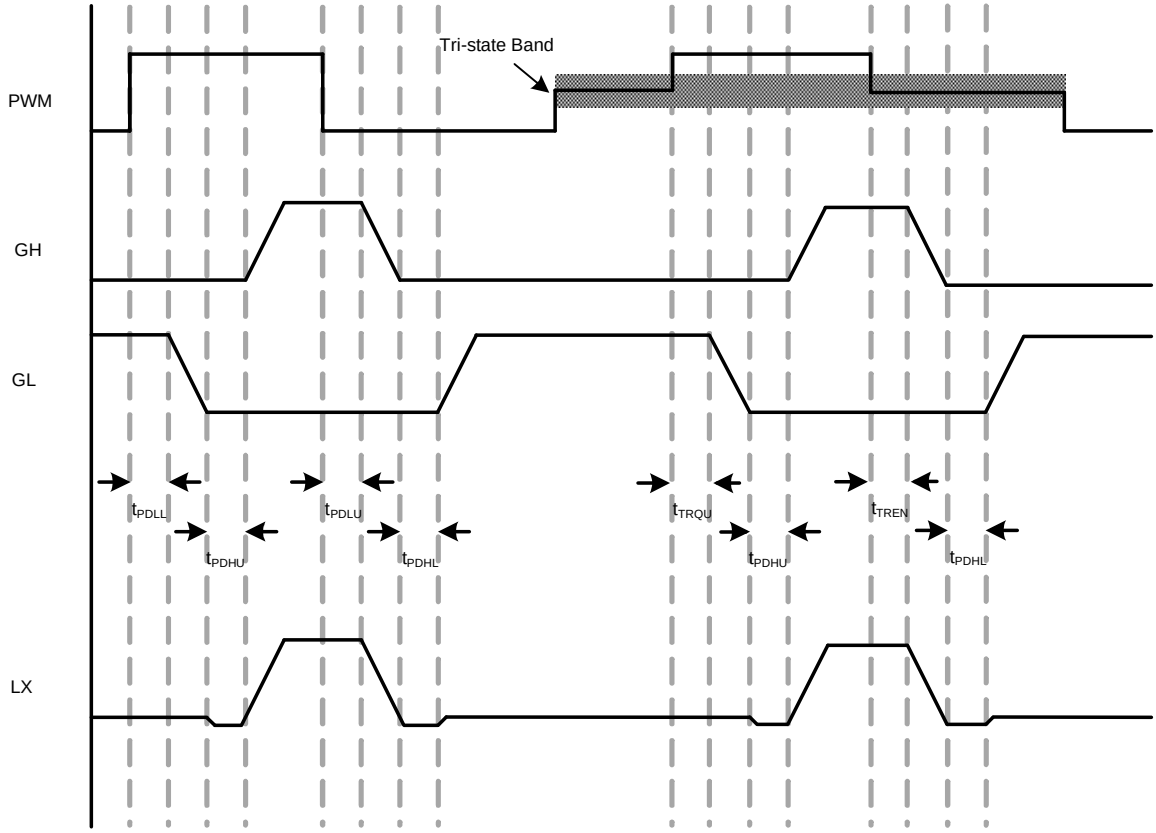
Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{CC} = V_{PVCC} = V_{EN} = 5V, V_{IN} =12V and T_A = 25°C.

Symbol	Parameter	Test Conditions	APW8703			Unit
			Min	Typ	Max	
EN INPUT AND SMOD Input						
	EN Input Logic High		1.2	-	-	V
	EN Input Logic Low		-	-	0.4	V
	EN Input Current	V_{EN} = 5V	-1	-	1	uA
	SMOD Input Logic High		1.5	-	-	V
	SMOD Input Logic Low		-	-	0.4	V
	SMOD Input Current	V_{SMOD} = 5V	-1	-	1	uA
GATE DRIVER TIMINGS (refer to Figure 1 and Table 1)						
t_{PDLU}	PWM to High side Gate	PWM H to L to GH H to L (Note4)	-	18	-	ns
t_{PDLL}	PWM to Low side Gate	PWM L to H to GL H to L (Note4)	-	25	-	ns
t_{PDHU}	LS to HS Gate Deadtime	GL H to L to GH L to H (Note4)	-	20	-	ns
t_{PDHL}	HS to LS Gate Deadtime	GH H to L to GL L to H (Note4)	-	20	-	ns
t_{TRQU}	Quit Tri-state Delay	Tri-state GL H to L to PWM H (Note 4)	-	40	-	ns
t_{TREN}	Enter Tri-state Delay	GH H to L to Tri-state GL L (Note 4)	-	120	-	ns

Note4: Not tested in production.

PWM Operation Characteristics



Note: LX during entering/exiting tri-state behaves depend on inductor current

Figure 1 : Timing chart

Table 1 : Truth table

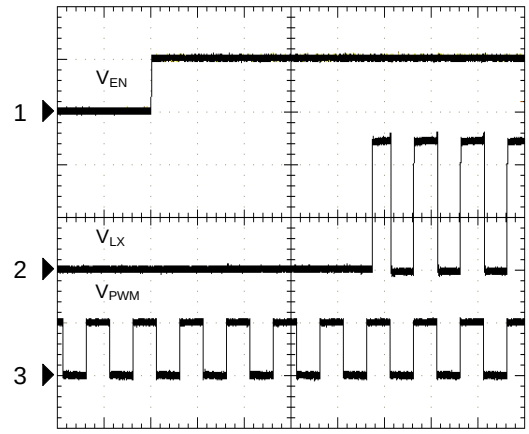
EN	SMOD	PWM	GH	GL
L	X	X	L	L
H	L	H	H	L
H	L	L	L	Skip mode
H	X	Tri-state	L	H
H	H	H	H	L
H	H	L	L	H

Pin Descriptions

PIN		FUNCTION
NUMBER	NAME	
1	OCSET	Over-Current Setting Input. Connect a resistor to GND to set the OCP trip level.
2	OCB	Fault Indication Pin. This pin goes low when a OCP condition is detected after a 0.6ms deglitch time.
3	EN	Enable Pin. Logic high enables the device. Logic low disables the device. The pin is not floating.
4	SMOD	Skip Mode or PWM Mode Selection. IC enter Skip Mode when SMOD pull low; IC enter PWM Mode when SMOD pull high.
5	AGND	Signal Ground for The IC. All voltage levels are measured with respect to this pin. Tie this pin to the ground island/plane through the lowest impedance connection available.
6	PWM	PWM Drive Logic Input.
7	NC	No Connection.
8,9,22,24	VIN	Supply Voltage Input Pin for Power Stage.
10,11,16,17,18,25	LX	Junction Point of The High-side and Low-side MOSFET. Connect the output LC filter for PWM output voltage.
12,13,14,15,19	PGND	Power ground.
20	BST	High-Side Gate Driver Power Input Pin. Connect a 0.1uF capacitor from BST to LX.
21	PVCC	Supply Voltage Input Pin for Low Side Gate Driver.
23	VCC	Supply voltage Input Pin for Control Circuitry. Decoupling at least 1uF of a MLCC capacitor from the VCC pin to the AGND pin.

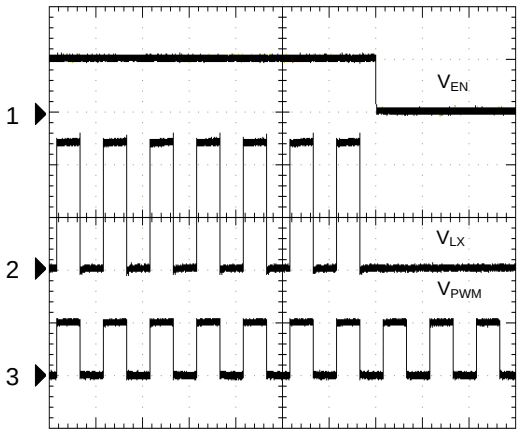
Operating Waveforms

Enable



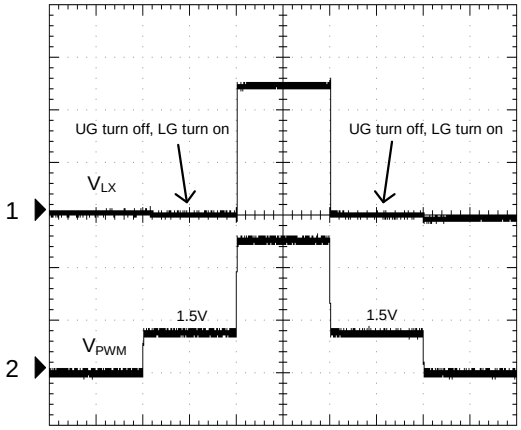
CH1: V_{EN}, 5V/Div
CH2: V_{LX}, 5V/Div
CH3: V_{PWM}, 5V/Div
Time: 10us/Div

Shutdown



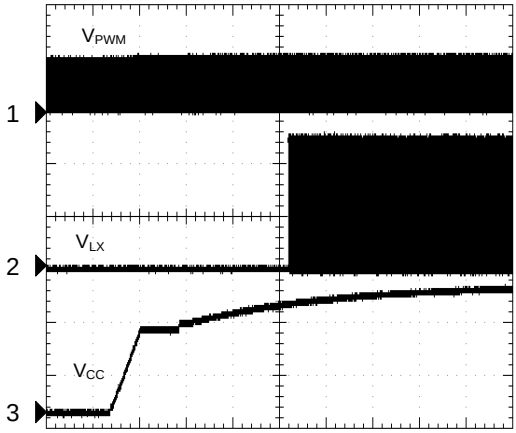
CH1: V_{EN}, 5V/Div
CH2: V_{LX}, 5V/Div
CH3: V_{PWM}, 5V/Div
Time: 10us/Div

Tri-State



CH1: V_{LX}, 5V/Div
CH2: V_{PWM}, 2V/Div
Time: 10us/Div

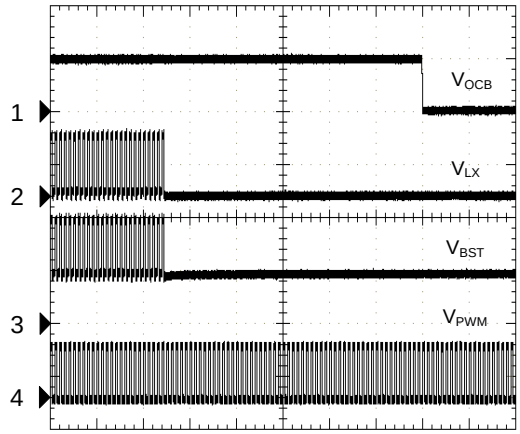
VCC Power on



CH1: V_{PWM}, 5V/Div
CH2: V_{LX}, 5V/Div
CH3: V_{CC}, 2V/Div
Time: 1ms/Div

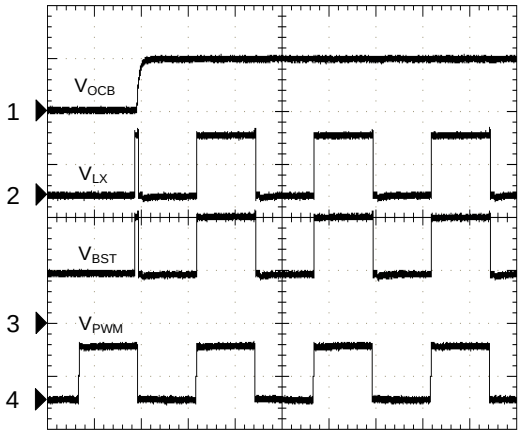
Operating Waveforms (Cont.)

Thermal Shutdown



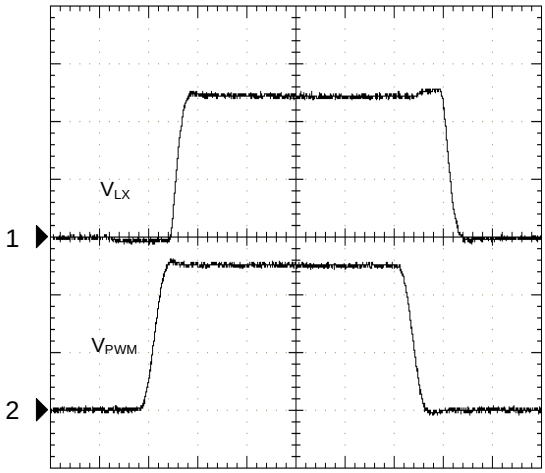
CH1: V_{OCB}, 5V/Div
CH2: V_{LX}, 5V/Div
CH3: V_{BST}, 5V/Div
CH4: V_{PWM}, 5V/Div
Time: 100us/Div

Thermal Shutdown release



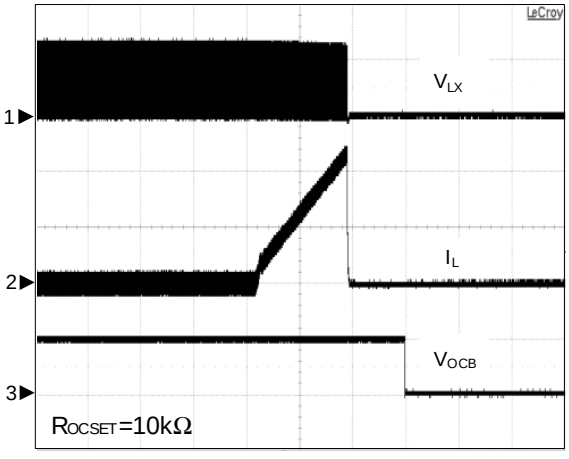
CH1: V_{OCB}, 5V/Div
CH2: V_{LX}, 5V/Div
CH3: V_{BST}, 5V/Div
CH4: V_{PWM}, 5V/Div
Time: 4us/Div

PWM Operation



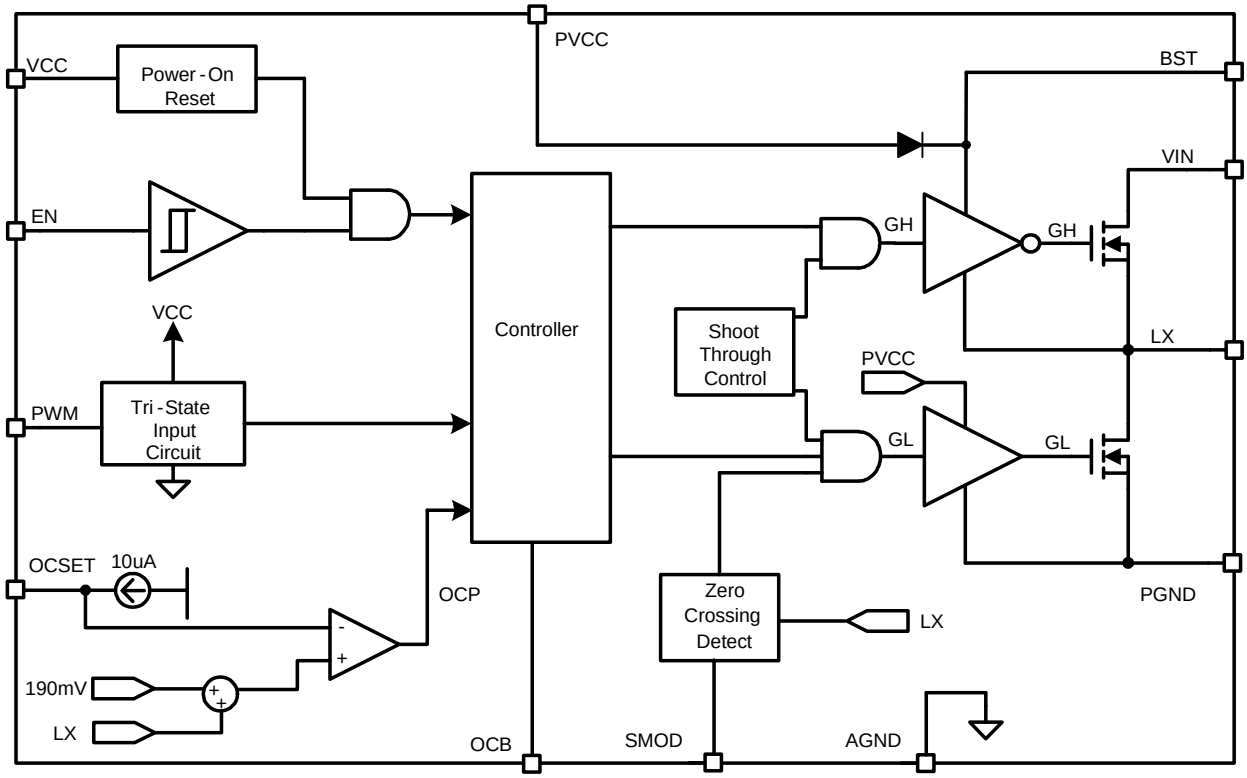
CH1: V_{LX}, 5V/Div
CH2: V_{PWM}, 2V/Div
Time: 80ns/Div

Over Current Protection

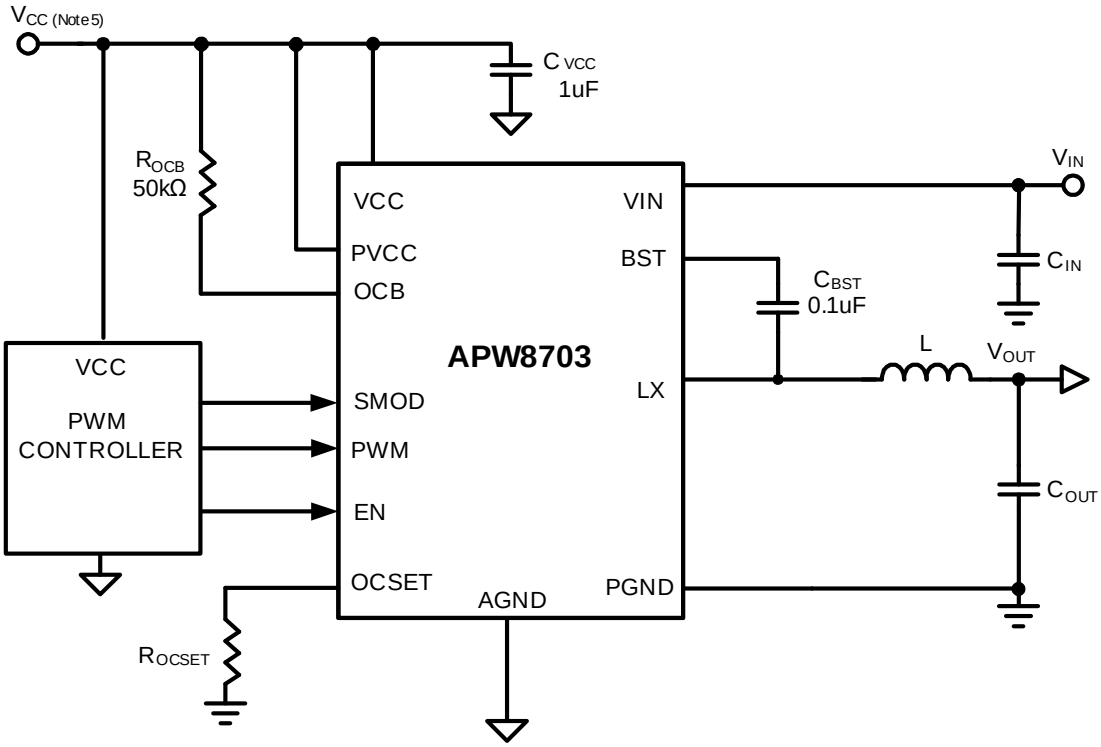


CH1: V_{LX}, 10V/Div, DC
CH2: I_L, 5A/Div, DC
CH3: V_{OCB}, 5V/Div, DC
TIME: 500µs/Div

Block Diagram



Typical Application Circuit



Note 5: VCC voltage rail must be SYNC with PWM controller VCC voltage level.

Function Description

VCC Power-On-Reset (POR)

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the VCC supply voltage exceeds the rising POR threshold, the POR enables the device. The POR circuit has a hysteresis and a deglitch feature so that it will typically ignore undershoot transients on the VCC pin.

Enable Control

Pulling the VEN above 1.2V will enable the driver output, and pulling VEN below 0.4V will disable the driver output. If enable function is not used, connect EN to VCC for normal operation.

PWM Control

The PWM pin has three states. If the pin is gave high level state, the internal pre-driver output of high-side (GH) goes high and internal pre-driver output of low-side (GL) goes low. If the pin is gave low level state, the GH goes low and GL goes high. If the pin is gave tri-state level, the GH goes low and GL goes High. Please refer to Table 1.

SMOD

APW8703 can be operated in the skip mode using SMOD pin. When SMOD is low, the IC will enter the skip mode. In Skip mode if the PWM is low and the ZC is detected, the GL will be pulled low, and low-side MOSFET will be off. It is useful if the converter has to operation in skip mode to improve efficiency at light load. When SMOD is high, the converter will operate in force PWM mode.

Over-current Protection (OCP)

The over-current protection function protects the switching converter to against over-current or short-circuit conditions. The IC senses the inductor current by detecting the drain to source voltage of low-side MOSFET during it's on-state. When the inductor current is over the internal OCP trip point, the both of gate drivers will be latched off.

The current limit circuit employs a "peak" current-sensing algorithm (See Figure 2). The APW8703 use the low-side MOSFET's $R_{DS(ON)}$ of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at LX pin is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.
The current-limit threshold is given by:

$$I_{LIMIT}=(190mV-R_{OCSET}*10uA)/R_{ON\_L}$$

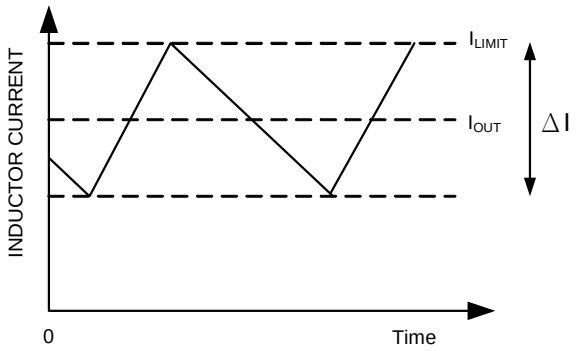


Figure 2. Current Limit algorithm

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature T_{OTR}, the IC will enter the over temperature protection state that suspends the PWM, which forces the UG and LG gate drivers output low. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 45°C. The OTP designed with a 45°C hysteresis lowers the average T_J during continuous thermal overload conditions, which increases lifetime of the APW8703.

OCB Output

The APW8703 provide an open-drain output to indicate that a fault has occurred. When current-limit occurs for a deglitch time of $t_{D(OCB)}$, the OCB goes low. Since the OCB pin is an open-drain output, connecting a resistor to a pull high voltage is necessary.

Layout Consideration

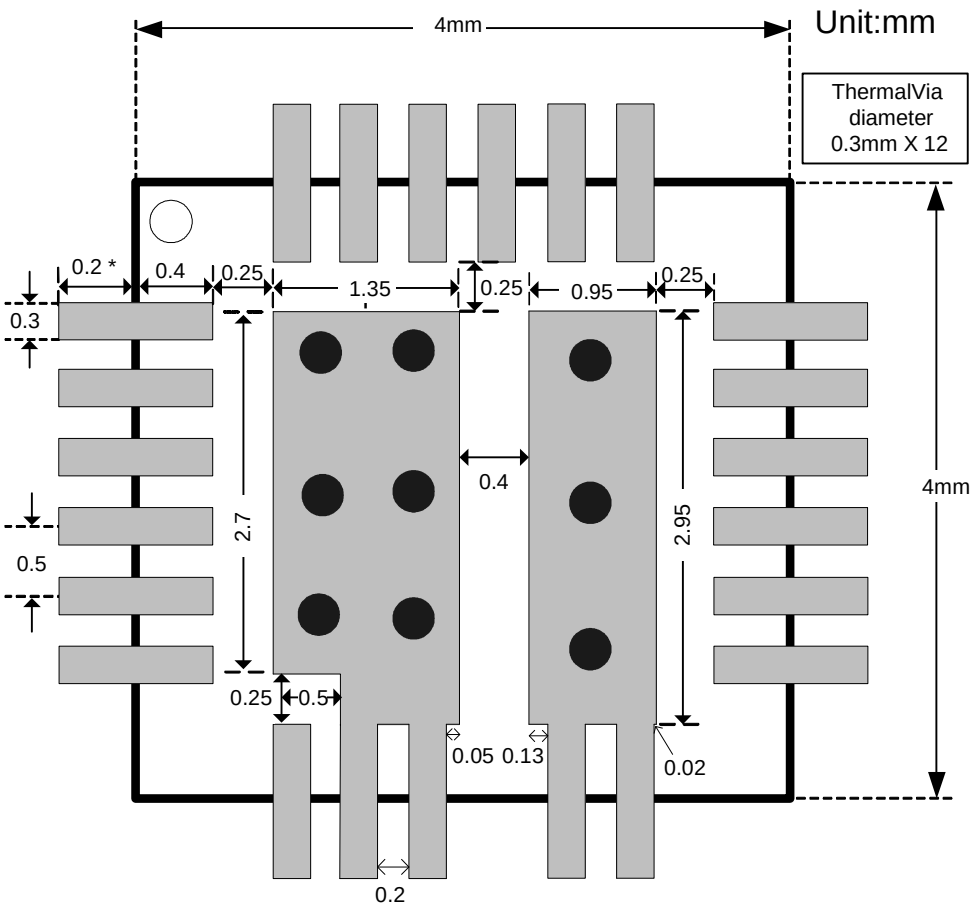
For all switching power supplies, the layout is an important step in the design; especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show noise problems and duty cycle jitter.

1. The input capacitors should be placed close to the VIN pin, and the ground terminals of input capacitors and output capacitors should be close PGND pin.
2. To minimize copper trace connections that can inject noise into the system, the inductor should be placed as close as possible to the LX pin to minimize the noise coupling into other circuits.
3. The traces of PWM signal from the PWM controller to the PWM pin of APW8703 should be short to eliminate the parasitical capacitance; the parasitical capacitance will cause an invalid PWM signal.

Application Information

Recommended Minimum Footprint

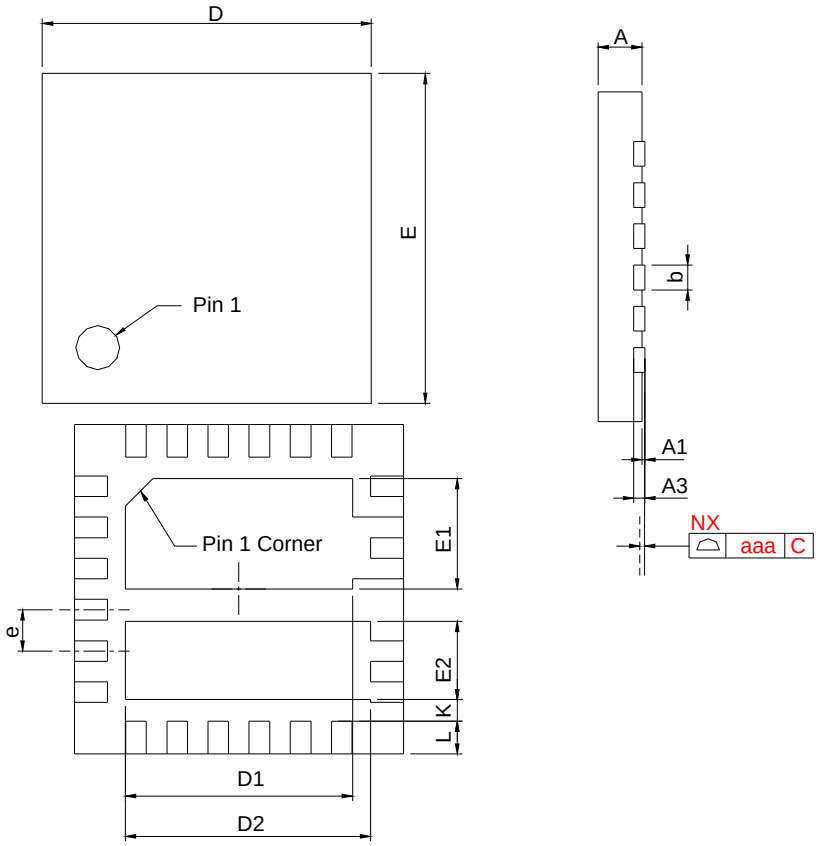
TQFN4x4-23



* Just Recommend

Package Information

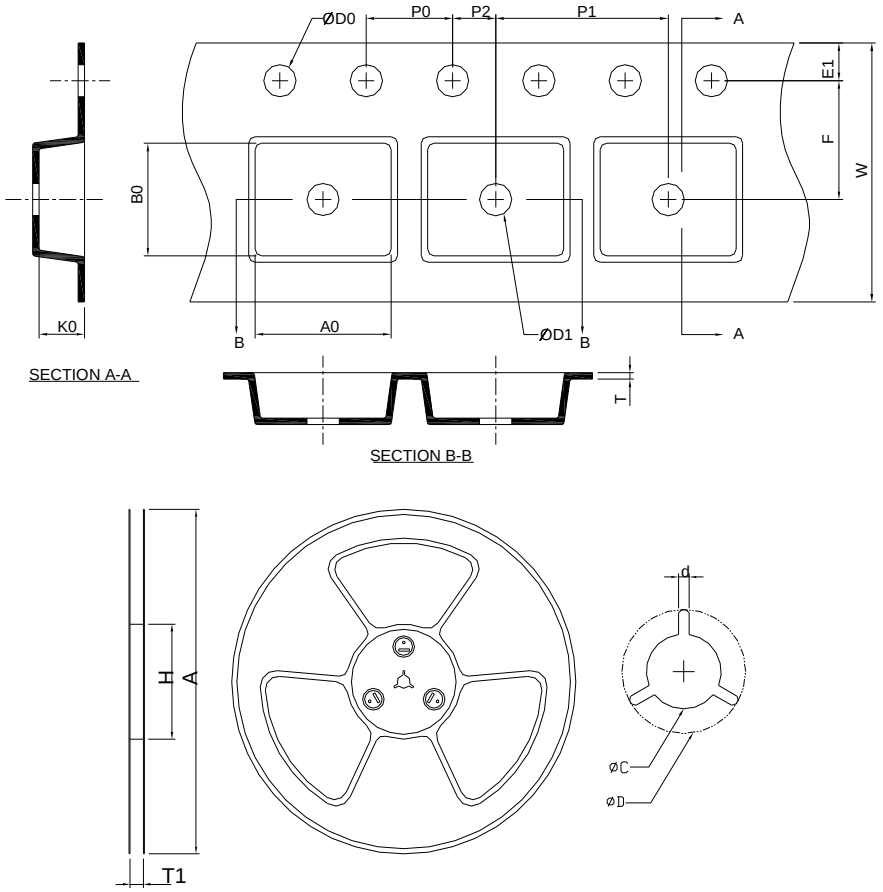
TQFN4x4-23



SYMBOL	TQFN4x4-23			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.20	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D1	2.58	2.78	0.102	0.109
D2	2.95	3.15	0.116	0.124
E	3.90	4.10	0.154	0.161
E1	1.24	1.44	0.049	0.057
E2	0.85	1.05	0.033	0.041
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Follow from JEDEC MO-229 WCCD-3.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN4x4	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.50±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.00±0.10	8.00±0.10	2.00±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.00±0.20

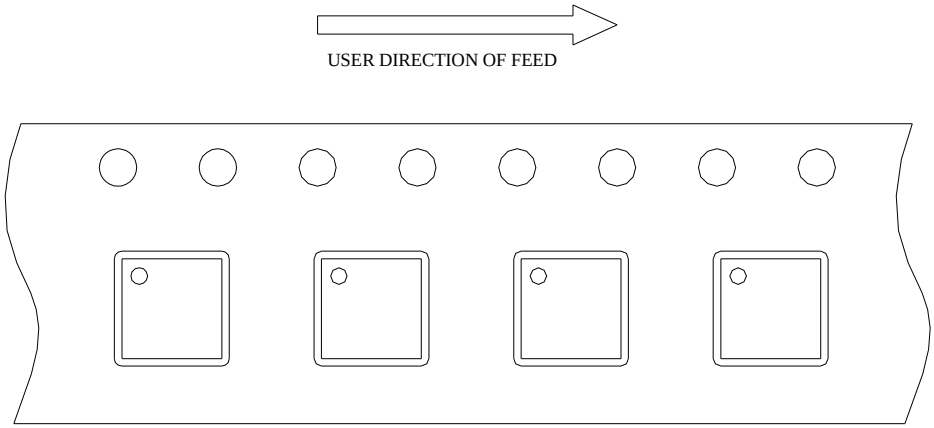
(mm)

Devices Per Unit

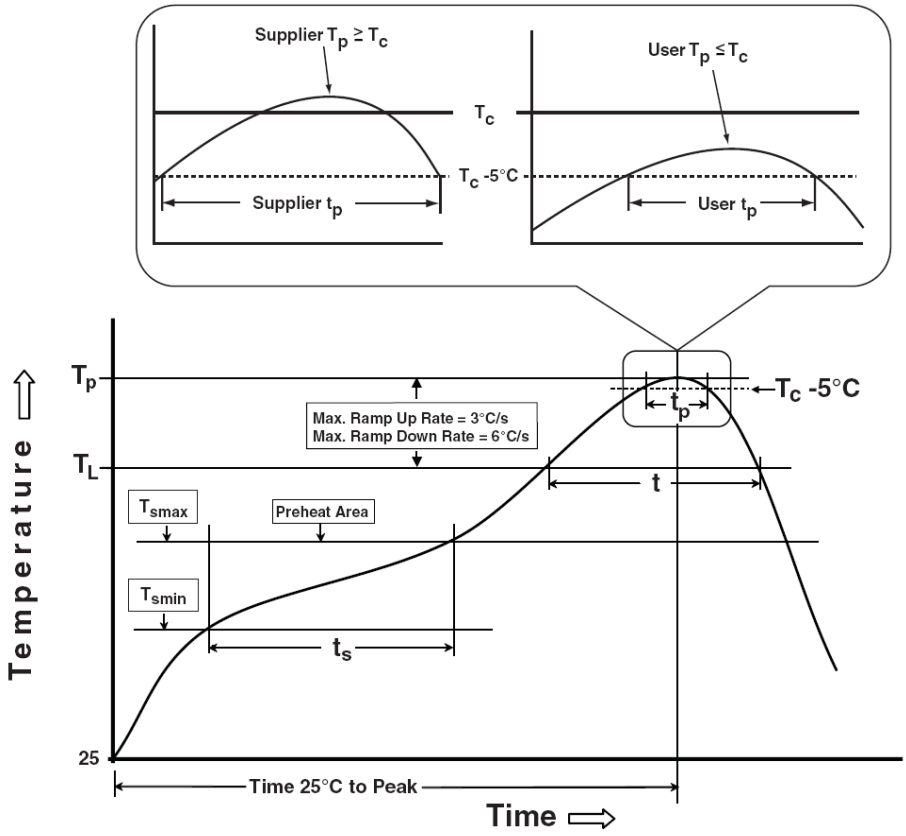
Package Type	Unit	Quantity
TQFN4x4	Tape & Reel	3000

Taping Direction Information

TQFN4x4-23



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 3350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ 125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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