Main Product Characteristics:

	NMOS	PMOS
V_{DSS}	30V	-30V
R_{DS}(on)	32.4mohm	61.6mohm
I_D	4A	-3.6A
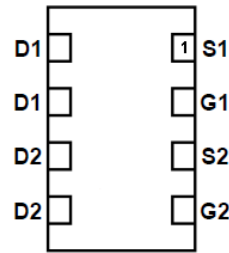
DFN 3x2-8L
Bottom View
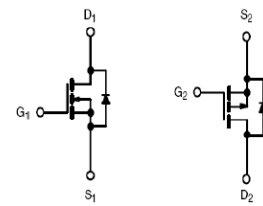
N-Channel Mosfet   **P-Channel Mosfet**

Schematic diagram

Features and Benefits:

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150℃ operating temperature

Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

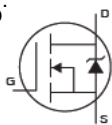| Symbol	Parameter	Max.		Units
		N-Channel	P-Channel	
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V (Silicon Limited)	4 ①	-3.6 ①	A
I_{DM}	Pulsed Drain Current ②	16	-14.4	
V_{GS}	Gate to source voltage	±12	±12	V
P_D @TC = 25°C	Power Dissipation ③	2.1	1.3	W
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	-55 to + 150	°C

Thermal Resistance

Symbol	Characterizes	Typ.	Max.		Units
			N-channel	P-Channel	
$R_{θJA}$	Junction-to-ambient ($t \leqslant 5s$) ④	—	60	95	℃/W

Electrical Characterizes @T$_A$=25℃ unless otherwise specified

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source breakdown voltage	N-channel	30	—	—	V	V$_{GS}$ = 0V, I$_D$ = 250µA
		P-Channel	-30	—	—		V$_{GS}$ = 0V, I$_D$ = -250µA
R$_{DS(on)}$	Static Drain-to-Source on-resistance	N-channel	—	32.4	36	mΩ	V$_{GS}$= 4.5V,I$_D$ = 4.8A
		P-Channel	—	61.6	65		V$_{GS}$= -4.5V,I$_D$ = -2.3A
V$_{GS(th)}$	Gate threshold voltage	N-channel	0.5	—	2	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 250µA
		P-Channel	-0.5	—	-2		V$_{DS}$ = V$_{GS}$, I$_D$ = -250µA
I$_{DSS}$	Drain-to-Source leakage current	N-channel	—	—	1	µA	V$_{DS}$ =30V,V$_{GS}$ = 0V
		P-Channel	—	—	-1		V$_{DS}$ =-30V,V$_{GS}$ = 0V
I$_{GSS}$	Gate-to-Source forward leakage	N-channel	—	—	100	nA	V$_{GS}$ =12V
		N-channel	-100	—	—		V$_{GS}$ = -12V
		P-Channel	—	—	100		V$_{GS}$ =12V
		P-Channel	-100	—	—		V$_{GS}$ =-12V

Source-Drain Ratings and Characteristics

| Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
I$_s$	Continuous Source Current	N-channel	—	—	4	A	MOSFET symbol showing the integral reverse p-n junction diode.
		P-Channel	—	—	-3.6		
I$_{SM}$	Pulsed Source Current	N-channel	—	—	16	A	
		P-Channel	—	—	-14.4		
V$_{SD}$	Diode Forward Voltage	N-channel	—	0.82	1.2	V	I$_S$=2.4A, V$_{GS}$=0V
		P-Channel	—	-0.85	-1.2		I$_S$=-1.5A, V$_{GS}$=0V

Test circuits and Waveforms:

Switch Time Test Circuit:
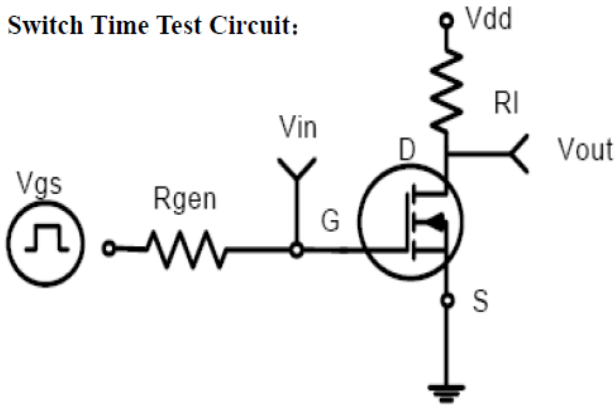
Switching time waveform:
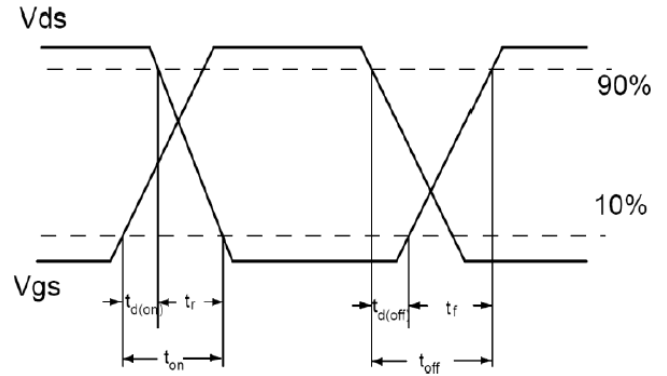
Notes:

①The maximum current rating is limited by bond-wires.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of RθJA is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C
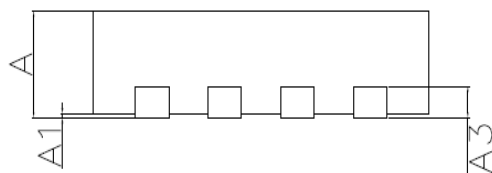
Thermal characteristics
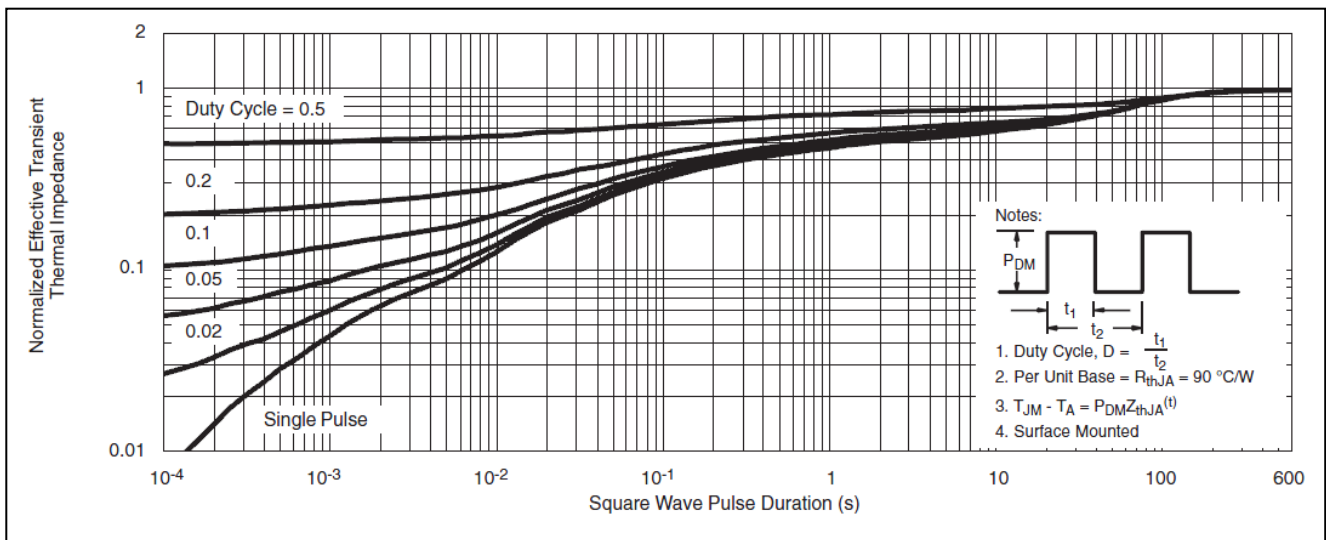
Figure1. Normalized Thermal Transient Impedance, Junction-to-Ambient

Mechanical Data：

DFN 3X2_8L PACKAGE OUTLINE DIMENSION

TOP VIEW

PIN 1 DOT
BY MARKING
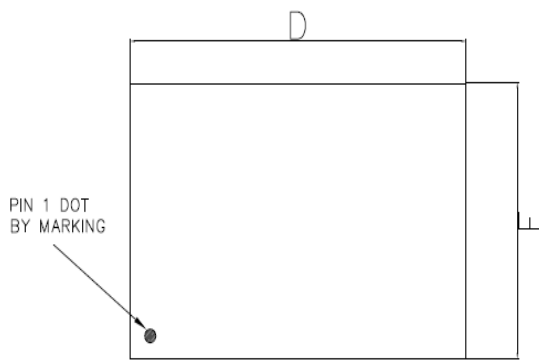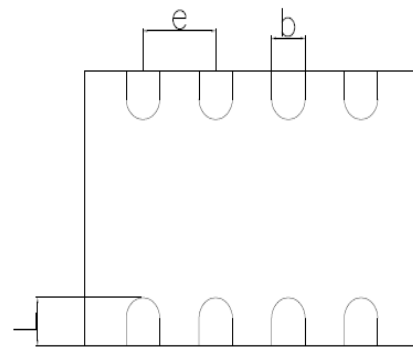
BOTTOM VIEW

SIDE VIEW

Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A3	0.200REF			0.008REF		
D	2.950	3.000	3.050	0.116	0.118	0.120
E	1.950	2.000	2.050	0.077	0.079	0.081
b	0.250	0.300	0.350	0.010	0.012	0.014
L	0.280	0.350	0.420	0.016	0.014	0.017
e	0.650BSC			0.026BSC		

Ordering and Marking Information

Device Marking: 3036C

Package (Available)
DFN 3x2-8L
Operating Temperature Range
C : -55 to 150 ⁰C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
DFN 3x2-8L	3000pcs	10pcs	30000pcs	4pcs	120000pcs

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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