PAH8002EP: Low Power Optical Heart Rate Detection Chip

General Description

The PAH8002EP is a low power and high-performance CMOS-process optical chip with three LEDs: two Green and one Infrared, and integrated DSP, targeted as a Heart Rate Detection (HRD) chip. It is based on optical sensing technology that captures higher resolution image than the traditional photodiode. The images are then processed through our integrated DSP to attain processed PPG (Photoplethysmogram) data for use in deducing heart rate.

Key Features

- Heart rate detection function (HRD)
- SRAM buffer support
- Integrated ultra-low power mode, while in Sleep mode
- Adjustable sleep rate control
- Communication interface options
  - I²C
  - Four-Wire SPI
- I²C interface up to 1 Mbit/s
- SPI interface up to 2 Mbit/s
- Hardware reset support
- Integrated chip-on-board LEDs with wavelength of 525nm and 940nm

Applications

- Heart Rate Monitor Accessories
- Wearables: Smartwatch, Wrist Band

*Disclaimer:

The PAH8002EP-2P is not designed for usage in medical device. In addition, the data and information of heart rate measurement provided by this chip may not be completely accurate and may exceed heart rate tolerance as per the specification stated in the document due to different factors, such as interference with signal from external sources, incorrect wearing position and changes in weather conditions or user's body condition.

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Key Parameters

Parameter	Value
Operating Temperature, Tj (°C)	-20 to +60
Array Size	1 pixel
Pixel Size (µm)	780 x 780
Max Frame Rate (fps)	50K
Dynamic Range (dB)	70
Supply Voltage (V)	VDDM: 3.3 – 3.6 VDD_LEDx: 3.3 – 3.6 VDDIO: 1.62 – 3.6 Analog: 2.8 Digital: 1.8

Power Consumption (mW) @3.3V
Note: Including LED current, without I/O toggling, package only
	Active:
	■ Double Injection Type :
	  4.95 with one LED
	  8.25 with two LEDs
	  0.165 with IR Touch Detection
	■ Printing Cover Type:
	  5.94 with two LEDs
	  0.165 with IR Touch Detection
	Sleep: 0.08

Heart Rate Measurement Range (bpm)	30 - 240
Package Size (mm)	3.6 x 6.36 x 1.0

Ordering Information

Part Number	Package Type
PAH8002EP-2P	22-Pin LGA

RoHS compliant

For any additional inquiries, please contact us at
http://www.pixart.com/contact.asp

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1.0 Introduction

1.1 Overview

The PAH8002EP is a low power and high-performance CMOS-process optical chip, targeted as a Heart Rate Detection (HRD) chip. It is built-in with 2 Green LEDs, 1 Infrared LED and integrated DSP It comes with two communication interfaces, which are I^2C supporting up to 1 Mbit/s and Four-Wire SPI supporting up to 2 Mbit/s. SRAM buffer of 832 bytes is supported for the power saving at the host.

The Figure 1 shows the architecture block diagram of the device. Refer to the subsequent chapters for detailed information on the functionality of the different interface blocks.

Note: Throughout this document PAH8002EP low power Optical CMOS Heart Rate Chip is referred to as the chip.
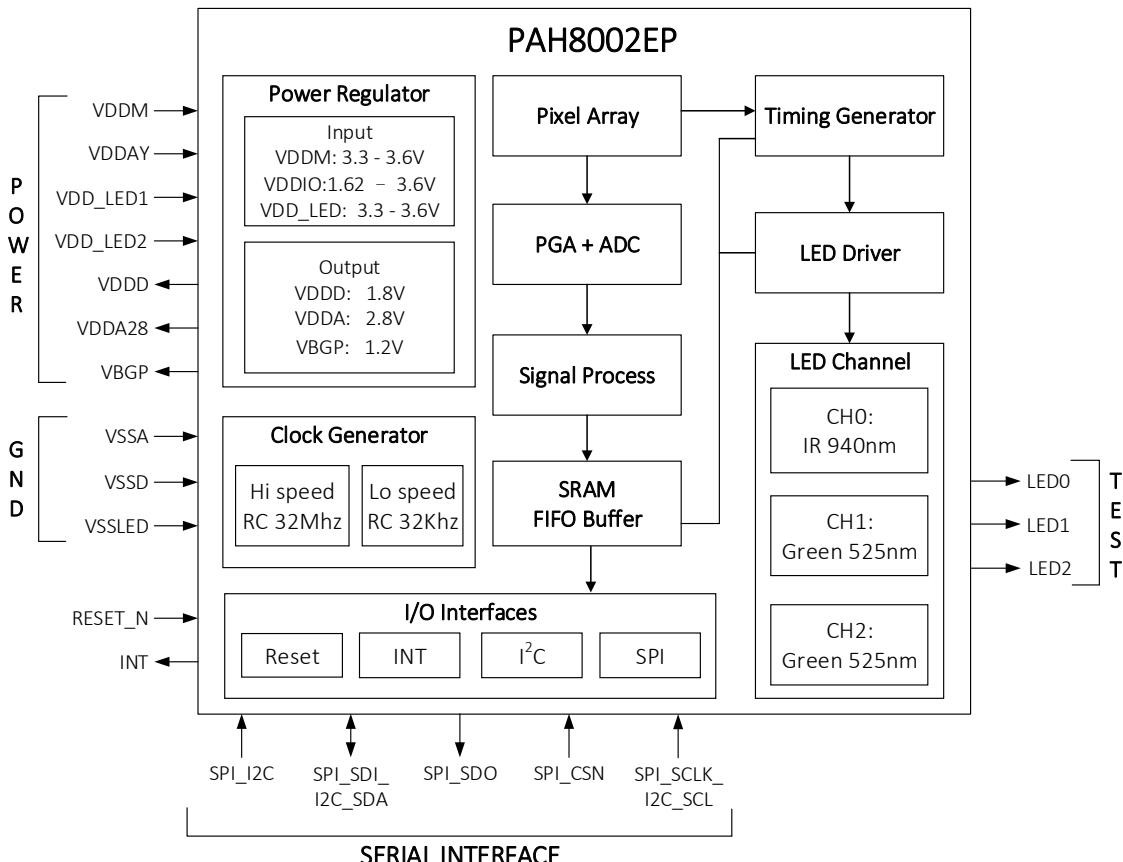
Figure 1. Functional Block Diagram

1.2 Terminology

Term	Description
GND	Ground
BiDir	Bi-Directional
PPG	Photoplethysmogram
Touch	Touch detection for wear on or wear off
SW reset	Software reset by register

1.3 Signal Description
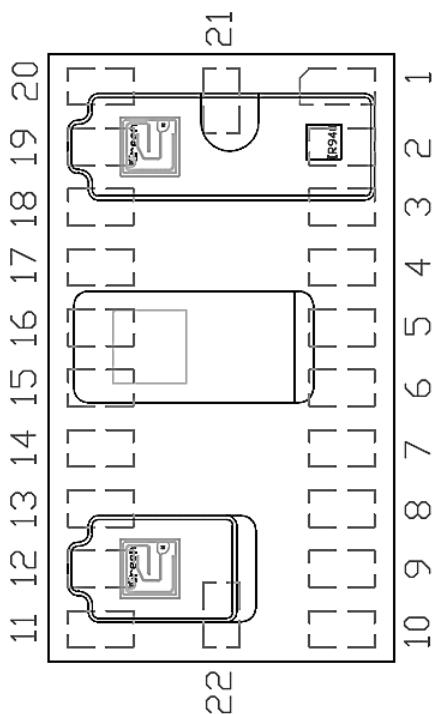
Figure 2. Pin Configuration

Table 1. Signal Pins Description

Pin No.	Signal Name	Type	Description
Functional Group:		Power Supplies	
1	VDD_LED01	Input	IR/Green LED Anode. Provide VDDM supply voltage
2	VDDAY	Input	Analog circuit power regulator input. Connect to VDDA28 or provide 2.8V voltage
3	VDDA28	Output	Analog circuit power regulator output. Must connect 1μF capacitor to GND
4	VDDD	Output	Digital circuit power regulator output. Must connect 1μF capacitor to GND
5	VBGP	Output	Reference regulator output. Must connect 0.1μF capacitor to GND
7	VDDM	Input	Power supply (3.3 - 3.6V) for internal power regulator
8	VSSLED	GND	LED Ground
15	VSSD	GND	Digital Ground
19	VDDIO	Input	I/O Power Supply (1.62 - 3.6V)
20	VSSA	GND	Analog Ground
s22	VDD_LED2	Input	Green LED Anode. Provide VDDM supply voltage
Functional Group:		Interface	
11	SPI_SDI_I2C_SDA	BiDir	4-wire SPI: Data input I^{2}C: Data input-output
12	SPI_SDO	Output	4-wire SPI: Data output
13	SPI_CSN	Input	4-wire SPI: Chip Select. Active Low
14	SPI_SCLK_I2C_SCL	Input	4-wire SPI/ I^{2}C: Clock

Pin No.	Signal Name	Type	Description
Functional Group:		Functional I/O	
16	INT	Output	Data ready interrupt. Default is edge sensitive interrupt, can be changed to level sensitive interrupt (high active) in INT Type register
17	SPI_I2C	Input	Interface Selection I^{2}C: Pull down (Tie to GND) 4-wire SPI: Pull high (Tie to VDDIO)
18	RESET_N	Input	Hardware control to enter Reset Mode. Connect to VDDIO when not used Level High: Leave Reset Mode Level Low: Enter Reset Mode
Functional Group:		Reserved	
9	LED0	RSV	Reserved for LED0 test pin
6	LED1	RSV	Reserved for LED1 test pin
10	LED2	RSV	Reserved for LED2 test pin
21	NC	RSV	Reserved. No Connection

2.0 Operating Specifications

2.1 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit	Notes
Analog Voltage	V_{DDM_MAX}	-0.4	$V_{DDM} + 0.3$	V	
I/O Voltage	V_{DDIO_MAX}	-0.4	$V_{DDIO} + 0.3$	V	
I/O Pin Input High Voltage	V_{DDIO_IN}	-0.4	$V_{DDIO} + 0.3$	V	All I/O pins
Relative Humidity	RH	0	50	%	Non-condensing, Non-biased
ESD	ESD_{HBM}		2	kV	Class 2 on all pins, as per human body model. JESD22-A114E with 15 sec zap interval.

Notes:

1. At room temperature.
2. Maximum Ratings are those values beyond which damage to the device may occur.
3. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability.
4. Functional operation under absolute maximum-rated conditions is not implied and should be restricted to the Recommended Operating Conditions.

2.2 Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Description	Symbol	Min.	Typ.	Max.	Unit	Notes
Ambient Temperature	T_A	-20	25	60	°C	
Operating Junction Temperature	T_J	-20	-	60	°C	
Power Supply Voltage	V_{DDM}	3.25	3.3	3.6	V	Power regulator input supply. Includes ripples
Analog Supply Voltage	V_{DDAY}	2.66	2.8	2.94	V	If supply from external power regulator. Includes ripples
I/O Supply Voltage	V_{DDIO}	1.62	1.8	3.6	V	Includes ripples
Power Regulator Output Voltage	V_{DDD}	1.62	1.8	1.98	V	For digital circuit. Includes ripples
	V_{DDA28}	2.52	2.8	3.08	V	For analog circuit to be connected to V_{DDAY}. Includes ripples
	V_{BGP}	1.08	1.2	1.32	V	For power regulator reference. Includes ripples
Supply Noise	V_{Npp}	-	-	100	mV_{p-p}	Peak to peak within 10K – 80 MHz
Serial Clock Frequency	SCK_SPI	-	-	2	MHz	
	SCK_I²C	-	400[1]	1000[2]	KHz	1. Max value for Fast mode 2. Max value for Fast mode plus

Note: PixArt does not guarantee the performance if the operating temperature is beyond the specified limit.

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2.3 Thermal Specifications

Table 4. Thermal Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T_S	-25	-	125	°C	
Lead-free Solder Temperature	T_P	-	-	245	°C	Refer to Package Handling Information document

2.4 DC Characteristics

Table 5. DC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Peak Power Supply Current	I_{DDM_MAX}	-	-	100	mA	For V_{DDM}
	I_{DDAY_MAX}	-	-	10	mA	For V_{DDAY}
Peak I/O Supply Current	I_{DDIO_MAX}	-	-	1	mA	For V_{DDIO}
Output Supply Current	I_{DDD_MAX}	-	-	80	mA	For V_{DDD}
Output Supply Current	I_{DDA28_MAX}	-	-	20	mA	For V_{DDA28}
Power Consumption						
Supply Current @ Sleep	I_{DDPD}	-	25	75	uA	For chip only Wakeup by read register
Inrush Current	I_{INRUSH}	-	-	60	mA	
With One Green LED						
Supply Current @ HRD PPG Double Injection Type	I_{DDHRD}	-	1.2	-	mA	For chip only, not including LED current, without I^{2}C interface I/O toggle
LED current	I_{DDLED}	-	0.3	-	mA	20 report/sec, LED DAC = 50mA, on yellow skin color
With Two Green LEDs						
Supply Current @ HRD PPG Double Injection Type	I_{DDHRD}	-	1.7	-	mA	For chip only, not including LED current, without I^{2}C interface I/O toggle
LED current	I_{DDLED}	-	0.8	-	mA	20 report/sec, LED DAC = 50mA, on yellow skin color
With Two Green LEDs						
Supply Current @ HRD PPG Printing Cover Type	I_{DDHRD}	-	0.6	-	mA	For chip only, not including LED current, without I^{2}C interface I/O toggle
LED current	I_{DDLED}	-	1.2		mA	20 report/sec, LED DAC = 50mA, on yellow skin color
With IR Touch Detection						
Supply Current @ Touch Detection mode	$I_{DDtouch}$		45		uA	For chip only, not including LED current, without I^{2}C interface I/O toggle
LED current at touch	I_{DDLED}	-	5	-	uA	3.8 report/sec, LED DAC = 50mA, on yellow skin color

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Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
I/O						
Input High Voltage	V_{IH}	0.7* V_{DDIO}	-	-	V	
Input Low Voltage	V_{IL}	-	-	0.3* V_{DDIO}	V	
Output High Voltage	V_{OH}	V_{DDIO} - 0.4	-	V_{DDIO} + 0.4	V	@I_{OH} = 2mA
Output Low Voltage	V_{OL}	-0.4	-	0.4	V	@I_{OL} = 2mA
LED						
Sink current	I_{LED}	40	50	60	mA	@ LED DAC = 50mA
LED cathode voltage	V_{LED-}	0.4		3.6	V	

Notes:
1. Electrical Characteristics are defined under recommended operating conditions.
2. All the parameters are tested under operating conditions: V_{DDM} = 3.3V, V_{DDIO} = 1.8 and 3.3V, T_A = 25°C

2.5 AC Characteristics

Table 6. AC Electrical Specifications

Parameters	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power Up from V_{DD}↑	t_{PU}	200	300	400	ms	From V_{DD}↑ to valid interface communication
SDI/SDO Read Hold Time	T_{HOLD}	-	3	-	us	Minimum hold time for valid data.
Address and data delay time	t_{delay}	2.75			us	Refer to Serial Interface section
Chip Pulse Interrupt Width	t_{INT}	0.00625	0.5	16	us	Default 0.5us, can be changed in INT_Pulse_Width register
Rise and Fall Times: SDI/SDO	t_r , t_f	-	30	-	ns	C_L = 30 pF
HW Reset Time	t_{reset}	200	300	400	ms	Reset_N from low to high period

Notes:
1. Electrical Characteristics are defined under recommended operating conditions
2. All the parameters are tested under operating conditions: T_A = 25°C, V_{DDM} = 3.3V, V_{DDIO} = 3.3V for 3.3V IO application and V_{DDIO} = 1.8 V for 1.8V IO application.

## 3.0 Mechanical Specifications

3.1 Mechanical Dimension
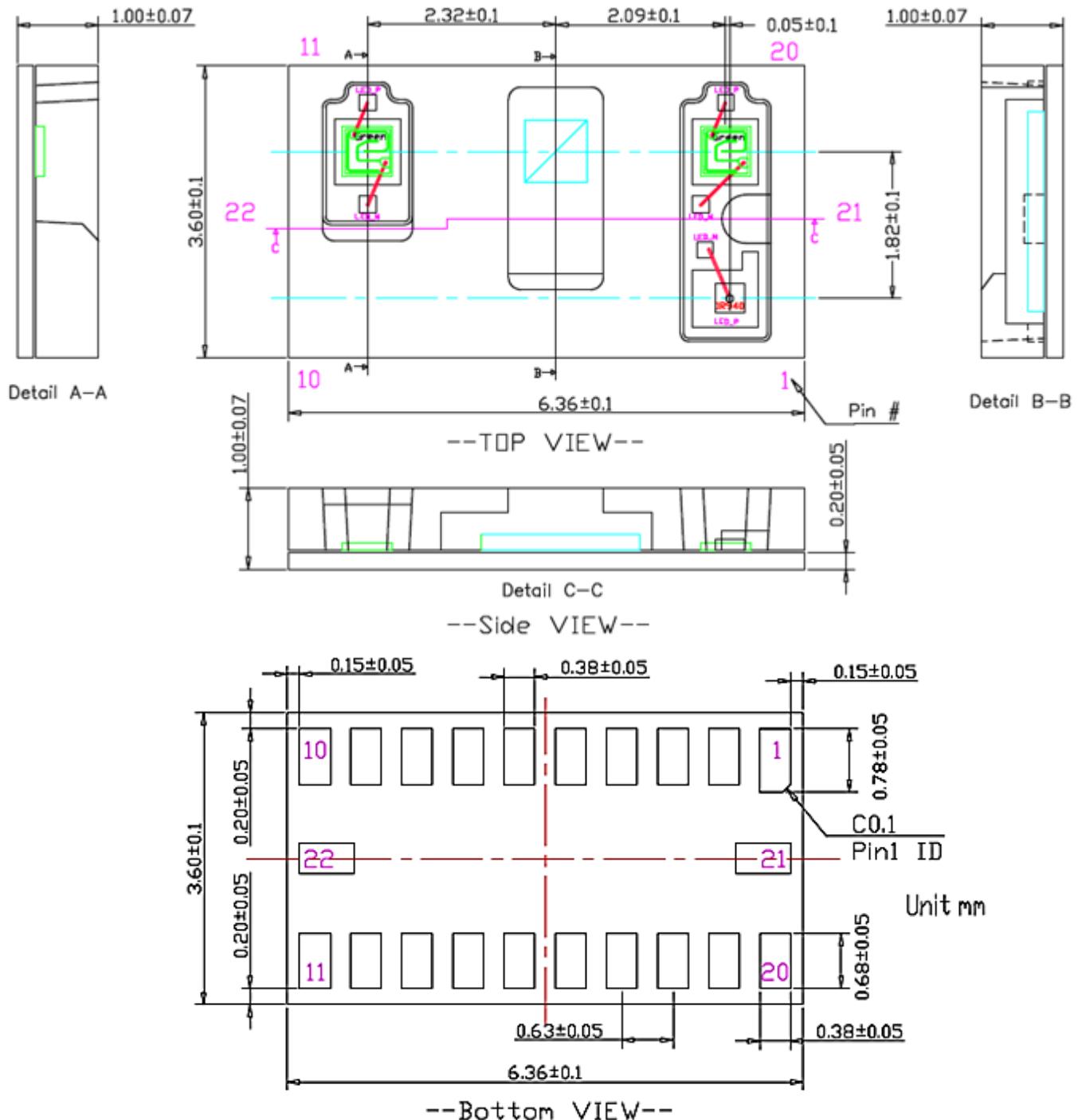
Figure 3. Package Outline Diagram

3.2   Package Marking

Refer to Figure 4. Package Marking for the code marking location on the device package.
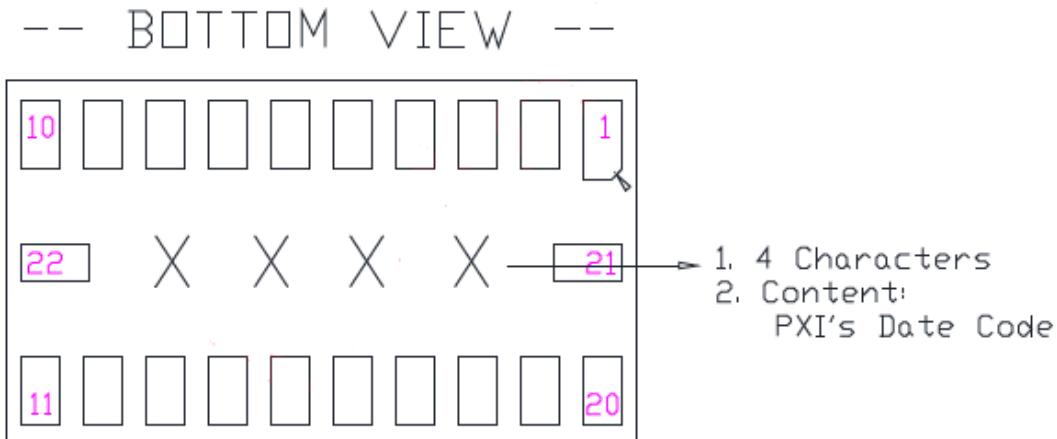
Figure 4. Package Marking

Table 7. Code Identification

Marking	Description
XXXX	PixArt Date Code

4.0 System Level Description

4.1 System Overview

This section describes on how the chip being used to make up a complete system including the explanation on the 3rd party components and how they work with the chip.

The PAH8002 is based on CMOS image chip technology. It is designed to meet the requirements as heart rate monitor accessories and wearables like smart watch or wrist band device. Figure 5 illustrates a system design for App Level diagram. The processor is accessing PPG data from 8002 chip, then pass it to App level. APP level applies PixArt provided algorithm library to determine the heart rate data and waveform. Figure 6. System Design for Firmware Level illustrates a system design for Firmware Level diagram. The processor will also access PPG data from 8002 chip, then perform heart rate calculation with PixArt algorithm library and send result to display or end device.

PAH8002 can be configured to generate different frame rate settings up to 50K fps.
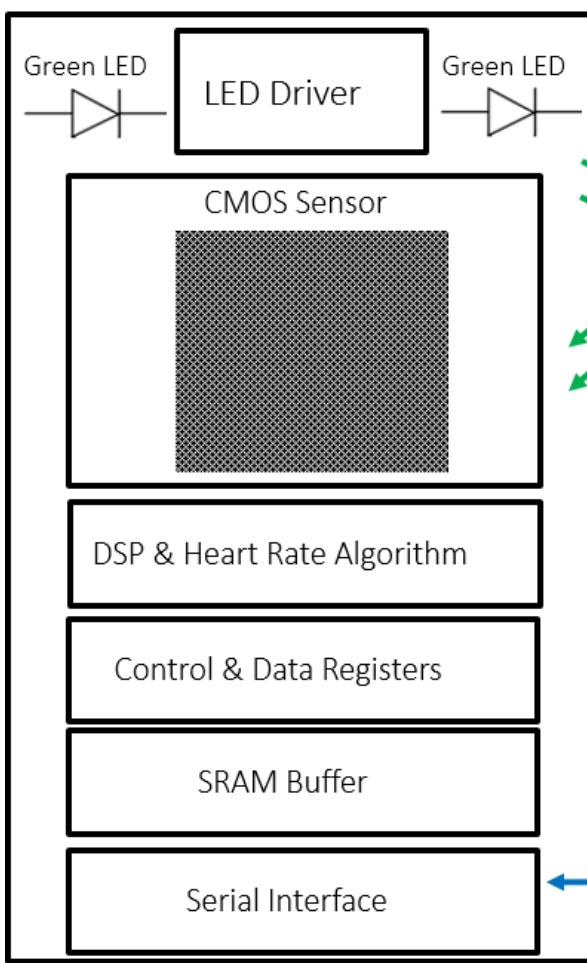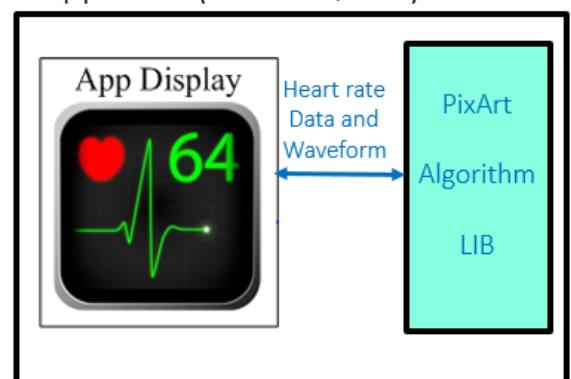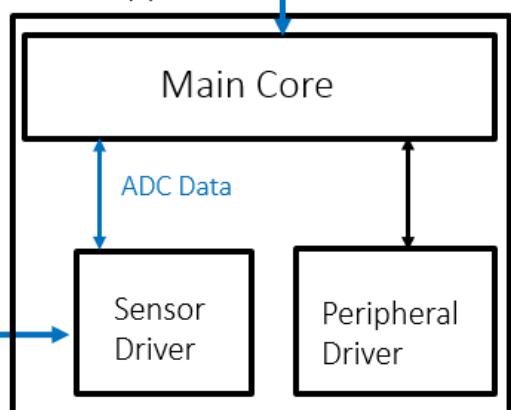
Figure 5. System Design for App Level
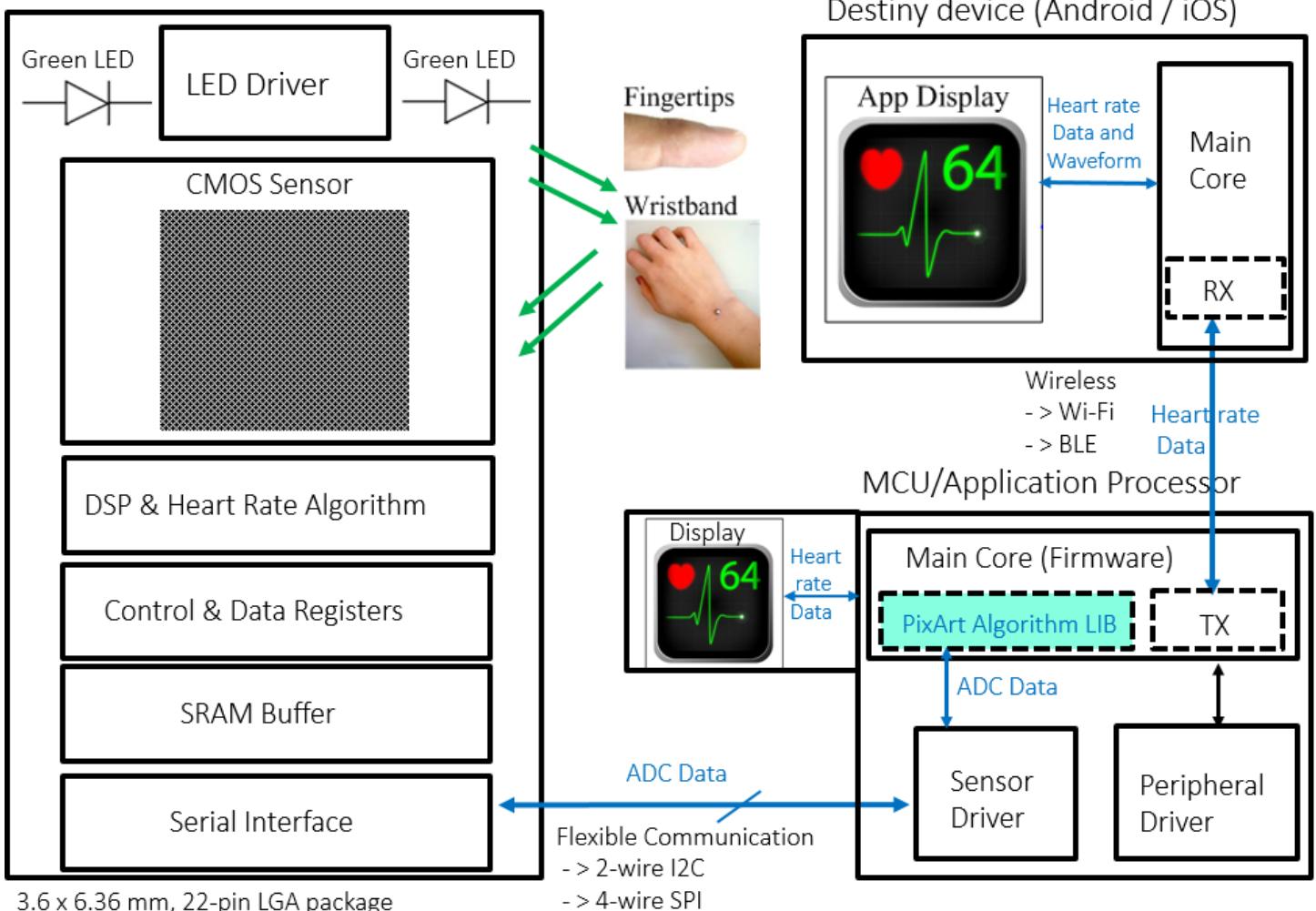
Figure 6. System Design for Firmware Level

4.2 Heart Rate Detection

Heart rate detection is an optical measurement technique that uses a light source and a detector to detect cardiovascular pulse wave that propagates through the body. The detected signal (pulse wave) called photoplethysmography and it is known as PPG/PTG. The PPG signal reflects the blood movement in the vessel, which goes from the heart to the fingertips through the blood vessels in a wave-like motion. Therefore, we can use this PPG signal to calculate heart rate.

This optical based technology could offer significant benefits in healthcare application as it is noninvasive, yet accurate and simple to use.

4.2.1 Applications

- Heart rate detection in general healthcare (Perfusion Index : Typ.1%)
- PPG Waveform

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4.2.2   Heart Rate Detection Performance

Parameters	Value	Unit	Conditions
Heart Rate Measurement Range	30 - 240	bpm	
Heart Rate Tolerance of Root Mean Square (RMS)	±3	bpm	@ Room temperature for steady state: 0 km/hr.
	±5	bpm	@ Room temperature for motion state: 0 – 9 km/hr on the treadmill.
Response Time	8 - 10	second	@ Heart Rate = 72/bpm

Notes:
- PAH8002EP can provide heart rate measurement. However, it is not for medical device usage.
- For usage of heart rate detection chip on the wearable device that to be put on the wrist, finger or palm,
  - The chip must be placed securely and in-contact with the skin surface as well as keeping it stable without any motion during measurement in acquiring accurate heart rate measurement.
  - Do not wear the device on the wrist bone. It should be wear on the higher position of, especially for those with a smaller wrist.
- Chip's performance is optimized with good blood flow. It is recommended to have light exercise for a few minutes to increase your blood flow before turning on the heart rate monitor.
- On cold weather condition or user is having poor blood circulation (e.g.: cold hands, fingers and feet), the chip performance (heart rate accuracy) could be effected as the blood flow is slower in the measuring spot position. It is recommended to activate the heart rate monitor in indoor use.
- If the chip is having problem to read heart rate, may try to swap it on the other side of hand wrist to repeat the measurement.
- For continuous heart rate measurement, do minimize hand movement and extreme bending of the wrist.

4.3   Reference Schematic

### 4.3.1   Schematic Design- Double Injection Type
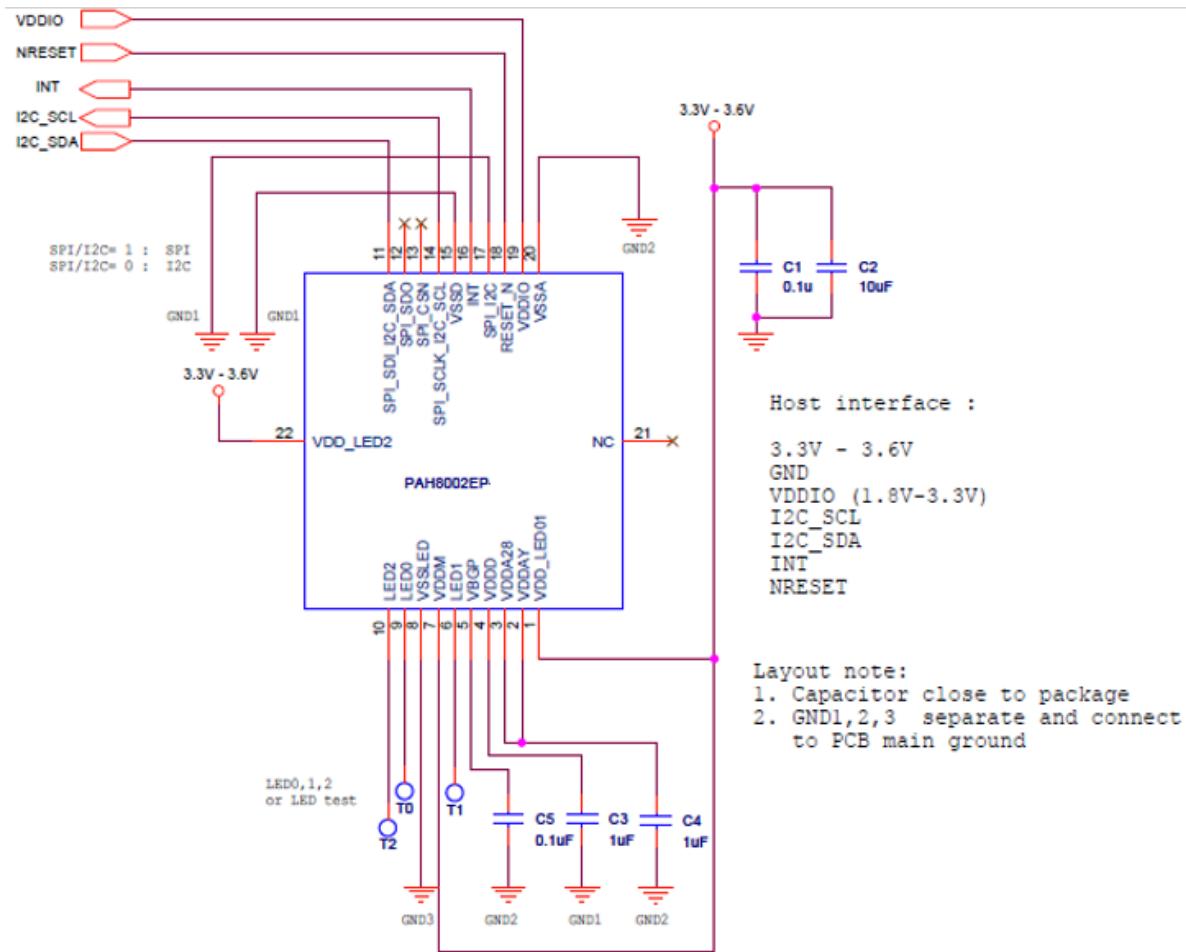
Figure 7. Reference Application Circuit –Double Injection Type

4.3.2 Schematic Design- Printing Cover Type
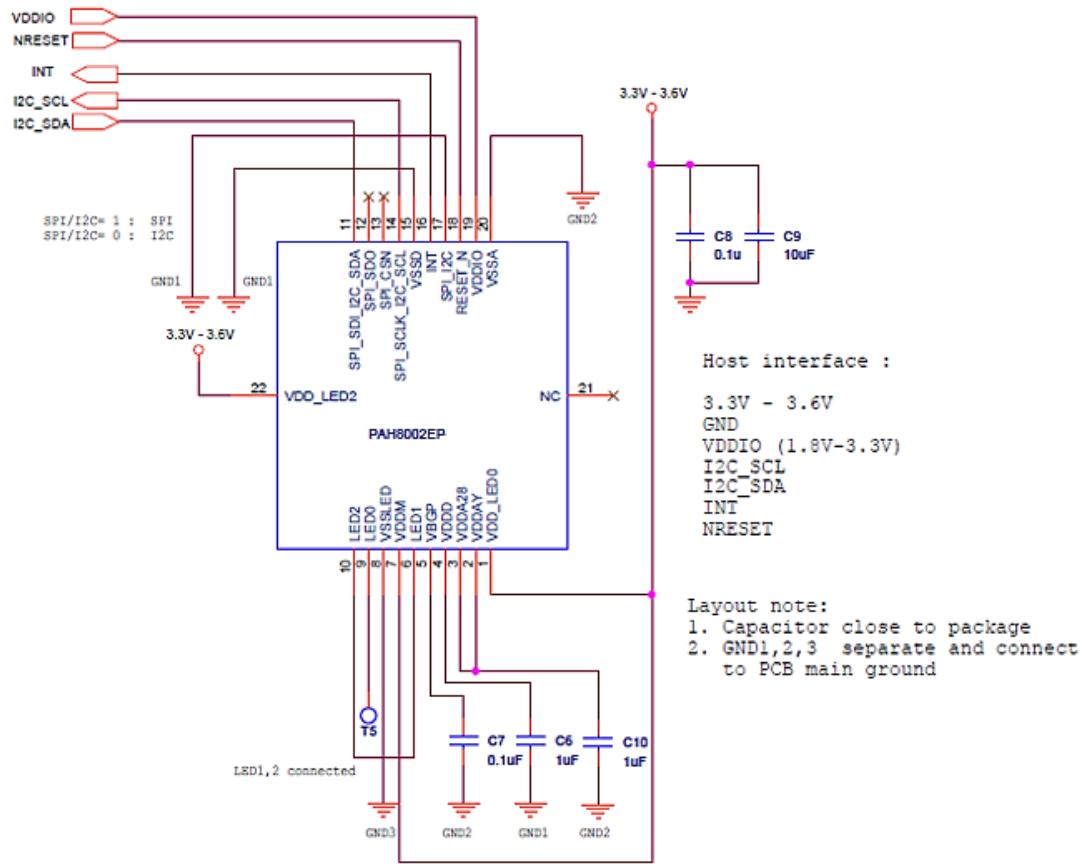
Figure 8 Reference Application Circuit–Printing Cover Type

4.4 Design Guidelines

4.4.1 Schematic Design

1. VDDM & VDDIO: 3.3V~3.6V (for 3.3V System)
2. VDDM: 3.3V~3.6V, VDDIO: 1.62V~1.98V (for 1.8V System)
3. It is recommended to separate the power system for VDDM to avoid power interference.
4. SPI_SDI_I2C_SDA and SPI_SCLK_I2C_SCL pull high to VDDIO with resistor for I²C Only
5. VDDD, VDDA28 must have 1µF and VBGP must have 0.1µF capacitor connecting to GND and place closely to 8002.
6. The GND1, GND2 and GND3 must be separated and connected to PCB main GND.
7. INT pin is recommended to be connected to MCU HW INT as data ready INT for power saving.
8. Ensure that the VDDM and VDDIO's power noise should be under 100mV (with 0.1µF and 10µF capacitor)
9. Tie SPI_I2C pin to VDDIO for SPI or tie to GND for I²C.
10. At power on, VDDM and VDDIO must be powered on at the same time or VDDIO to be powered on before VDDM.
    ※When VDDIO to be powered on before VDDM, the host should prevent using the I²C interface (that is connected with 8002) to switch on the LDO providing VDDM voltage.
11. At power off, VDDM and VDDIO must be powered off at the same time or VDDM to be powered off first before VDDIO.

4.4.2   Recommended Layout Information of Main Board

4.4.2.1   Pad Dimension on PCB/FPC

1. Pad size design:
    - If use solder mask defined (SMD), pad size is referred as solder mask opening size.
    - If use non-solder mask defined (non-SMD), pad size is referred as copper metal size.
2. Recommended dimension of pad is shown in below figure. The actual pad size design will need to consider components aside.

    (Refer to Figure 9. Recommended Layout PCB).
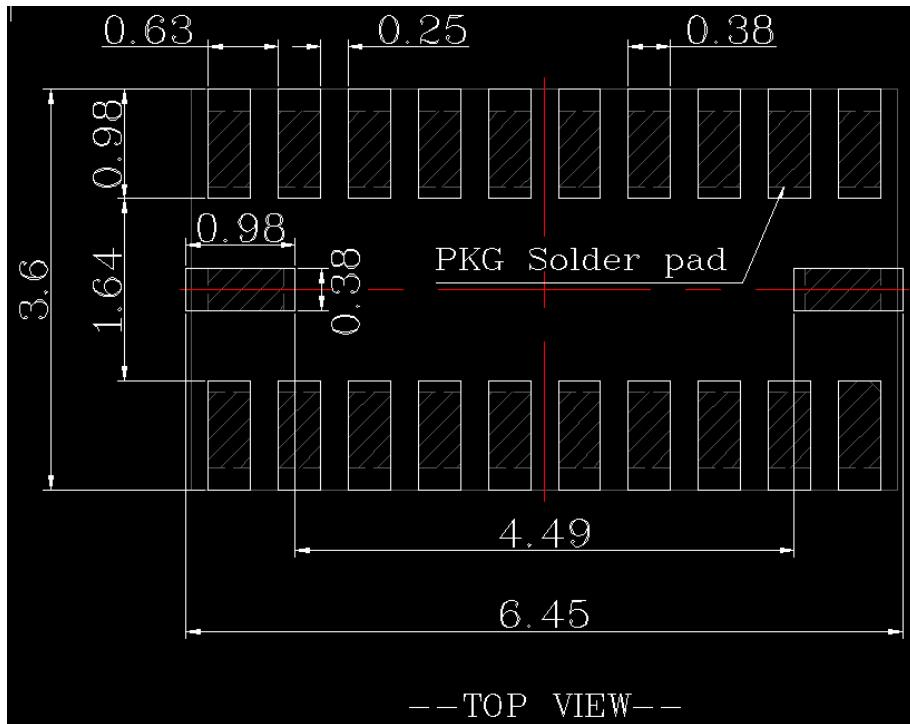
Notes: All dimension is mm.

Figure 9. Recommended Layout PCB

4.4.2.2   Recommended Stiffener type for FPC (Flex) back-side (at Sensor package area)

1. If use FPC (Flex) board, stiffener is required to be added onto the back of FPC (Flex) to enhance the Flex strength.
2. Recommended Stiffener type: FR4 or stainless steel.
3. Recommended stiffener thickness: minimum 0.4mm for FR4 type, minimum 0.15mm for stainless steel.

4.4.2.3   Recommended use 0.1~0.12mm thickness stencil for SMT process.

1. The stencil thickness selection will need to consider passive component size aside package.
2. In case of the package is surface mounted on FPCB (Flexible Printed Circuit Boards), the overall thickness of cover layer & adhesive layer is recommenced to be controlled under than 40μm.

4.4.2.4 PCB Layout Guidelines

The following guidelines can be refer to Figure 10. PCB Layout Guide.

1. Capacitor 0.1μF and 1μF must be placed close to the chip package.
2. The GND plane of GND of VSSA, VSSD and VSSLED must be layout separately and connected to the PCB's main GND.

Figure 10. PCB Layout Guide

S E E. F E E L. T O U C H.
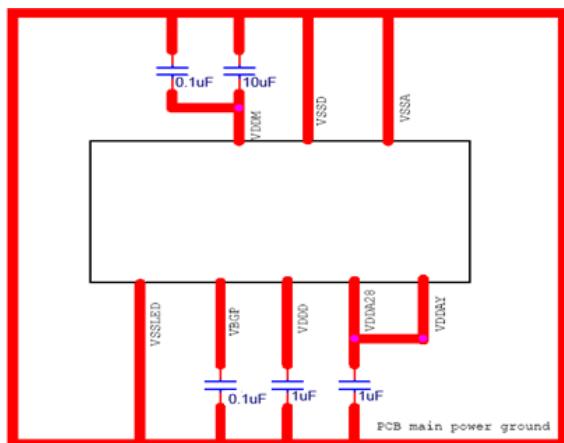
4.5   Recommend Guideline for PCB Assembly

Recommended vendor and type for Pb-free solder paste

- Almit LFM-48W TM-HP
- Senju M705-GRN360-K

IR Reflow Soldering Profile can be refer to Figure 11. IR Reflow Soldering Profile.

Temperature profile is the most important control in reflow soldering. It must be fine-tuned to establish a robust process. The typical recommended IR reflow profile is:
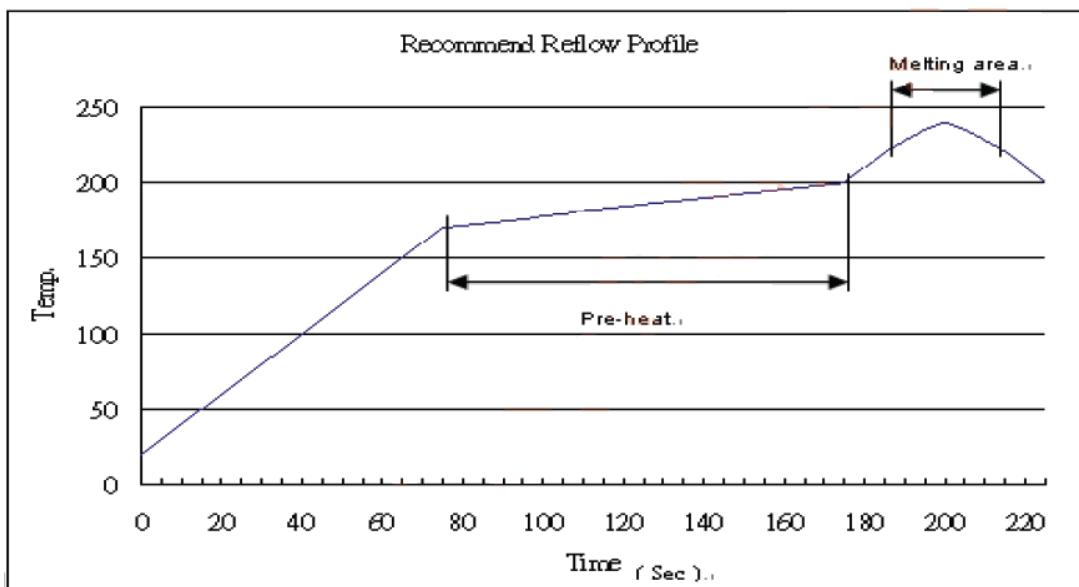
Figure 11. IR Reflow Soldering Profile

Note:
(1) Average Ramp-up Rate (30℃ to preheat zone): 1.5~2.5℃/Sec
(2) Preheat zone:
    (2.1) Temperature ramp from 170~200℃
    (2.2) Exposure time: 90 +/- 30 sec
(3) Melting zone:
    (3.1) Melting area temperature > 220℃ for at least 30~50sec
    (3.2) Peak temperature: 245℃
MS Level: MS Level 3

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4.6 Package Information

4.6.1 Carrier Tape Drawing
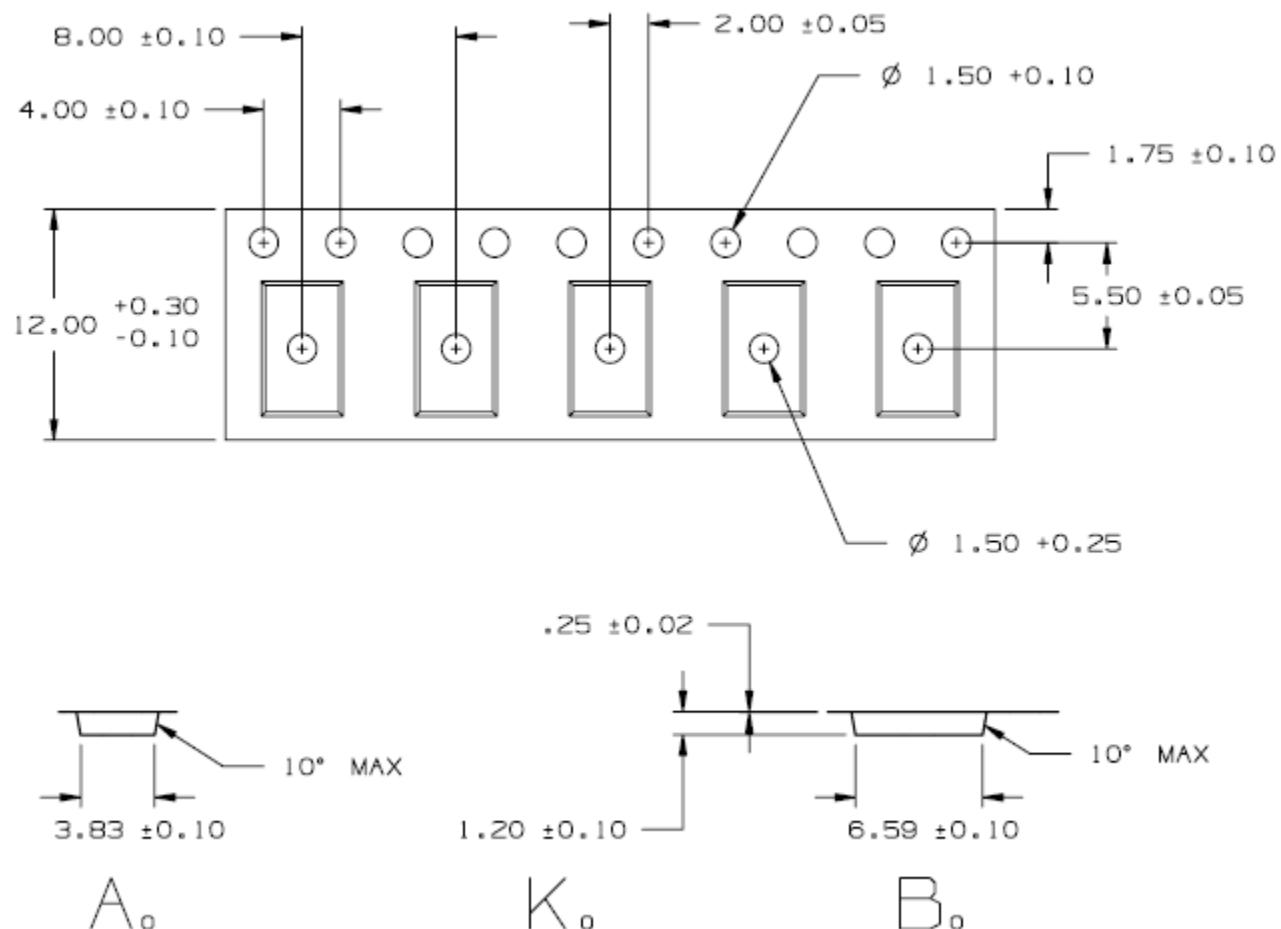
Figure 12. Carrier Tape Drawing

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4.6.2   Unit Orientation
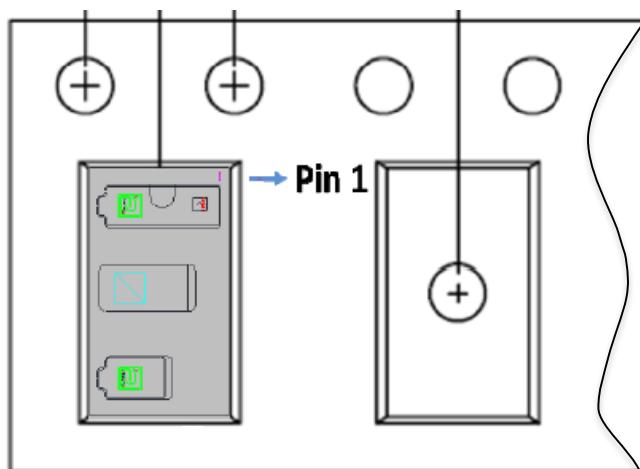
Figure 13. Unit Orientation

The maximum capacity of one packing box for PAH8002EP-2P: One Inner packing box = 2500 units
Note: The Tape and Reel packing with vacuum pack is 1year storage available @ 25°C, 50%RH

5.0 Registers List

Table 8. Register Bank0

Note: Switch to Register Bank0 by writing 0x00 to Reg-0x7F

| Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x00	Product_ID_LB	RO	0x02	0x6E	AE_Ch0_Mid_HB	R/W	0x00
0x01	Product_ID_HB	RO	0x80	0x6F	AE_Ch0_Max_LB	R/W	0xF0
0x02	Version_ID	RO	0xDx	0x70	AE_Ch0_Max_HB	R/W	0x00
0x0D	Ch0_Man_ET_LB	R/W	0xC8	0x71	AE_Ch0_Min_LB	R/W	0x52
0x0E	Ch0_Man_ET_HB	R/W	0x00	0x72	AE_Ch0_Min_HB	R/W	0x00
0x0F	Ch1_Man_ET_LB	R/W	0xA0	0x77	AE_Ch0_Outerbound_Hi_LB	R/W	0x00
0x10	Ch1_Man_ET_HB	R/W	0x00	0x78	AE_Ch0_Outerbound_Hi_HB	R/W	0x06
0x11	Ch2_Man_ET_LB	R/W	0x78	0x79	AE_Ch0_Outerbound_Lo_LB	R/W	0x00
0x12	Ch2_Man_ET_HB	R/W	0x00	0x7A	AE_Ch0_Outerbound_Lo_HB	R/W	0x02
0x16	Ana_BG	R/W	0x00	0x7B	AE_Ch0_Innertarget_Hi_LB	R/W	0x00
0x3B	Ch0_Samp_Num	R/W	0x32	0x7C	AE_Ch0_Innertarget_Hi_HB	R/W	0x05
0x3C	Ch1_Samp_Num	R/W	0x20	0x7D	AE_Ch0_Innertarget_Lo_LB	R/W	0x00
0x3D	Ch2_Samp_Num	R/W	0x20	0x7E	AE_Ch0_Innertarget_Lo_HB	R/W	0x03
0x47	Ch0_Global_EnH	R/W	0x01	0x85	AE_LED0_DAC_Min	R/W	0x01
0x48	Ch1_Global_EnH	R/W	0x00	0x8E	AE_LED0_DAC_EnH	R/W	0x01
0x49	Ch2_Global_EnH	R/W	0x00	0x8F	AE_Ch1_EnH	R/W	0x01
0x4A	LED0_Sub_EnH	R/W	0x00	0x90	AE_Ch1_Mid_LB	R/W	0xA0
0x4B	LED1_Sub_EnH	R/W	0x01	0x91	AE_Ch1_Mid_HB	R/W	0x00
0x4C	LED2_Sub_EnH	R/W	0x01	0x92	AE_Ch1_Max_LB	R/W	0xF0
0x4D	LED_OnOff_Swap	R/W	0x01	0x93	AE_Ch1_Max_HB	R/W	0x00
0x50	Normalized_Mode_EnL_1	R/W	0x00	0x94	AE_Ch1_Min_LB	R/W	0x52
0x51	Normalized_Mode_EnL_2	R/W	0x00	0x95	AE_Ch1_Min_HB	R/W	0x00
0x56	Normalized_Right_Shift	R/W	0x07	0x9A	AE_Ch1_Outerbound_Hi_LB	R/W	0x00
0x5A	Touch_Detect_EnH	R/W	0x00	0x9B	AE_Ch1_Outerbound_Hi_HB	R/W	0x06
0x5C	TouchDetection_Upper_TH_1	R/W	0x00	0x9C	AE_Ch1_Outerbound_Lo_LB	R/W	0x00
0x5D	TouchDetection_Upper_TH_2	R/W	0x02	0x9D	AE_Ch1_Outerbound_Lo_HB	R/W	0x02
0x5E	TouchDetection_Upper_TH_3	R/W	0x00	0x9E	AE_Ch1_Innertarget_Hi_LB	R/W	0x00
0x5F	TouchDetection_Upper_TH_4	R/W	0x00	0x9F	AE_Ch1_Innertarget_Hi_HB	R/W	0x05
0x60	TouchDetection_Lower_TH_1	R/W	0x80	0xA0	AE_Ch1_Innertarget_Lo_LB	R/W	0x00
0x61	TouchDetection_Lower_TH_2	R/W	0x00	0xA1	AE_Ch1_Innertarget_Lo_HB	R/W	0x03
0x62	TouchDetection_Lower_TH_3	R/W	0x00	0xA7	AE_LED1_DAC_Min	R/W	0x01
0x63	TouchDetection_Lower_TH_4	R/W	0x00	0xB0	AE_LED1_DAC_EnH	R/W	0x01
0x64	TouchDetection_Count_TH	R/W	0x0A	0xB1	AE_Ch2_EnH	R/W	0x01
0x65	NoTouchDetection_Count_TH	R/W	0x0A	0xB2	AE_Ch2_Mid_LB	R/W	0xA0
0x6C	AE_Ch0_EnH	R/W	0x01	0xB3	AE_Ch2_Mid_HB	R/W	0x00
0x6D	AE_Ch0_Mid_LB	R/W	0xA0	0xB4	AE_Ch2_Max_LB	R/W	0xF0
0xB5	AE_Ch2_Max_HB	R/W	0x00	0xC1	AE_Ch2_Innertarget_Hi_HB	R/W	0x05
0xB6	AE_Ch2_Min_LB	R/W	0x52	0xC2	AE_Ch2_Innertarget_Lo_LB	R/W	0x00

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0xB7	AE_Ch2_Min_HB	R/W	0x00	0xC3	AE_Ch2_Innertarget_Lo_HB	R/W	0x03
0xBC	AE_Ch2_Outerbound_Hi_LB	R/W	0x00	0xC9	AE_LED2_DAC_Min	R/W	0x01
0xBD	AE_Ch2_Outerbound_Hi_HB	R/W	0x06	0xD2	AE_LED2_DAC_EnH	R/W	0x01
0xBE	AE_Ch2_Outerbound_Lo_LB	R/W	0x00	0xDE	PGAgain_Sel	R/W	0x01
0xBF	AE_Ch2_Outerbound_Lo_HB	R/W	0x02	0xE1	SW_Reset_N	R/W	0x01
0xC0	AE_Ch2_Innertarget_Hi_LB	R/W	0x00	0xE6	LED_DAC_Change_Flag_EnH	R/W	0x00

Table 9. Register Bank1

Note: Switch to Register Bank1 by writing 0x01 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x7A	BG_Sub_EnH	R/W	0x00	0xBB	LED1_DAC_Code	R/W	0x40
0x7C	Congain_Sel	R/W	0x00	0xBC	LED2_DAC_Code	R/W	0x40
0x80	PS_Ctrl_EnH	R/W	0x01	0xC0	LPT_EnH	R/W	0x01
0xB4	LED0_Man_EnH	R/W	0x00	0xC3	OSC_EnL	R/W	0x00
0xB5	LED1_Man_EnH	R/W	0x00	0xD5	TIMER_Gen_Enable	R/W	0x00
0xB6	LED2_Man_EnH	R/W	0x00	0xD6	TIMER_Gen_Period_LB	R/W	0x40
0xB7	LED0_DAC_EnL	R/W	0x00	0xD7	TIMER_Gen_Period_HB	R/W	0x01
0xB8	LED1_DAC_EnL	R/W	0x00	0xE6	IF_Wakeup_Interval_LB	R/W	0x05
0xB9	LED2_DAC_EnL	R/W	0x00	0xE7	IF_Wakeup_Interval_HB	R/W	0x00
0xBA	LED0_DAC_Code	R/W	0x40	0xEA	SetFIFO_RptNum	R/W	0x03

Table 10. Register Bank2

Note: Switch to Register Bank2 by writing 0x02 to Reg-0x7F

Address	Register Name	Access	Default	Address	Register Name	Access	Default
0x25	INT_Mode_Sel	R/W	0x00	0x83	Readout_FIFO_Checksum_4	RO	0x00
0x29	INT_Output_EnL	R/W	0x01	0x8C	INT_SramFIFO_Overflow_Clear	R/W	0x00
0x45	Touch_Flag	RO	0x00	0x8D	INT_SramFIFO_Overflow_Mask	R/W	0x00
0x73	INT_Reg_Array	RO	0x00	0x8E	INT_SramFIFO_Underflow_Clear	R/W	0x00
0x74	INT_SramFIFO_DR_Mask	R/W	0x00	0x8F	INT_SramFIFO_Underflow_Mask	R/W	0x00
0x75	INT_SramFIFO_DR_Clear	R/W	0x00	0xA0	CH0_Exposure_Time_LB	RO	0x00
0x76	INT_TouchDet_Mask	R/W	0x00	0xA1	CH0_Exposure_Time_HB	RO	0x00
0x77	INT_TouchDet_Clear	R/W	0x00	0xA2	CH1_Exposure_Time_LB	RO	0x00
0x78	All_INT_Mask	R/W	0x00	0xA3	CH1_Exposure_Time_HB	RO	0x00
0x7A	INT_Type	R/W	0x01	0xA4	CH2_Exposure_Time_LB	RO	0x00
0x7B	INT_Pulse_Width	R/W	0x08	0xA5	CH2_Exposure_Time_HB	RO	0x00
0x80	Readout_FIFO_Checksum_1	RO	0x00	0xA6	LED0_DAC_Value	RO	0x00
0x81	Readout_FIFO_Checksum_2	RO	0x00	0xA7	LED1_DAC_Value	RO	0x00
0x82	Readout_FIFO_Checksum_3	RO	0x00	0xA8	LED2_DAC_Value	RO	0x00

Document Revision History

Revision Number	Date	Description
1.0	14 Apr 2016	1st Creation
1.1	07 Apr 2017	Modify PC Cover current consumption for new design
1.2	23 Aug 2017	Update Pad Dimension on PCB/FPC
1.3	25 Sep 2017	Update Recommended PCB Layout