

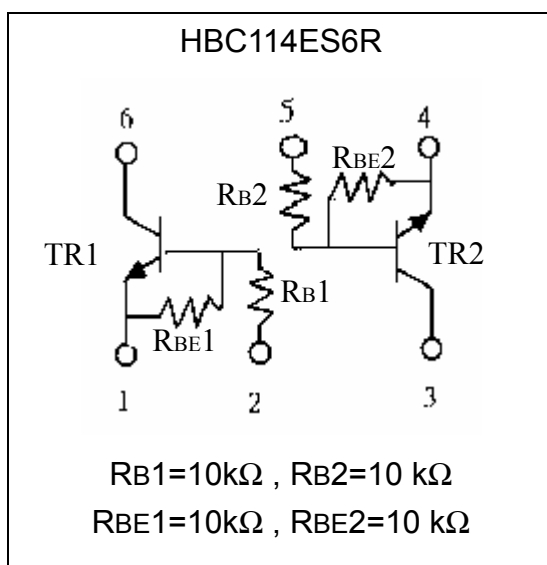
Dual NPN Digital Transistors

HBC114ES6R

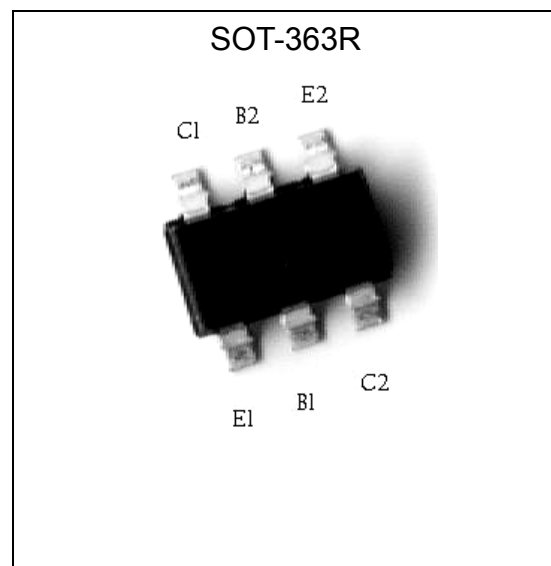
Features

- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- Only the on/off conditions need to be set for operation, making device design easy.
- Two DTC114E chips in a SOT-363 package.
- Mounting by SOT-323 automatic mounting machines is possible.
- Mounting cost and area can be cut in half.
- Transistor elements are independent, eliminating interference.
- Complements the HBA114ES6R.
- Pb-free package.

Equivalent Circuit



Outline



**Absolute Maximum Ratings** (Each Transistor, Ta=25°C)

Parameter	Symbol	Limits	Unit
Supply Voltage	V _{CC}	50	V
Input Voltage	V _{IN}	-10~+40	V
Output Current	I _O	50	mA
	I _{O(max.)}	100	mA
Power Dissipation	P _d	200 *1	mW
Junction Temperature	T _j	150	°C
Storage Temperature	T _{stg}	-55~+150	°C

Note:*1.150mW per element must not be exceeded.

Characteristics (Each Transistor, Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Voltage	V _{I(off)}	-	-	0.5	V	V _{CC} =5V, I _O =100μA
	V _{I(on)}	3	-	-	V	V _O =0.3V, I _O =10mA
Output Voltage	V _{O(on)}	-	0.1	0.3	V	I _O /I _I =10mA/0.5mA
Input Current	I _I	-	-	0.88	mA	V _I =5V
Output Current	I _{O(off)}	-	-	0.5	μA	V _{CC} =50V, V _I =0V
DC Current Gain	G _I	30	-	-	-	V _O =5V, I _O =5mA
Input Resistance	R _I	7	10	13	kΩ	-
Resistance Ratio	R ₂ /R ₁	0.8	1	1.2	-	-
Transition Frequency	f _T	-	250	-	MHz	V _{CE} =10V, I _C =5mA, f=100MHz*

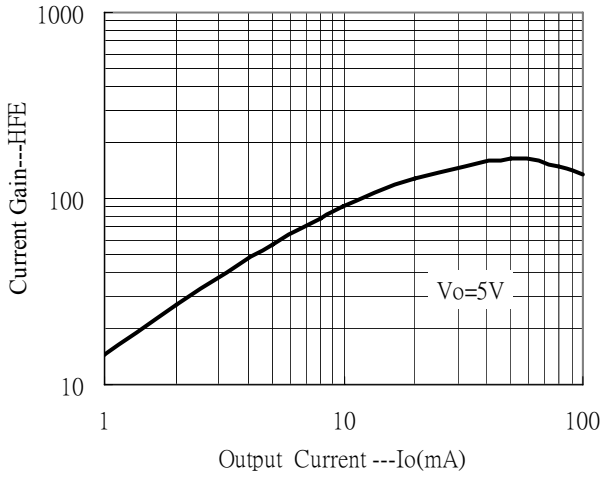
* Transition frequency of the device

Ordering Information

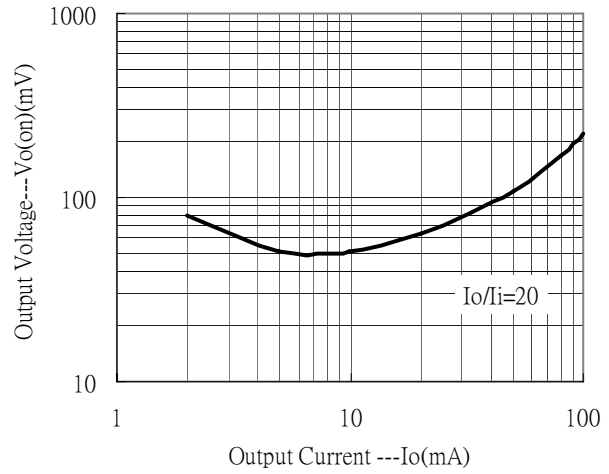
Device	Package	Shipping	Marking
HBC114ES6R	SOT-363 (Pb-free)	3000 pcs / Tape & Reel	7A

Characteristic Curves

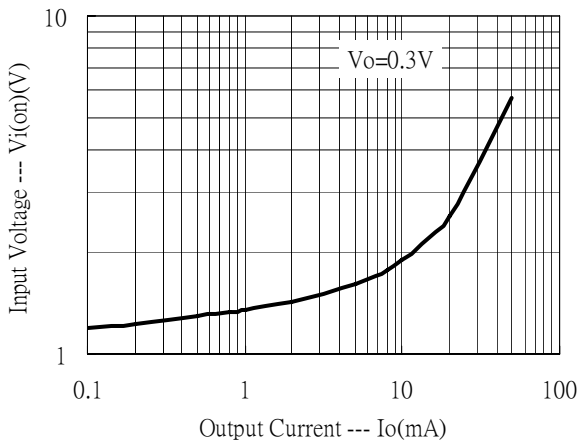
DC Current Gain vs Output Current



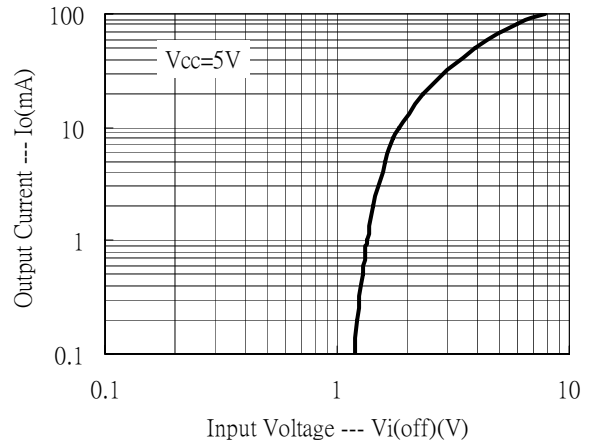
Output Voltage vs Output Current



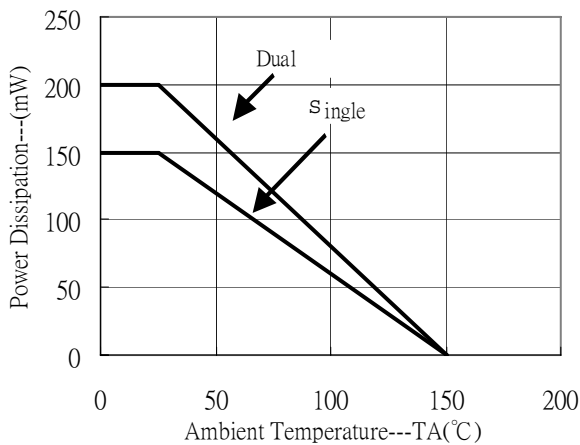
Input Voltage vs Output Current (ON Characteristics)



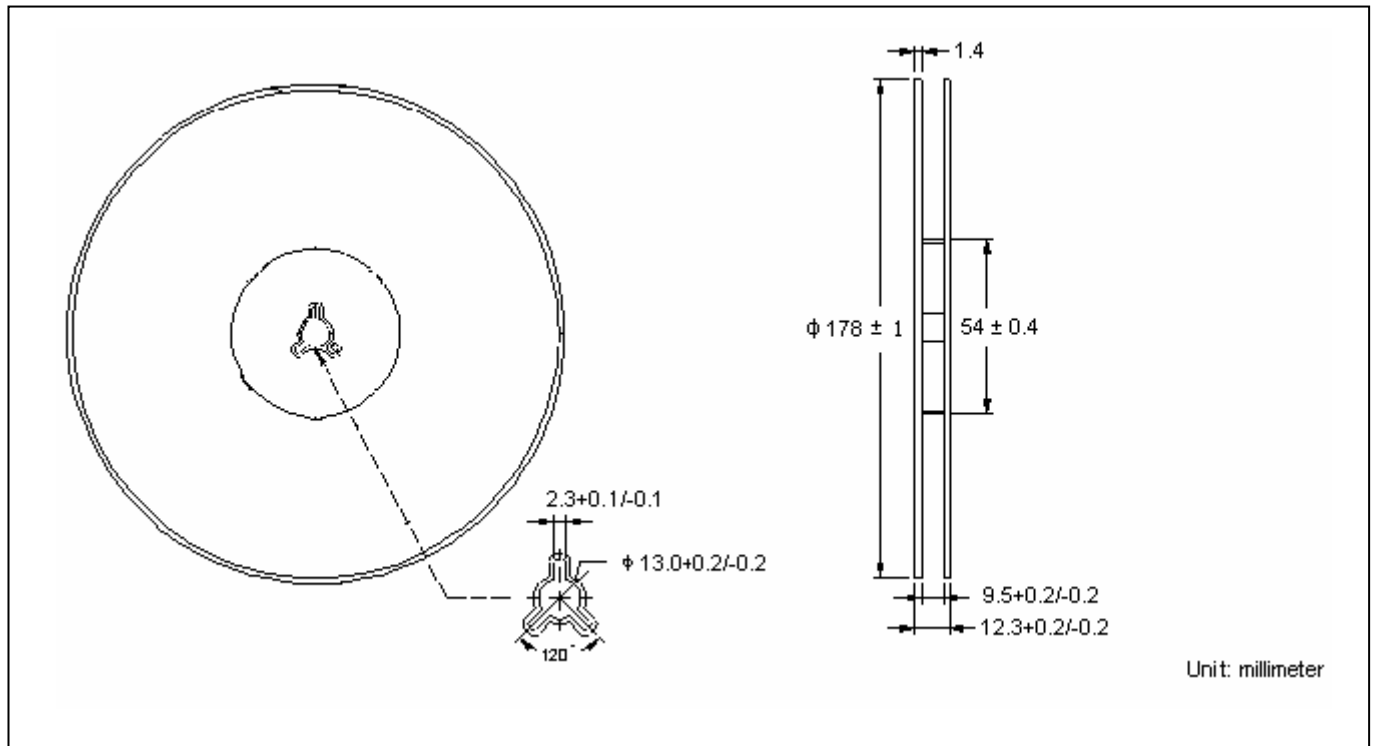
Output Current vs Input Voltage (OFF Characteristics)



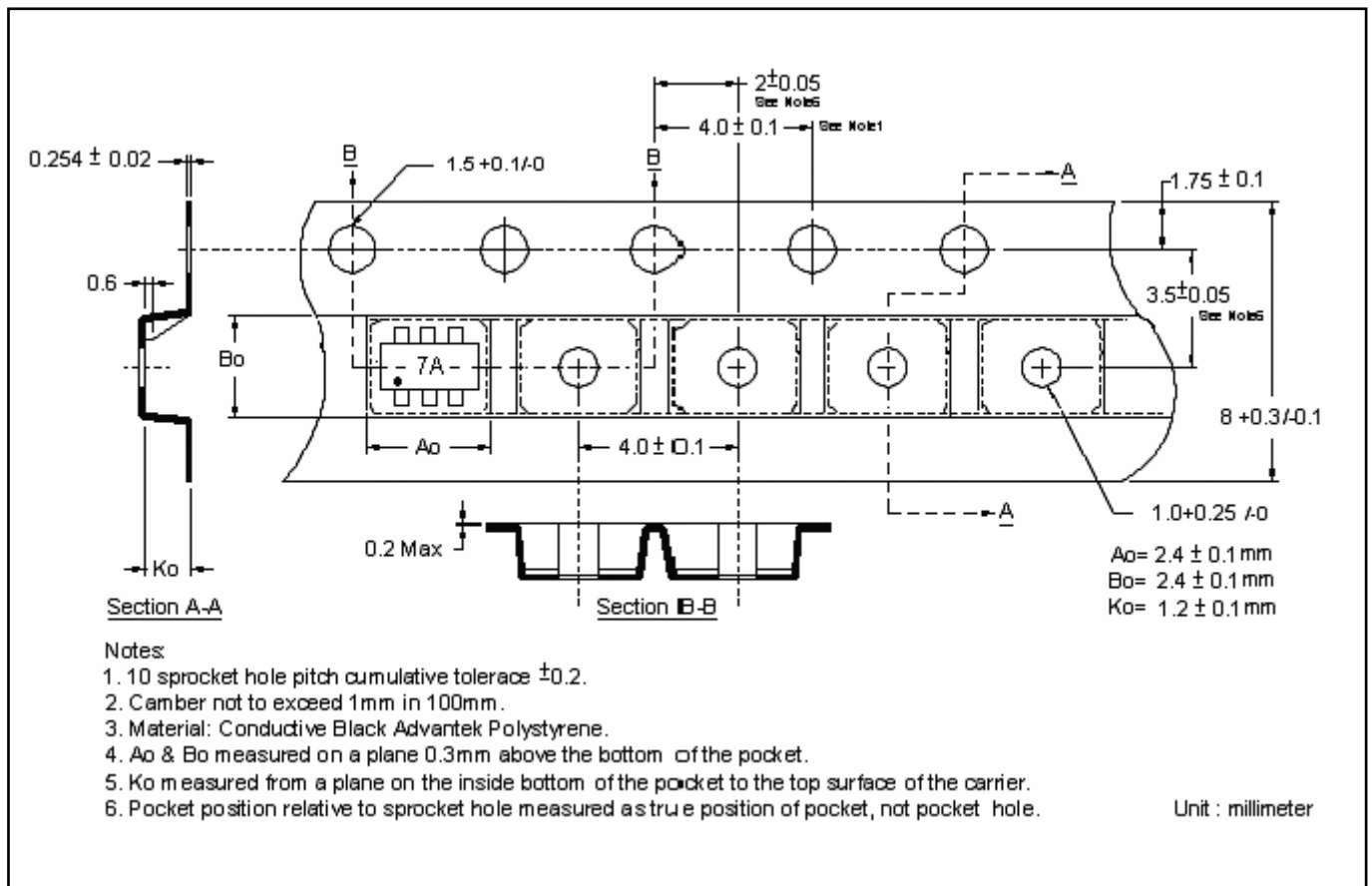
Power Derating Curves



Reel Dimension



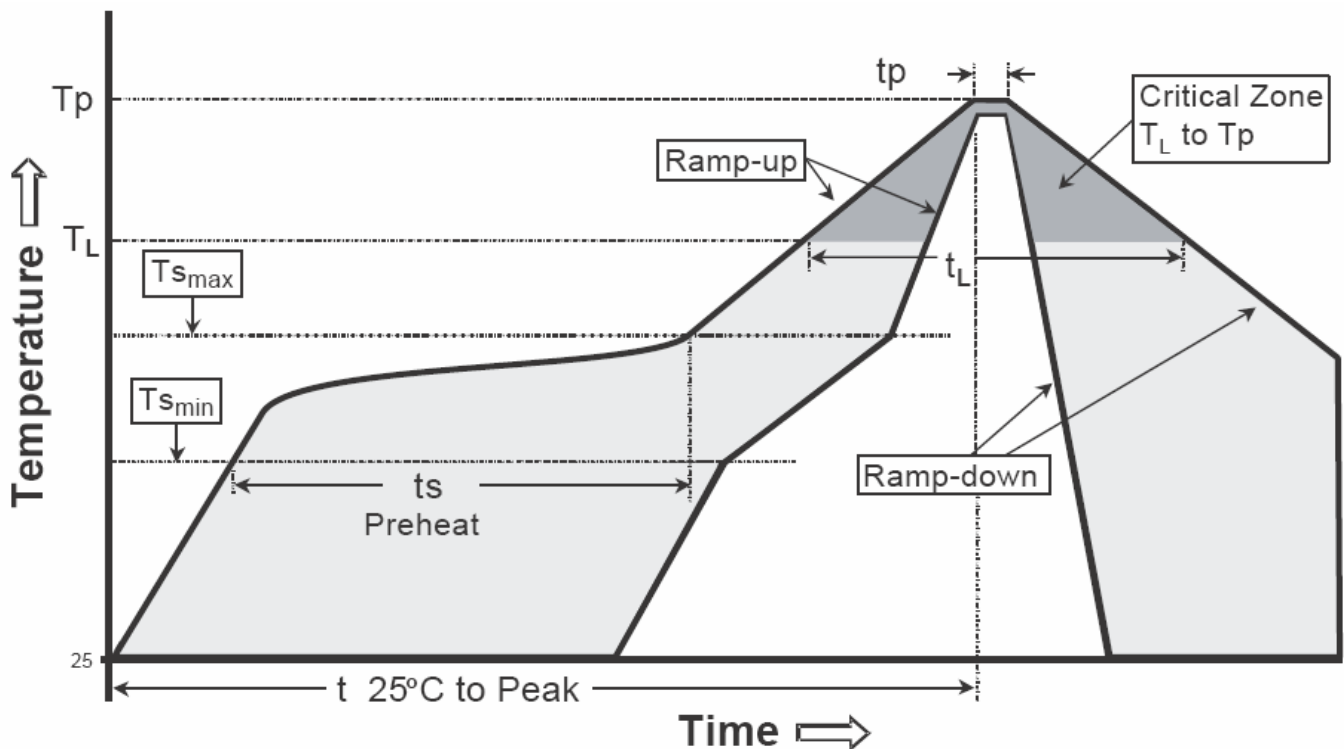
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

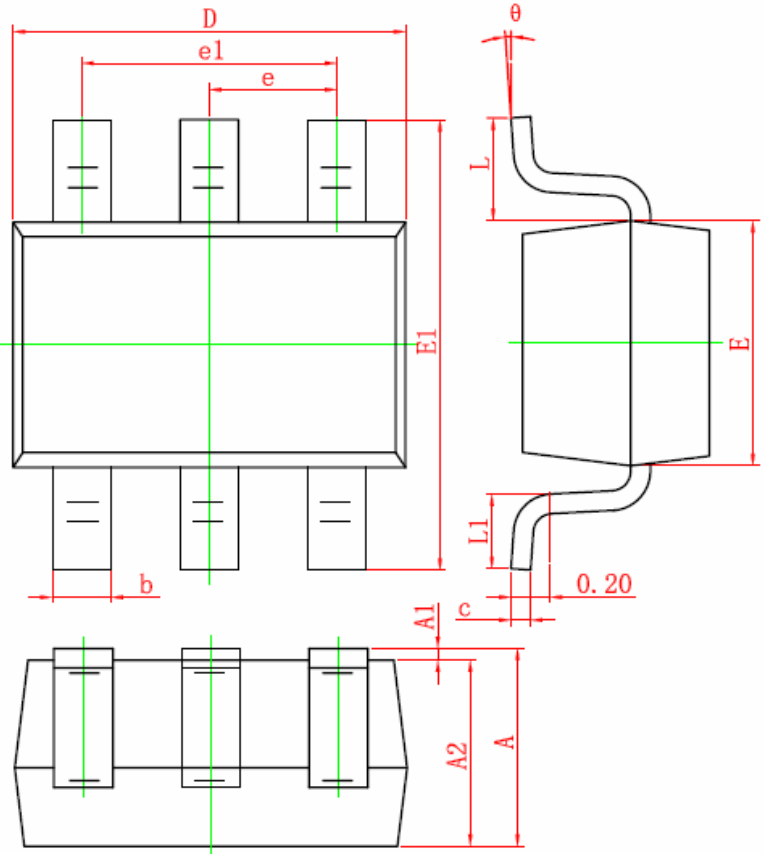
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _p)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(t _p)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

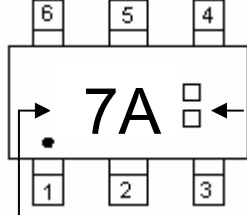
Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-363 Dimension



The diagram shows three views of the SOT-363R package: a top view, a side view, and a bottom view. Dimensions are labeled in red: D (total width), e1 (lead pitch), e (lead width), E1 (package height), E (package height), L (lead length), L1 (lead thickness), 0.20 (lead thickness), A1 (lead height), c (lead offset), A2 (package height), and A (package height). An angle θ is also indicated for the lead.

Marking:



Date Code:
 Year + Month
 Year : 6→2006,
 7→2007,..., etc
 Month : 1→Jan
 2→Feb, ..., 9→
 Sep, A→Oct, B
 →Nov, C→Dec

Device Code

6-Lead SOT-363R Plastic Surface Mounted Package
 CYStek Package Code: S6R

Style:
 Pin 1. Emitter1 (E1)
 Pin 2. Base1 (B1)
 Pin 3. Collector2 (C2)
 Pin 4. Emitter2 (E2)
 Pin 5. Base2 (B2)
 Pin 6. Collector1 (C1)

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.900	1.100	0.035	0.043	E1	2.150	2.450	0.085	0.096
A1	0.000	0.100	0.000	0.004	e	0.650	TYP	0.026	TYP
A2	0.900	1.000	0.035	0.039	e1	1.200	1.400	0.047	0.055
b	0.150	0.350	0.006	0.014	L	0.525	REF	0.021	REF
c	0.080	0.150	0.003	0.006	L1	0.260	0.460	0.010	0.018
D	2.000	2.200	0.079	0.087	θ	0°	8°	0°	8°
E	1.150	1.350	0.045	0.053					

Notes : 1.Controlling dimension : millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead : Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek **semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.**
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.