

2SJ587

Silicon P Channel MOS FET
High Speed Switching

HITACHI

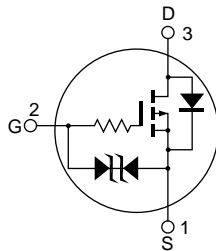
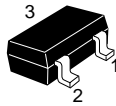
ADE-208-801 (Z)
1st.Edition.
June 1999

Features

- Low on-resistance
 $R_{DS} = 8.5 \Omega$ typ. ($V_{GS} = -4 \text{ V}$, $I_D = -25 \text{ mA}$)
 $R_{DS} = 15$ typ. ($V_{GS} = -2.5 \text{ V}$, $I_D = -10 \text{ mA}$)
- 2.5 V gate drive device.
- Small package (SMPAK)

Outline

SMPAK



1. Source
2. Gate
3. Drain

Absolute Maximum Ratings (Ta = 25°C)

| Item | Symbol | Ratings | Unit |
|--|---------------------------------|-------------|------|
| Drain to source voltage | V_{DSS} | -20 | V |
| Gate to source voltage | V_{GSS} | ±10 | V |
| Drain current | I_D | -50 | mA |
| Drain peak current | $I_{D(pulse)}$ ^{Note1} | -200 | mA |
| Body-drain diode reverse drain current | I_{DR} | -50 | mA |
| Channel dissipation | Pch ^{Note 2} | 100 | mW |
| Channel temperature | Tch | 150 | °C |
| Storage temperature | Tstg | -55 to +150 | °C |

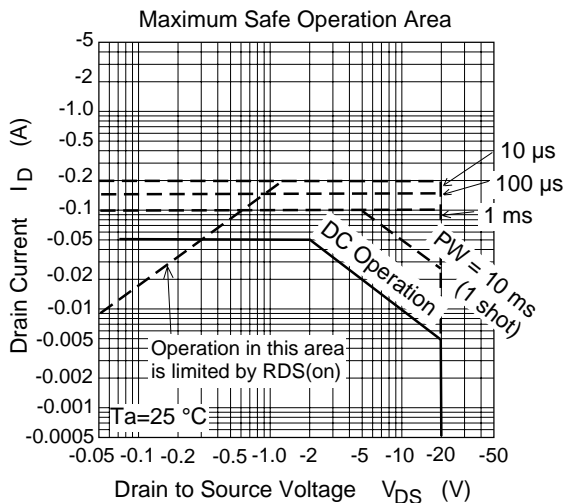
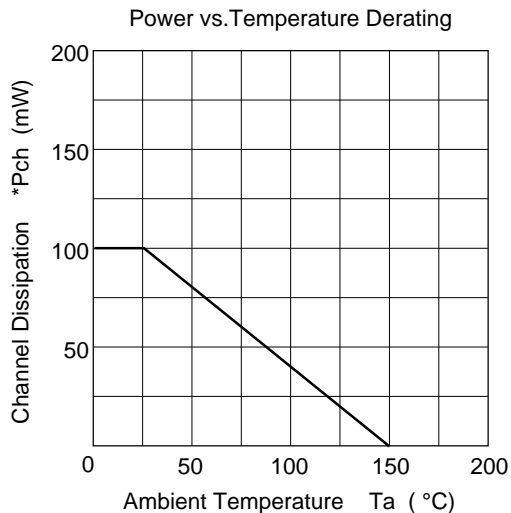
Note: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value on the alumina ceramic board (12.5x 20 x0.7 mm)

Electrical Characteristics (Ta = 25°C)

| Item | Symbol | Min | Typ | Max | Unit | Test Conditions |
|--|---------------|------|-----|------|------|---|
| Drain to source breakdown voltage | $V_{(BR)DSS}$ | -20 | — | — | V | $I_D = -100 \mu A, V_{GS} = 0$ |
| Gate to source breakdown voltage | $V_{(BR)GSS}$ | ±10 | — | — | V | $I_G = \pm 100 \mu A, V_{DS} = 0$ |
| Gate to source leak current | I_{GSS} | — | — | ±5 | μA | $V_{GS} = \pm 8 V, V_{DS} = 0$ |
| Zero gate voltage drain current | I_{DSS} | — | — | -1 | μA | $V_{DS} = -20 V, V_{GS} = 0$ |
| Gate to source cutoff voltage | $V_{GS(off)}$ | -0.8 | — | -1.8 | V | $I_D = -10 \mu A, V_{DS} = -5 V$ |
| Static drain to source on state resistance | $R_{DS(on)}$ | — | 4.1 | 5.0 | Ω | $I_D = -25 mA, V_{GS} = -4 V$ ^{Note 3} |
| | $R_{DS(on)}$ | — | 6.0 | 8.5 | Ω | $I_D = -10 mA, V_{GS} = -2.5 V$ ^{Note 3} |
| Forward transfer admittance | $ y_{fs} $ | 32.5 | 50 | — | mS | $I_D = -25 mA, V_{DS} = -10 V$ ^{Note 3} |
| Input capacitance | Ciss | — | 13 | — | pF | $V_{DS} = -10 V$ |
| Output capacitance | Coss | — | 10 | — | pF | $V_{GS} = 0$ |
| Reverse transfer capacitance | Crss | — | 1.8 | — | pF | f = 1 MHz |
| Turn-on delay time | $t_{d(on)}$ | — | 22 | — | ns | $I_D = -25 mA, V_{GS} = -4 V$ |
| Rise time | t_r | — | 48 | — | ns | $R_L = 400 \Omega$ |
| Turn-off delay time | $t_{d(off)}$ | — | 50 | — | ns | |
| Fall time | t_f | — | 60 | — | ns | |

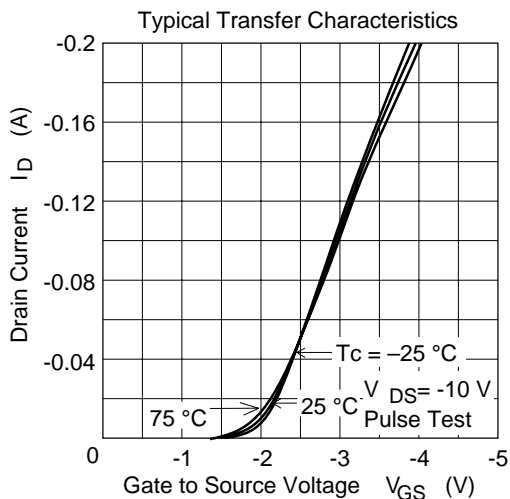
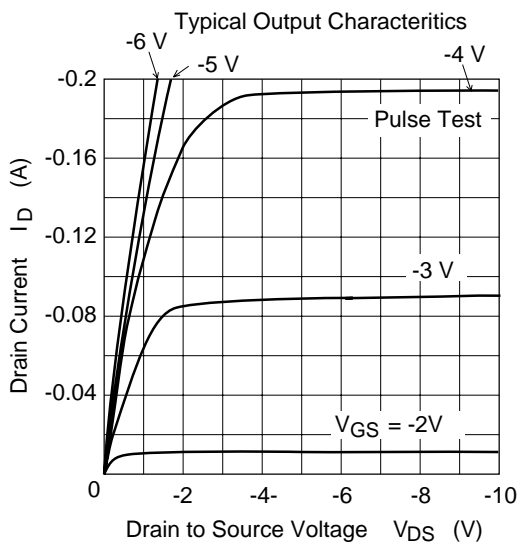
Note: 3. Pulse test
 4. Marking is DP

Main Characteristics

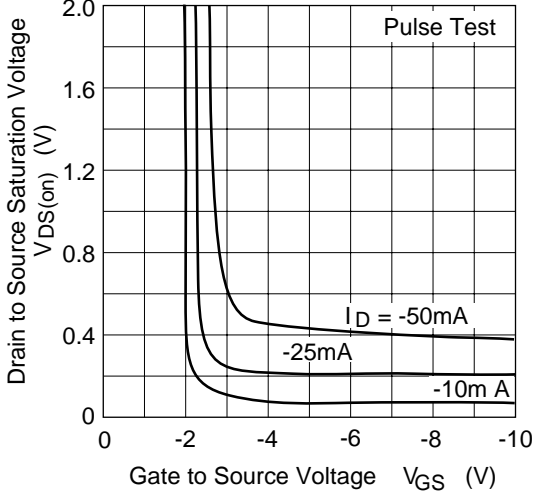


*Value on the alumina ceramic board.(12.5x20x0.7mm)

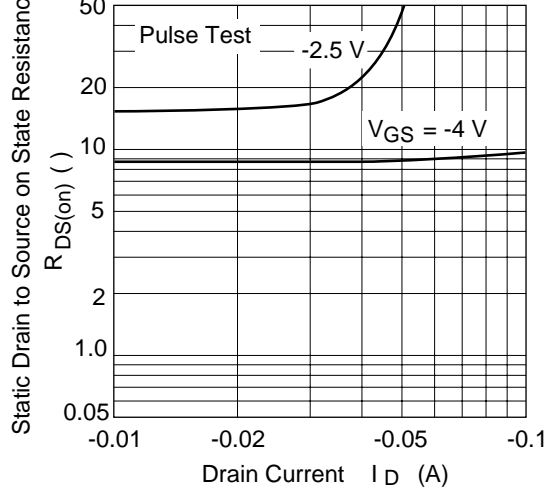
Value on the alumina ceramic board.(12.5x20x0.7mm)



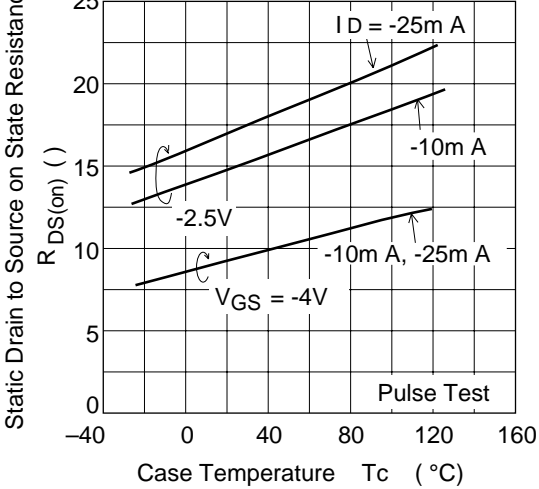
Drain to Source Saturation Voltage vs. Gate to Source Voltage



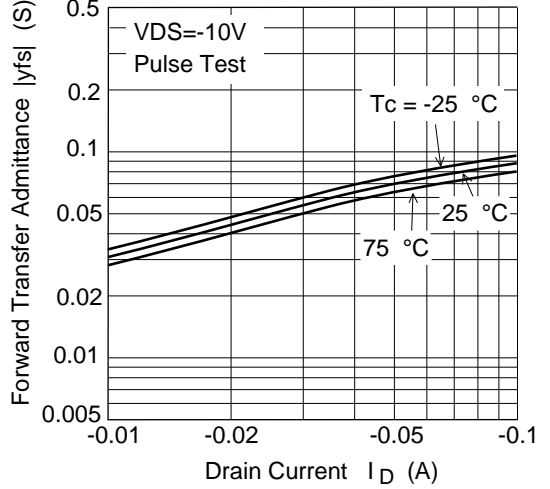
Static Drain to Source on State Resistance vs. Drain Current

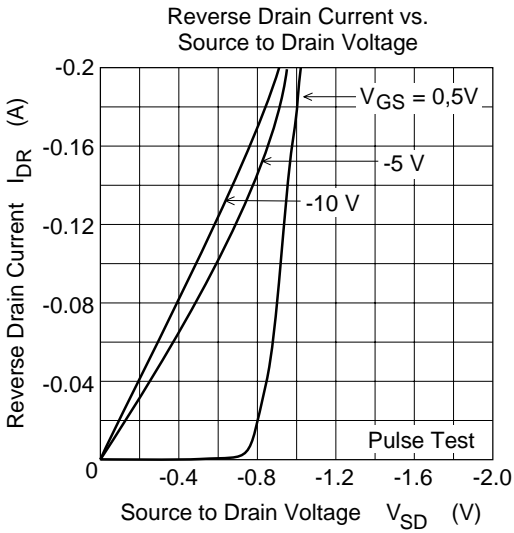
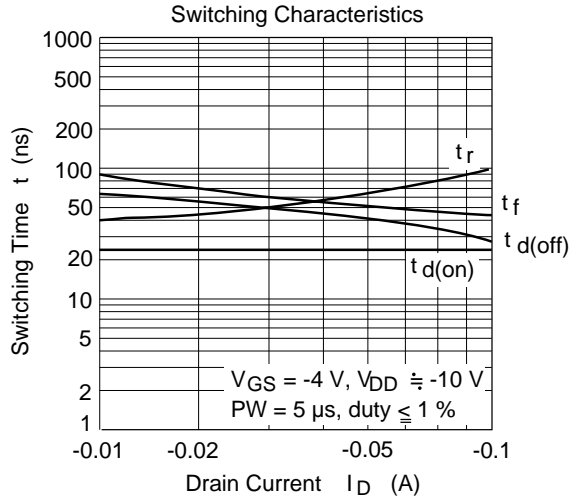
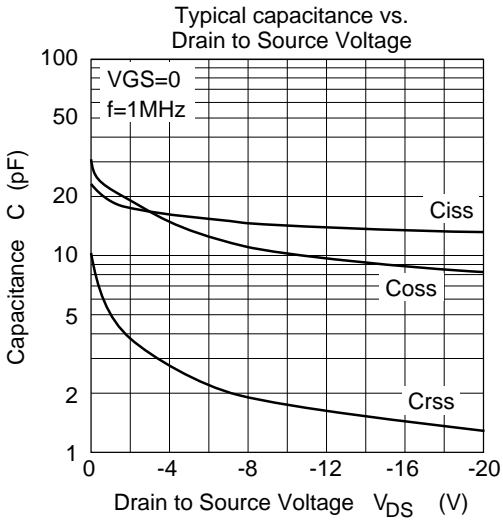


Static Drain to Source on State Resistance vs. Temperature

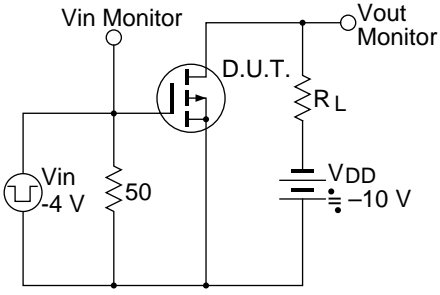


Forward Transfer Admittance vs. Drain Current

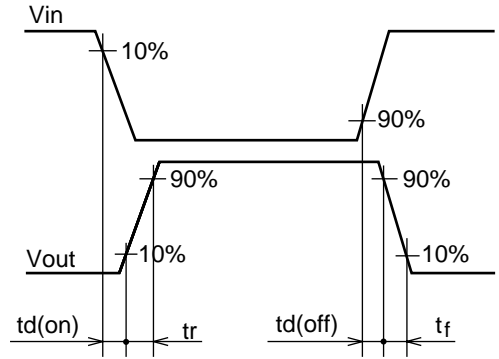




Switching Time Test Circuit

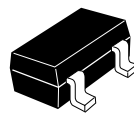
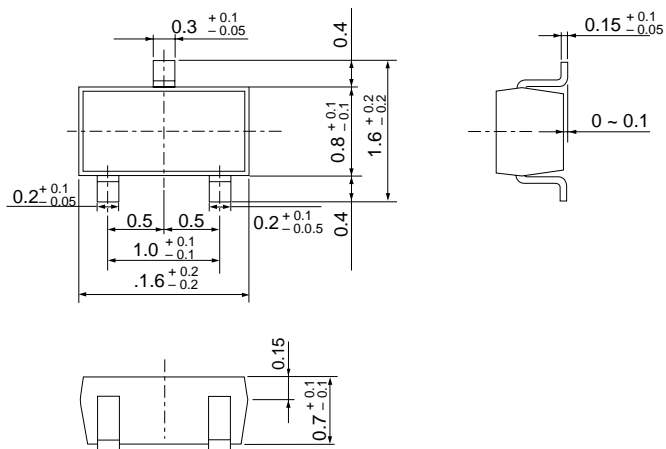


Waveforms



Package Dimensions

Unit: mm



| Hitachi Code | SMPAK |
|--------------|-------|
| EIAJ | - |
| JEDEC | - |

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