



N-CHANNEL MOSFET

Qualified per MIL-PRF-19500/556

Qualified Levels:
JAN, JANTX, and
JANTXV

DESCRIPTION

This family of 2N6782, 2N6784 and 2N6786 switching transistors are military qualified up to the JANTXV level for high-reliability applications. These devices are also available in a low profile U-18 LCC surface mount package. Microsemi also offers numerous other transistor products to meet higher and lower power ratings with various switching speed requirements in both through-hole and surface-mount packages.

Important: For the latest information, visit our website <http://www.microsemi.com>.

FEATURES

- JEDEC registered 2N6782, 2N6784 and 2N6786 number series.
- JAN, JANTX, and JANTXV qualifications are available per MIL-PRF-19500/556. (See [part nomenclature](#) for all available options.)
- RoHS compliant versions available (commercial grade only).

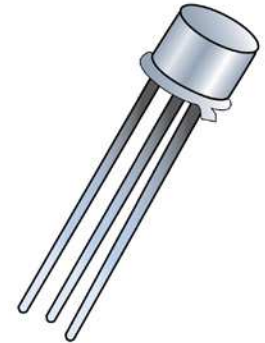
APPLICATIONS / BENEFITS

- Lightweight top-hat design with flexible terminals offers a variety of mounting flexibility.
- Military and other high-reliability applications.

MAXIMUM RATINGS @ T_A = +25 °C unless otherwise stated

Parameters / Test Conditions	Symbol	Value	Unit
Operating & Storage Junction Temperature Range	T _J & T _{stg}	-55 to +150	°C
Thermal Resistance Junction-to-Case	R _{θJC}	8.33	°C/W
Total Power Dissipation	P _T	@ T _A = +25 °C	0.8
		@ T _C = +25 °C ⁽¹⁾	15
Drain-Source Voltage, dc	V _{DS}	2N6782	100
		2N6784	200
		2N6786	400
Gate-Source Voltage, dc	V _{GS}	± 20	V
Drain Current, dc @ T _C = +25 °C ⁽²⁾	I _{D1}	2N6782	3.50
		2N6784	2.25
		2N6786	1.25
Drain Current, dc @ T _C = +100 °C ⁽²⁾	I _{D2}	2N6782	2.25
		2N6784	1.50
		2N6786	0.80
Off-State Current (Peak Total Value) ⁽³⁾	I _{DM}	2N6782	14.0
		2N6784	9.0
		2N6786	5.5
Source Current	I _S	2N6782	3.50
		2N6784	2.25
		2N6786	1.25

See notes on next page.



**TO-205AF (TO-39)
Package**

Also available in:

U-18 LCC package
(surface mount)
 **2N6782U & 2N6786U**

MSC – Lawrence

6 Lake Street,
Lawrence, MA 01841
Tel: 1-800-446-1158 or
(978) 620-2600
Fax: (978) 689-0803

MSC – Ireland

Gort Road Business Park,
Ennis, Co. Clare, Ireland
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Website:

www.microsemi.com

- Notes:**
- Derate linearly 0.12 W/°C for $T_C > +25\text{ }^\circ\text{C}$.
 - The following formula derives the maximum theoretical I_D limit. I_D is also limited by package and internal wires and may be limited due to pin diameter.

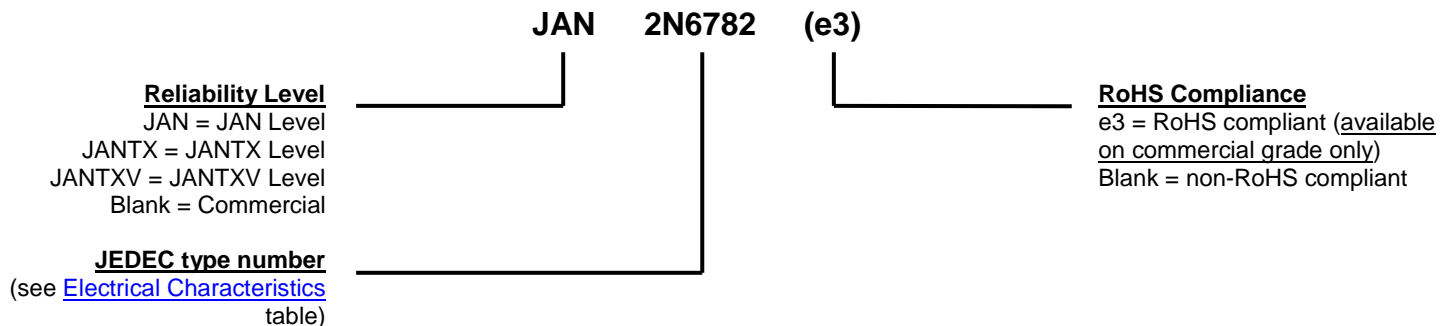
$$I_D = \sqrt{\frac{T_J(\text{max}) - T_C}{R_{\theta JC} \times R_{DS(on)} @ T_J(\text{max})}}$$

- $I_{DM} = 4 \times I_{D1}$ as calculated in note 1.

MECHANICAL and PACKAGING

- CASE: Hermetically sealed, kovar base, nickel cap.
- TERMINALS: Tin/lead solder dip nickel plate or RoHS compliant pure tin plate (commercial grade only).
- MARKING: Part number, date code, manufacturer's ID.
- WEIGHT: Approximately 1.064 grams.
- See [Package Dimensions](#) on last page.

PART NOMENCLATURE



SYMBOLS & DEFINITIONS

Symbol	Definition
di/dt	Rate of change of diode current while in reverse-recovery mode, recorded as maximum value.
I_F	Forward current
R_G	Gate drive impedance
V_{DD}	Drain supply voltage
V_{DS}	Drain source voltage, dc
V_{GS}	Gate source voltage, dc

ELECTRICAL CHARACTERISTICS @ $T_A = +25\text{ }^\circ\text{C}$, unless otherwise noted

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
OFF CHARACTERISTICS				
Drain-Source Breakdown Voltage $V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$	2N6782 2N6784 2N6786 $V_{(BR)DSS}$	100 200 400		V
Gate-Source Voltage (Threshold) $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_J = +125\text{ }^\circ\text{C}$ $V_{DS} \geq V_{GS}, I_D = 0.25\text{ mA}, T_J = -55\text{ }^\circ\text{C}$	$V_{GS(th)1}$ $V_{GS(th)2}$ $V_{GS(th)3}$	2.0 1.0	4.0 5.0	V
Gate Current $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}, T_J = +125\text{ }^\circ\text{C}$	I_{GSS1} I_{GSS2}		± 100 ± 200	nA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}$ $V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}$	2N6782 2N6784 2N6786 I_{DSS1}		25	μA
Drain Current $V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}, T_J = +125\text{ }^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 160\text{ V}, T_J = +125\text{ }^\circ\text{C}$ $V_{GS} = 0\text{ V}, V_{DS} = 320\text{ V}, T_J = +125\text{ }^\circ\text{C}$	2N6782 2N6784 2N6786 I_{DSS2}		0.25	mA
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 1.50\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 0.80\text{ A pulsed}$	2N6782 2N6784 2N6786 $r_{DS(on)1}$		0.60 1.50 3.60	Ω
Static Drain-Source On-State Resistance $V_{GS} = 10\text{ V}, I_D = 3.50\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 1.25\text{ A pulsed}$	2N6782 2N6784 2N6786 $r_{DS(on)2}$		0.61 1.60 3.70	Ω
Static Drain-Source On-State Resistance $T_J = +125\text{ }^\circ\text{C}$ $V_{GS} = 10\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 1.50\text{ A pulsed}$ $V_{GS} = 10\text{ V}, I_D = 0.80\text{ A pulsed}$	2N6782 2N6784 2N6786 $r_{DS(on)3}$		1.08 2.81 7.92	Ω
Diode Forward Voltage $V_{GS} = 0\text{ V}, I_D = 3.50\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 2.25\text{ A pulsed}$ $V_{GS} = 0\text{ V}, I_D = 1.25\text{ A pulsed}$	2N6782 2N6784 2N6786 V_{SD}		1.5 1.5 1.4	V

ELECTRICAL CHARACTERISTICS @ $T_A = +25\text{ }^\circ\text{C}$, unless otherwise noted (continued)
DYNAMIC CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Gate Charge:				
On-State Gate Charge				
$V_{GS} = 10\text{ V}$, $I_D = 3.50\text{ A}$, $V_{DS} = 50\text{ V}$ 2N6782	$Q_{g(on)}$		8.1	nC
$V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$, $V_{DS} = 100\text{ V}$ 2N6784		8.6		
$V_{GS} = 10\text{ V}$, $I_D = 1.25\text{ A}$, $V_{DS} = 200\text{ V}$ 2N6786		12		
Gate to Source Charge				
$V_{GS} = 10\text{ V}$, $I_D = 3.50\text{ A}$, $V_{DS} = 50\text{ V}$ 2N6782	Q_{gs}		1.7	nC
$V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$, $V_{DS} = 100\text{ V}$ 2N6784		1.5		
$V_{GS} = 10\text{ V}$, $I_D = 1.25\text{ A}$, $V_{DS} = 200\text{ V}$ 2N6786		1.8		
Gate to Drain Charge				
$V_{GS} = 10\text{ V}$, $I_D = 3.50\text{ A}$, $V_{DS} = 50\text{ V}$ 2N6782	Q_{gd}		4.5	nC
$V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$, $V_{DS} = 100\text{ V}$ 2N6784		5.5		
$V_{GS} = 10\text{ V}$, $I_D = 1.25\text{ A}$, $V_{DS} = 200\text{ V}$ 2N6786		7.6		

SWITCHING CHARACTERISTICS

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Turn-on delay time				
$I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 50\text{ V}$ 2N6782	$t_{d(on)}$		15	ns
$I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 100\text{ V}$ 2N6784				
$I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 200\text{ V}$ 2N6786				
Rinse time				
$I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 50\text{ V}$ 2N6782	t_r		25	ns
$I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 100\text{ V}$ 2N6784		20		
$I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 200\text{ V}$ 2N6786		20		
Turn-off delay time				
$I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 50\text{ V}$ 2N6782	$t_{d(off)}$		25	ns
$I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 100\text{ V}$ 2N6784		30		
$I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 200\text{ V}$ 2N6786		35		
Fall time				
$I_D = 3.50\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 50\text{ V}$ 2N6782	t_f		20	ns
$I_D = 2.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 100\text{ V}$ 2N6784		20		
$I_D = 1.25\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 7.5\text{ }\Omega$, $V_{DD} = 200\text{ V}$ 2N6786		30		
Diode Reverse Recovery Time				
$di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 50\text{ V}$, $I_F = 3.50\text{ A}$ 2N6782	t_{rr}		180	ns
$di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 50\text{ V}$, $I_F = 2.25\text{ A}$ 2N6784		350		
$di/dt \leq 100\text{ A}/\mu\text{s}$, $V_{DD} \leq 50\text{ V}$, $I_F = 1.25\text{ A}$ 2N6786		540		

GRAPHS

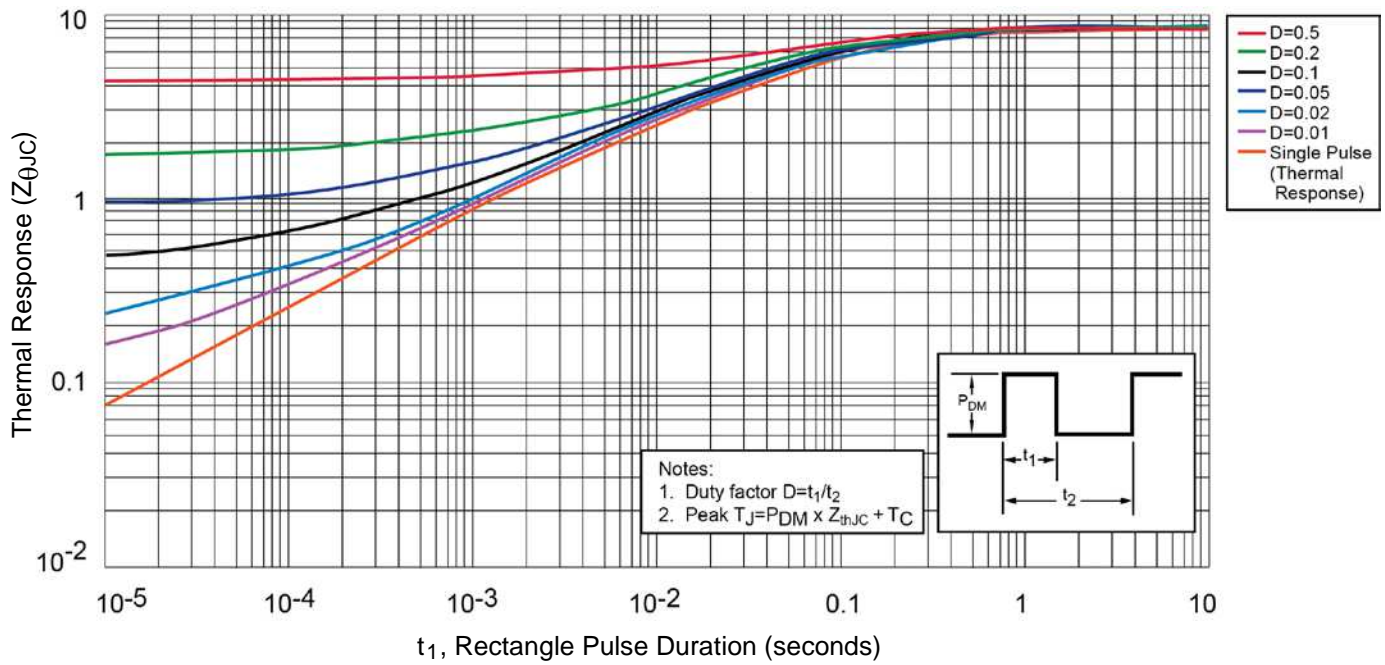
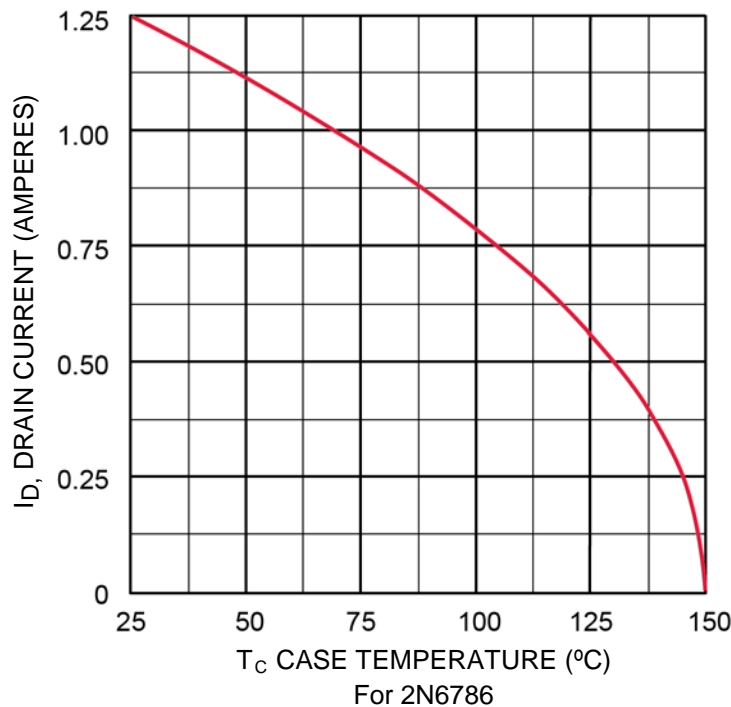
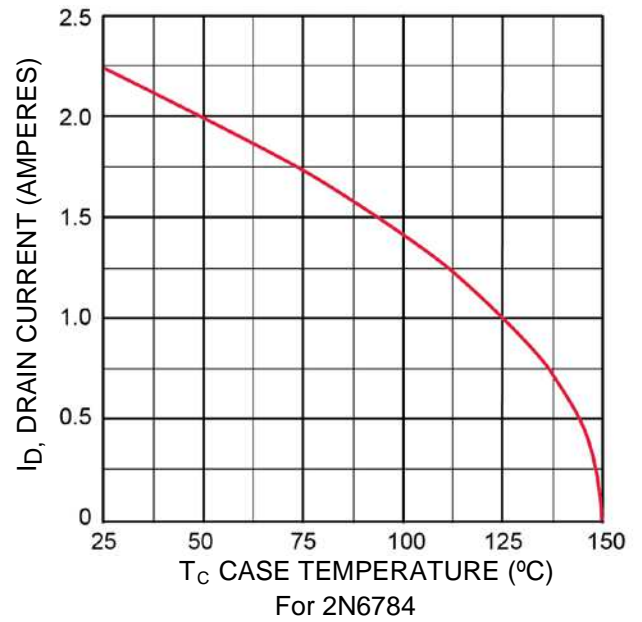
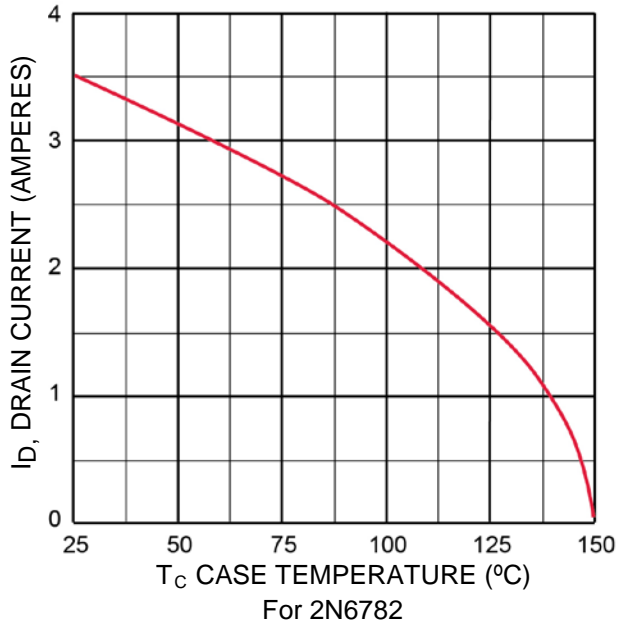
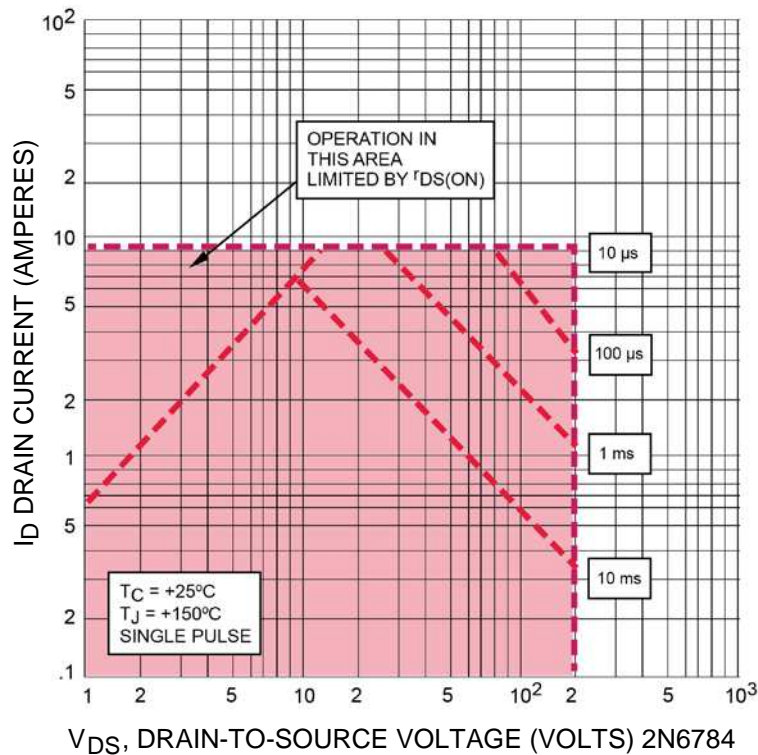
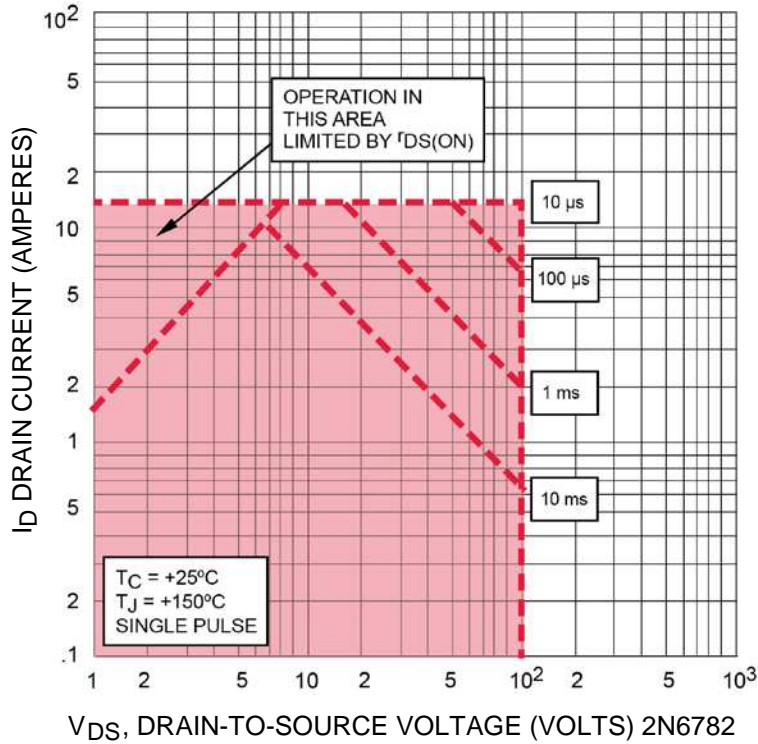


FIGURE 1
Thermal Response Curves

GRAPHS (continued)
FIGURE 2 – Maximum Drain Current vs Case Temperature Graphs


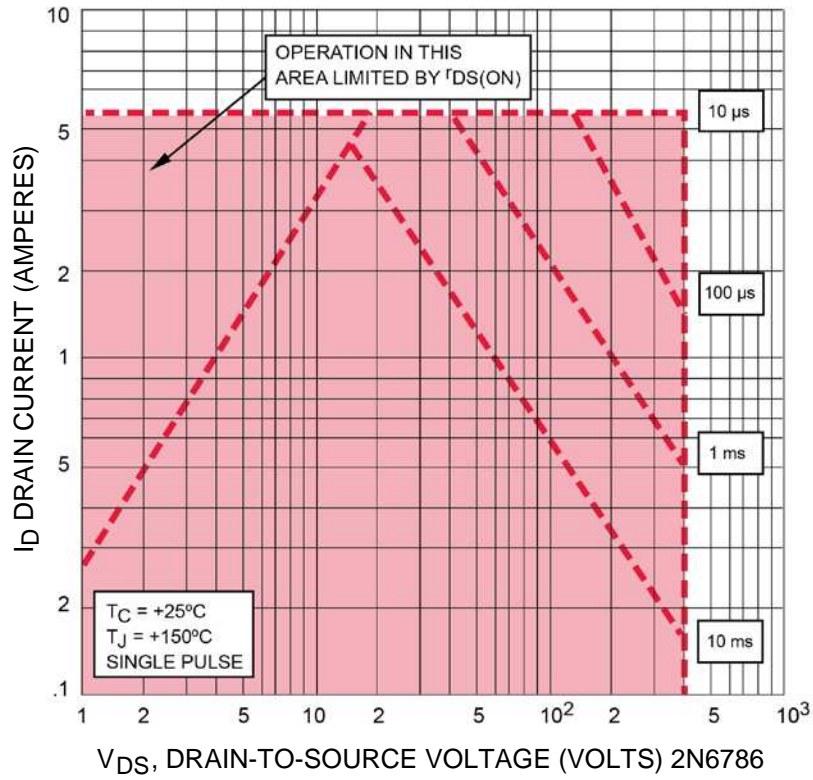
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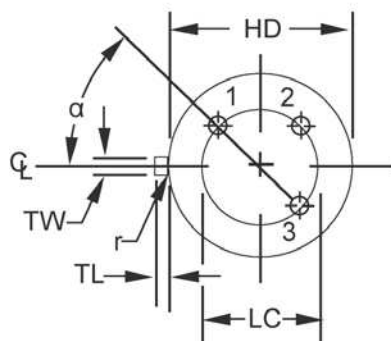
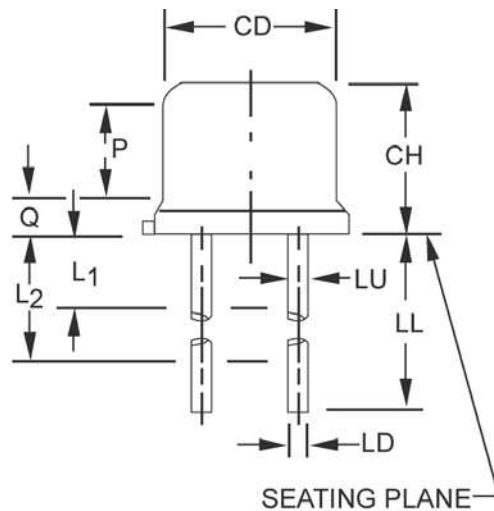
FIGURE 3 – Maximum Safe Operating Area



GRAPHS (continued)

FIGURE 3 – Maximum Safe Operating Area



PACKAGE DIMENSIONS


Symbol	Dimensions				Note
	Inch		Millimeters		
	Min	Max	Min	Max	
CD	0.305	0.335	7.75	8.51	
CH	0.160	0.180	4.06	4.57	
HD	0.335	0.370	8.51	9.40	
LC	0.200 TP		5.08 TP		6
LD	0.016	0.021	0.41	0.53	7, 8
LL	0.500	0.750	12.70	19.05	7, 8
LU	0.016	0.019	0.41	0.48	7, 8
L1		0.050		1.27	7, 8
L2	0.250		6.35		7, 8
P	.100		2.54		5
Q		0.050		1.27	4
TL	0.029	0.045	0.74	1.14	3
TW	0.028	0.034	0.72	0.86	2
r		0.010		0.25	9
α	45° TP		45° TP		6

NOTES:

- Dimensions are in inches. Millimeters are given for general information only.
- Beyond radius (r) maximum, J shall be held for a minimum length of .011 (0.028 mm).
- Dimension TL measured from maximum HD.
- Outline in this zone is not controlled.
- Dimension CD shall not vary more than .010 (0.25 mm) in zone P. This zone is controlled for automatic handling.
- Leads at gauge plane .054 +.001, -.000 (1.37 +0.03, -0.00 mm) below seating plane shall be within .007 (0.18 mm) radius of true position (TP) at maximum material condition (MMC) relative to tab at MMC.
- LU applies between L1 and L2. LD applies between L2 and L minimum. Diameter is uncontrolled in L1 and beyond LL minimum.
- All three leads.
- Radius (r) applies to both inside corners of tab.
- Drain is electrically connected to the case.
- In accordance with ASME Y14.5M, diameters are equivalent to Φ x symbology.