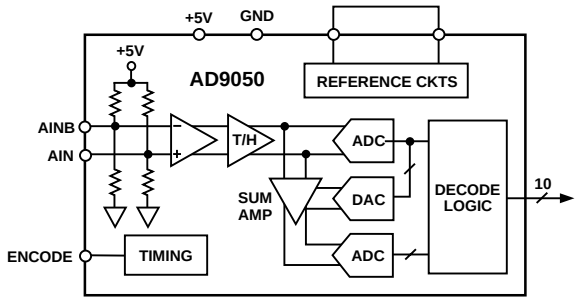
10-Bit, 40 MSPS/60 MSPS A/D Converter

AD9050

FEATURES
Low Power: 315 mW @ 40 MSPS, 345 mW @ 60 MSPS
On-Chip T/H, Reference
Single +5 V Power Supply Operation
Selectable 5 V or 3 V Logic I/O
SNR: 53 dB Minimum at 10 MHz w/40 MSPS

APPLICATIONS
Medical Imaging
Instrumentation
Digital Communications
Professional Video

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD9050 is a complete 10-bit monolithic sampling analog-to-digital converter (ADC) with an onboard track-and-hold and reference. The unit is designed for low cost, high performance applications and requires only +5 V and an encode clock to achieve 40 MSPS or 60 MSPS sample rates with 10-bit resolution.

The encode clock is TTL compatible and the digital outputs are CMOS; both can operate with 5 V/3 V logic, selected by the user. The two-step architecture used in the AD9050 is optimized to provide the best dynamic performance available while maintaining low power consumption.

A 2.5 V reference is included onboard, or the user can provide an external reference voltage for gain control or matching of multiple devices. Fabricated on an advanced BiCMOS process, the AD9050 is packaged in space saving surface mount packages (SOIC, SSOP) and is specified over the industrial (–40°C to +85°C) temperature range. The 60 MSPS version (AD9050BRS-60) is only available in the SSOP package.

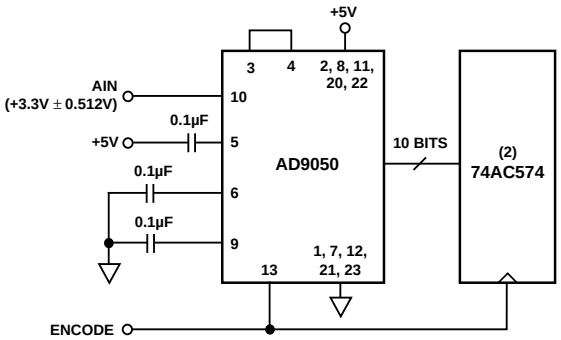


Figure 1. Typical Connections

REV. B

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AD9050–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_D, V_{DD} = +5 V; internal reference; ENCODE = 40 MSPS for BR/BRS, 60 MSPS for BRS-60 unless otherwise noted)

Parameter	Temp	Test Level	AD9050BR/BRS Min	AD9050BR/BRS Typ	AD9050BR/BRS Max	AD9050BRS-60 Min	AD9050BRS-60 Typ	AD9050BRS-60 Max	Units
RESOLUTION				10			10		Bits
DC ACCURACY									
Differential Nonlinearity	+25°C	I		0.75	1.75		0.85	1.85	LSB
	Full	V		1.0			1.1		LSB
Integral Nonlinearity	+25°C	I		1.0	1.75		1.25	2.0	LSB
	Full	V		1.25			1.50		LSB
No Missing Codes	Full	IV		GUARANTEED			GUARANTEED		
Gain Error	+25°C	I		±1.0	7.5		±1.0	8.5	% FS
Gain Tempco[1]	Full	V		±100			±100		ppm/°C
ANALOG INPUT									
Input Voltage Range	+25°C	V		1.024			1.024		V p-p
Input Offset Voltage	+25°C	I	–10	+7	+25	–10	+7	+25	mV
	Full	IV	–32		+51	–32		+51	mV
Input Resistance	+25°C	I	3.5	5.0	6.5	3.5	5.0	6.5	kΩ
Input Capacitance	+25°C	V		5			5		pF
Analog Bandwidth	+25°C	V		100			100		MHz
BANDGAP REFERENCE									
Output Voltage	+25°C	I	2.4	2.5	2.6	2.4	2.5	2.6	V
Temperature Coefficient[1]	Full	V		±50			±50		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	+25°C	I	40			60			MSPS
Minimum Conversion Rate	+25°C	IV		1.5	3		1.5	3	MSPS
Aperture Delay (t_A)	+25°C	V		2.7			2.7		ns
Aperture Uncertainty (Jitter)	+25°C	V		5			5		ps, rms
Output Propagation Delay (t_{PD})[2]	Full	IV	5		15	5		15	ns
DYNAMIC PERFORMANCE									
Transient Response	+25°C	V		10			10		ns
Overvoltage Recovery Time	+25°C	V		10			10		ns
ENOBS									
f_{IN} = 2.3 MHz	+25°C	V		8.93			8.93		ENOBs
f_{IN} = 10.3 MHz	+25°C	I	8.51	8.85		8.15	8.51		ENOBs
Signal-to-Noise Ratio (SINAD)[3]									
f_{IN} = 2.3 MHz	+25°C	V		55.5			55.5		dB
f_{IN} = 10.3 MHz	+25°C	I	53	55		51	53		dB
Signal-to-Noise Ratio (Without Harmonics)									
f_{IN} = 2.3 MHz	+25°C	V		56			56		dB
f_{IN} = 10.3 MHz	+25°C	I	53.5	55.5		51.5	54.0		dB
2nd Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	V		–69			–69		dBc
f_{IN} = 10.3 MHz	+25°C	I		–67	–60		–64	–58.5	dBc
3rd Harmonic Distortion									
f_{IN} = 2.3 MHz	+25°C	V		–75			–75		dBc
f_{IN} = 10.3 MHz	+25°C	I		–70	–58		–62	–57.5	dBc
Two-Tone Intermodulation Distortion (IMD)[4]	+25°C	V		65			65		dBc
Differential Phase	+25°C	V		0.15			0.15		Degrees
Differential Gain	+25°C	V		0.25			0.25		%

Parameter	Temp	Test Level	AD9050BR/BRS Min	AD9050BR/BRS Typ	AD9050BR/BRS Max	AD9050BRS-60 Min	AD9050BRS-60 Typ	AD9050BRS-60 Max	Units
ENCODE INPUT									
Logic "1" Voltage	Full	IV	2.0			2.0			V
Logic "0" Voltage	Full	IV			0.8			0.8	V
Logic "1" Current	Full	IV			1			1	µA
Logic "0" Current	Full	IV			1			1	µA
Input Capacitance	+25°C	V		10			10		pF
Encode Pulse Width High (t_{EH})	+25°C	IV	10		166	6.7		166	ns
Encode Pulse Width Low (t_{EL})	+25°C	IV	10		166	6.7		166	ns
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	IV	4.95			4.95			V
Logic "0" Voltage	Full	IV			0.05			0.05	V
Logic "1" Voltage (3.0 V_{DD})	Full	IV	2.95			2.95			V
Logic "0" Voltage (3.0 V_{DD})	Full	IV			0.05			0.05	V
Output Coding			Offset	Binary	Code	Offset	Binary	Code	
POWER SUPPLY									
V_D, V_{DD} Supply Current[5]	Full	IV	40	63	80	40	69	87.2	mA
Power Dissipation[5]	Full	IV		315	400		345	486	mW
Power Supply Rejection Ratio (PSRR)[6]	+25°C	I			±10			±10	mV/V

NOTES
[1]"Gain Tempco" is for converter only; "Temperature Coefficient" is for bandgap reference only.
[2]Output propagation delay (t_{PD}) is measured from the 50% point of the rising edge of the encode command to the midpoint of the digital outputs with 10 pF maximum loads.
[3]RMS signal to rms noise with analog input signal 0.5 dB below full scale at specified frequency for BR/BRS, 1.0 dB below full scale for BRS-60.
[4]Intermodulation measured relative to either tone with analog input frequencies of 9.5 MHz and 9.9 MHz at 7 dB below full scale.
[5]Power dissipation is measured at full update rate with AIN of 10.3 MHz and digital outputs loaded with 10 pF maximum. See Figure 4 for power dissipation at other conditions.
[6]Measured as the ratio of the change in offset voltage for 5% change in $+V_D$.

Specifications subject to change without notice.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% Production Tested.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

ABSOLUTE MAXIMUM RATINGS*

V_D, V_{DD} . . . . . +7 V
ANALOG IN . . . . . –1.0 V to V_D + 1.0 V
Digital Inputs . . . . . –0.5 V to V_D
V_{REF} Input . . . . . –0.5 V to V_D
Digital Output Current . . . . . 20 mA
Operating Temperature
AD9050BR/BRS/BRS-60 . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9050BR	–40°C to +85°C	R-28
AD9050BRS	–40°C to +85°C	RS-28
AD9050BRS-60	–40°C to +85°C	RS-28

*R = Small Outline (SO); RS = Shrink Small Outline (SSOP).

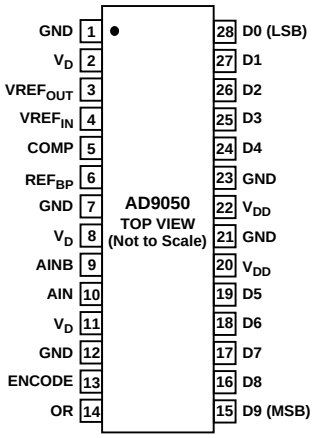
Table I. AD9050 Digital Coding (Single Ended Input AIN, AINB Bypassed to GND)

Analog Input	Voltage Level	OR (Out of Range)	Digital Output MSB . . . LSB
3.813	Positive Full Scale + 1 LSB	1	1111111111
3.300	Midscale	0	0111111111
2.787	Negative Full Scale – 1 LSB	1	0000000000

PIN FUNCTION DESCRIPTIONS

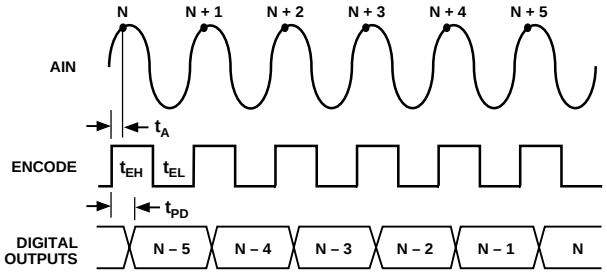
Pin No	Name	Function
1, 7, 12, 21, 23	GND	Ground.
2, 8, 11	V_D	Analog +5 V ± 5% power supply.
3	$VREF_{OUT}$	Internal bandgap voltage reference (nominally +2.5 V).
4	$VREF_{IN}$	Input to reference amplifier. Voltage reference for ADC is connected here.
5	COMP	Internal compensation pin, 0.1 μF bypass connected here to V_D (+5 V).
6	REF_{BP}	External connection for (0.1 μF) reference bypass capacitor.
9	AINB	Complementary analog input pin (Analog input bar).
10	AIN	Analog input pin.
13	ENCODE	Encode clock input to ADC. Internal T/H is placed in hold mode (ADC is encoding) on rising edge of encode signal.
14	OR	Out of range signal. Logic "0" when analog input is in nominal range. Logic "1" when analog input is out of nominal range.
15	D9 (MSB)	Most significant bit of ADC output.
16–19	D8–D5	Digital output bits of ADC.
20, 22	V_{DD}	Digital output power supply (only used by digital outputs).
24–27	D4–D1	Digital output bits of ADC.
28	D0 (LSB)	Least significant bit of ADC output.

PIN CONFIGURATION



CAUTION

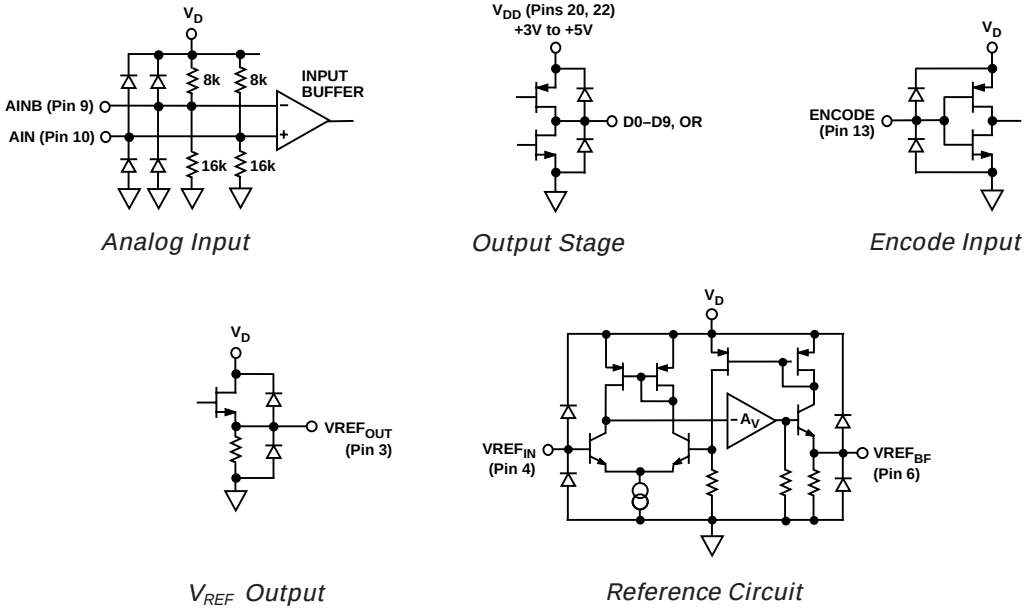
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9050 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



		MIN	TYP	MAX
t_A	APERTURE DELAY		2.7ns	
t_{EH}	PULSE WIDTH HIGH	10ns*		166ns
t_{EL}	PULSE WIDTH LOW	10ns*		166ns
t_{PD}	OUTPUT PROP DELAY	5.0ns	8.2ns	15.0ns

*FOR BR/BRS, SEE SPECIFICATION TABLE

Figure 2. Timing Diagram



Analog Input *Output Stage* *Encode Input*

V_{REF} Output *Reference Circuit*

Figure 3. Equivalent Circuits

AD9050–Typical Performance Curves

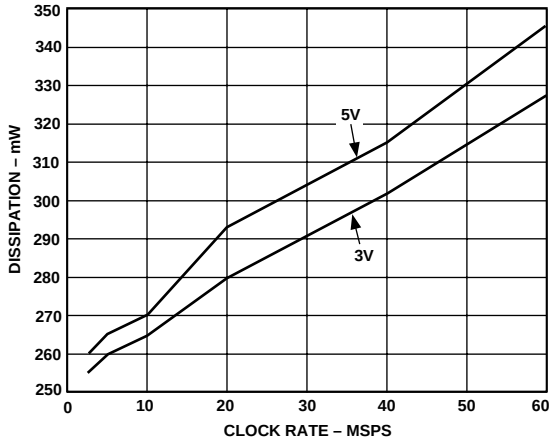


Figure 4. Power Dissipation vs. Clock Rate

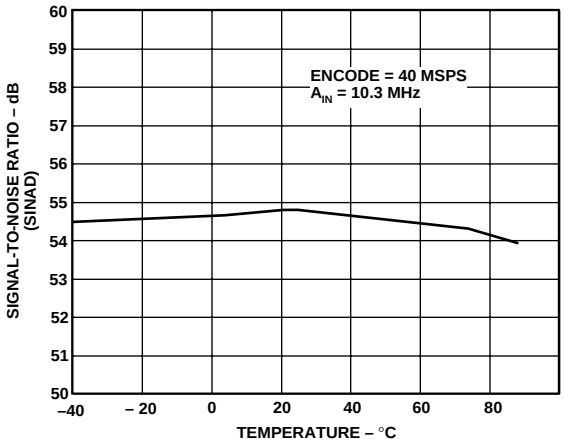


Figure 7. SNR vs. Temperature

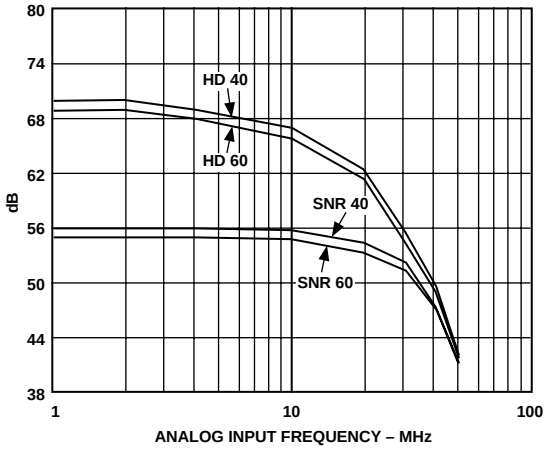


Figure 5. SNR/Distortion vs. Frequency

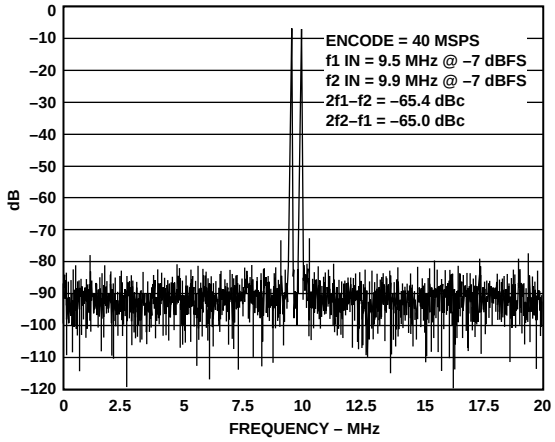


Figure 8. Two-Tone IMD

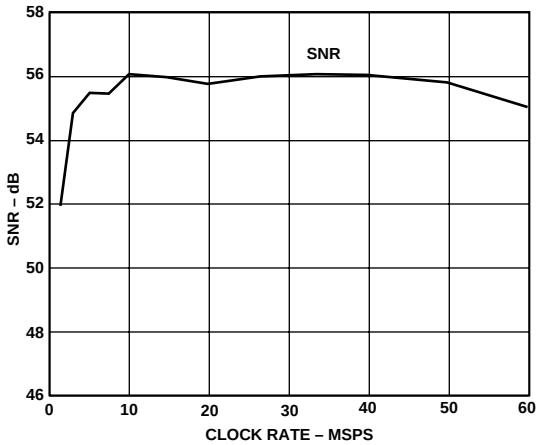


Figure 6. SNR vs. Clock Rate

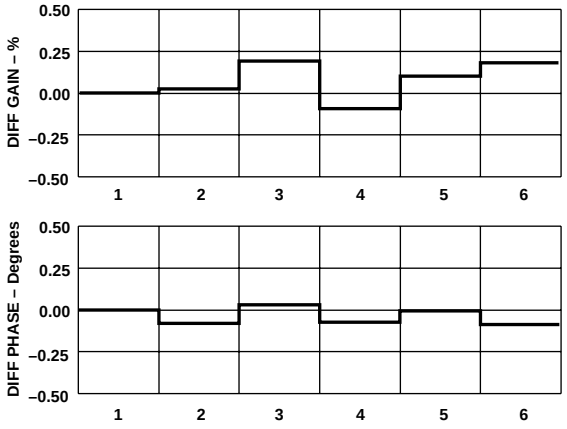


Figure 9. Differential Gain/Differential Phase

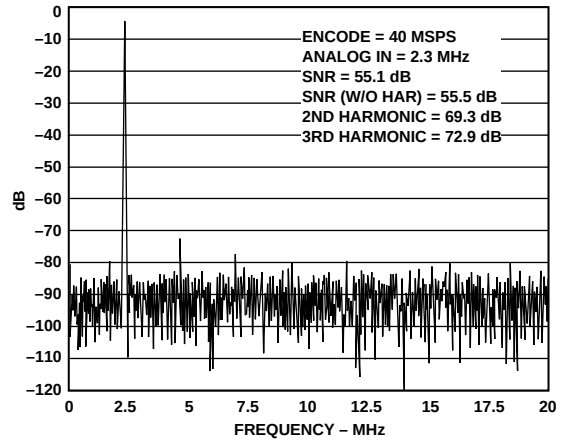


Figure 10. FFT Plot 40 MSPS, 2.3 MHz

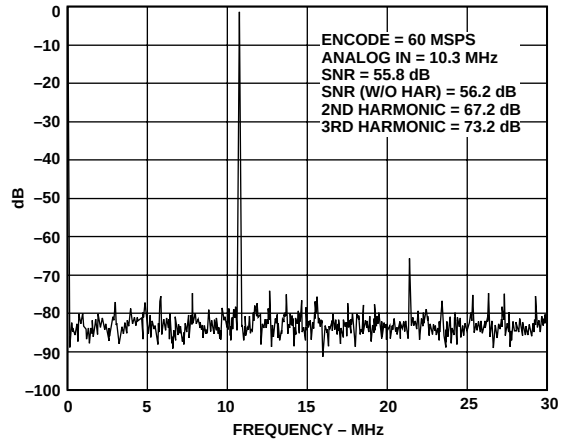


Figure 11. FFT Plot 60 MSPS, 10.3 MHz

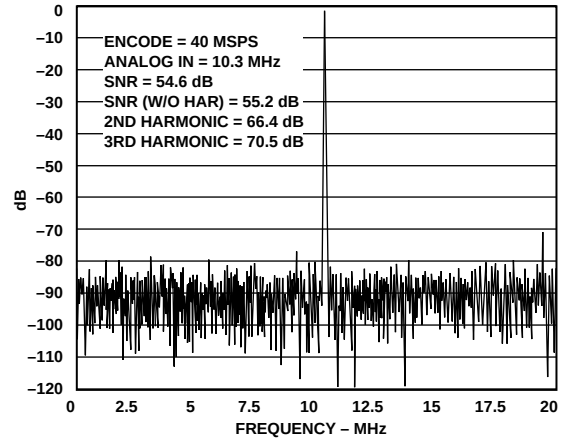


Figure 12. FFT Plot 40 MSPS, 10.3 MHz

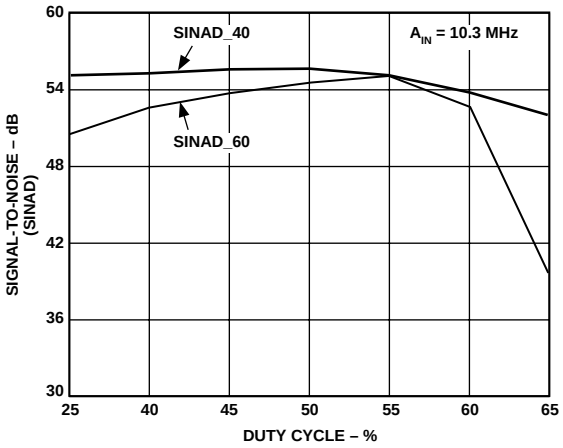


Figure 13. SNR vs. Clock Pulse Width

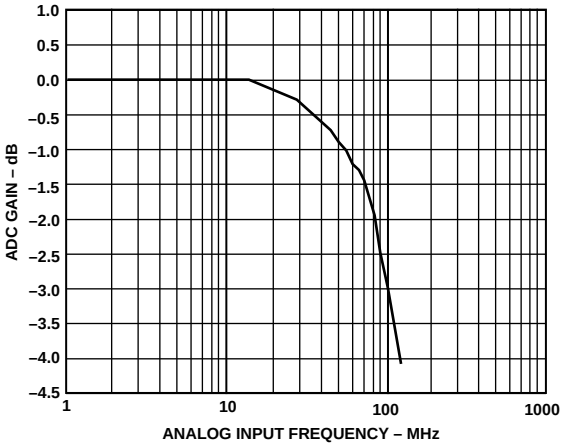


Figure 14. ADC Gain vs. AIN Frequency

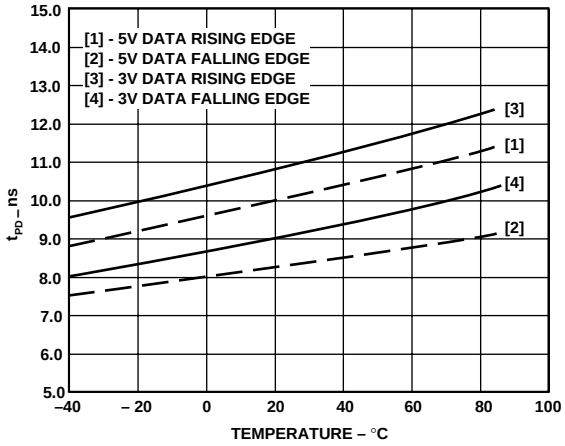


Figure 15. t_{PD} vs. Temperature 3 V/5 V

THEORY OF OPERATION

Refer to the block diagram on the front page.

The AD9050 employs a subranging architecture with digital error correction. This combination of design techniques ensures true 10-bit accuracy at the digital outputs of the converter.

At the input, the analog signal is buffered by a high speed differential buffer and applied to a track-and-hold (T/H) that holds the analog value present when the unit is strobed with an ENCODE command. The conversion process begins on the rising edge of this pulse. The two stage architecture completes a coarse and then a fine conversion of the T/H output signal.

Error correction and decode logic correct and align data from the two conversions and present the result as a 10-bit parallel digital word. Output data are strobed on the rising edge of the ENCODE command. The subranging architecture results in five pipeline delays for the output data. Refer to the AD9050 Timing Diagram.

USING THE AD9050

3 V System

The digital input and outputs of the AD9050 can be easily configured to directly interface to 3 V logic systems. The encode input (Pin 13) is TTL compatible with a logic threshold of 1.5 V. This input is actually a CMOS stage (refer to Equivalent Encode Input Stage) with a TTL threshold, allowing operation with TTL, CMOS and 3 V CMOS logic families. Using 3 V CMOS logic allows the user to drive the encode directly without the need to translate to +5 V. This saves the user power and board space. As with all high speed data converters, the clock signal must be clean and jitter free to prevent the degradation of dynamic performance.

The AD9050 outputs can also directly interface to 3 V logic systems. The digital outputs are standard CMOS stages (refer to AD9050 Output Stage) with isolated supply pins (Pins 20, 22 V_{DD}). By varying the voltage on the V_{DD} pins, the digital output levels vary respectively. By connecting Pins 20 and 22 to the 3 V logic supply, the AD9050 will supply 3 V output levels. Care should be taken to filter and isolate the output supply of the AD9050 as noise could be coupled into the ADC, limiting performance.

Analog Input

The analog input of the AD9050 is a differential input buffer (refer to AD9050 Equivalent Analog Input). The differential inputs are internally biased at +3.3 V, obviating the need for external biasing. Excellent performance is achieved whether the analog inputs are driven single-ended or differential (for best dynamic performance, impedances at AIN and AINB should match).

Figure 16 shows typical connections for the analog inputs when using the AD9050 in a dc coupled system with single ended signals. All components are powered from a single +5 V supply. The AD820 is used to offset the ground referenced input signal to the level required by the AD9050.

AC coupling of the analog inputs of the AD9050 is easily accomplished. Figure 17 shows capacitive coupling of a single ended signal while Figure 18 shows transformer coupling differentially into the AD9050.

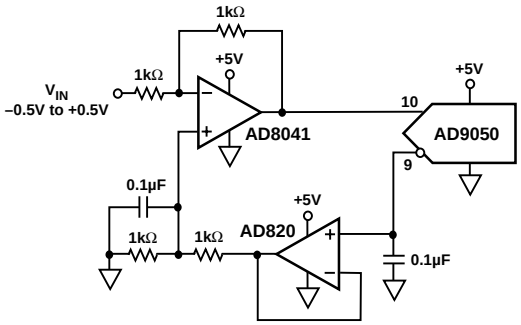


Figure 16. Single Supply, Single Ended, DC Coupled AD9050

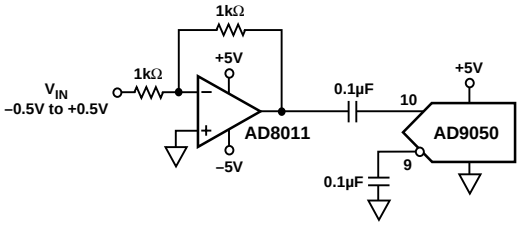


Figure 17. Single Ended, Capacitively Coupled AD9050

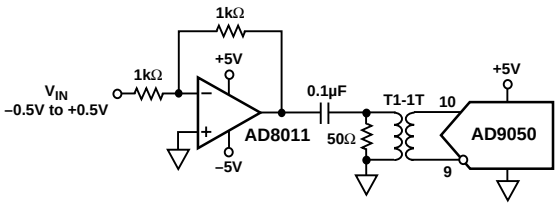


Figure 18. Differentially Driven AD9050 Using Transformer Coupling

The AD830 provides a unique method of providing dc level shift for the analog input. Using the AD830 allows a great deal of flexibility for adjusting offset and gain. Figure 19 shows the AD830 configured to drive the AD9050. The offset is provided by the internal biasing of the AD9050 differential input (Pin 9). For more information regarding the AD830, see the AD830 data sheet.

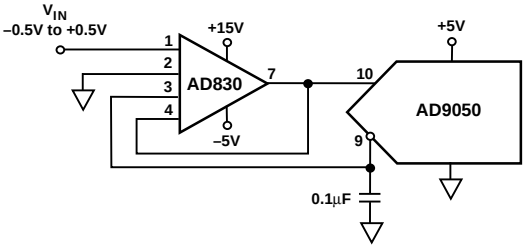


Figure 19. Level Shifting with the AD830

Overdrive of the Analog Input

Special care was taken in the design of the analog input section of the AD9050 to prevent damage and corruption of data when the input is overdriven. The nominal input range is +2.788 V to 3.812 V (1.024 V p-p centered at 3.3 V). Out-of-range comparators detect when the analog input signal is out of this range and shut the T/H off. The digital outputs are locked at their maximum or minimum value (i.e., all "0" or all "1"). This precludes the digital outputs from changing to an invalid value when the analog input is out of range.

When the analog input signal returns to the nominal range, the out-of-range comparators switch the T/H back to the active mode and the device recovers in approximately 10 ns.

The input is protected to one volt outside the power supply rails. For nominal power (+5 V and ground), the analog input will not be damaged with signals from +6.0 V to –1.0 V.

Timing

The performance of the AD9050 is very insensitive to the duty cycle of the clock. Pulse width variations of as much as ±10% will cause no degradation in performance. (see Figure 13, SNR vs. Clock Pulse Width).

The AD9050 provides latched data outputs, with five pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (refer to the AD9050 Timing Diagram). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9050; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9050 is 3 MSPS. Below a nominal of 1.5 MSPS the internal T/H switches to a track function only. This precludes the T/H from drooping to the rail during the conversion process and minimizes saturation issues. At clock rates below 3 MSPS dynamic performance degrades. The AD9050 will operate in burst mode operation, but the user must flush the internal pipeline each time the clock stops. This requires five clock pulses each time the clock is restarted for the first valid data output (refer to Figure 2 Timing Diagram).

Power Dissipation

The power dissipation specification in the parameter table is measured under the following conditions: encode is 40 MSPS or 60 MSPS, analog input is –0.5 dBFS at 10.3 MHz, the digital outputs are loaded with approximately 7 pF (10 pF maximum) and V_{DD} is 5 V. These conditions intend to reflect actual usage of the device.

As shown in Figure 4, the actual power dissipation varies based on these conditions. For instance, reducing the clock rate will reduce power as expected for CMOS-type devices. Also the loading determines the power dissipated in the output stages. From an ac standpoint, the capacitive loading will be the key (refer to Equivalent Output Stage).

The analog input frequency and amplitude in conjunction with the clock rate determine the switching rate of the output data bits. Power dissipation increases as more data bits switch at faster rates. For instance, if the input is a dc signal that is out of range, no output bits will switch. This minimizes power in the output stages, but is not realistic from a usage standpoint.

The dissipation in the output stages can be minimized by interfacing the outputs to 3 V logic (refer to USING THE AD9050, 3 V System). The lower output swings minimize consumption. Refer to Figure 4 for performance characteristics.

Voltage Reference

A stable and accurate +2.5 V voltage reference is built into the AD9050 (Pin 3, V_{REF} Output). In normal operation the internal reference is used by strapping Pins 3 and 4 of the AD9050 together. The internal reference has 500 µA of extra drive current that can be used for other circuits.

Some applications may require greater accuracy, improved temperature performance, or adjustment of the gain of the AD9050, which cannot be obtained by using the internal reference. For these applications, an external +2.5 V reference can be used to connect to Pin 4 of the AD9050. The $VREF_{IN}$ requires 5 µA of drive current.

The input range can be adjusted by varying the reference voltage applied to the AD9050. No appreciable degradation in performance occurs when the reference is adjusted ±5%. The full-scale range of the ADC tracks reference voltage changes linearly.

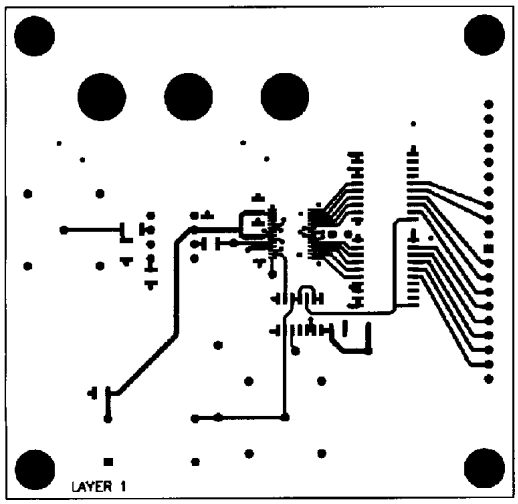


Figure 20. Evaluation Board Top Layer

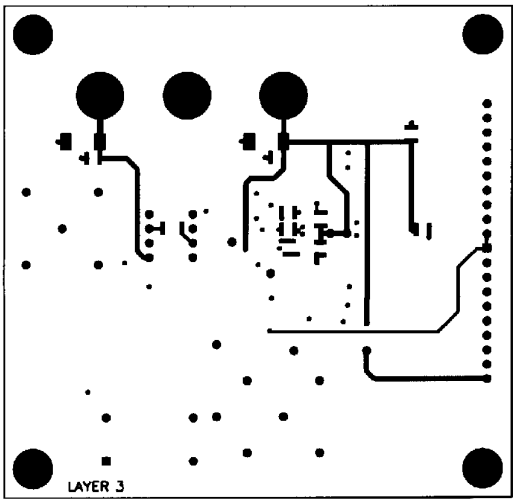


Figure 22. Evaluation Board Bottom Layer

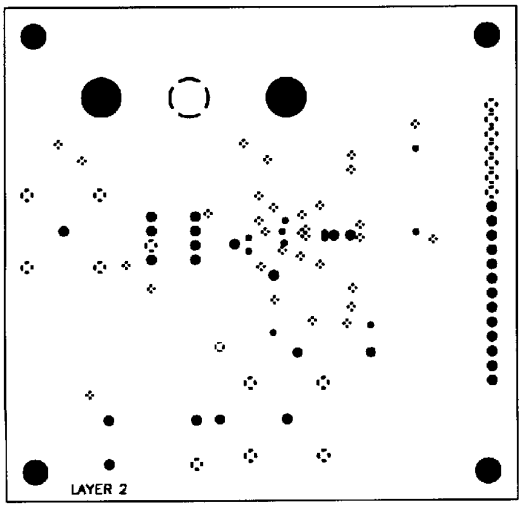


Figure 21. Evaluation Board Ground Layer

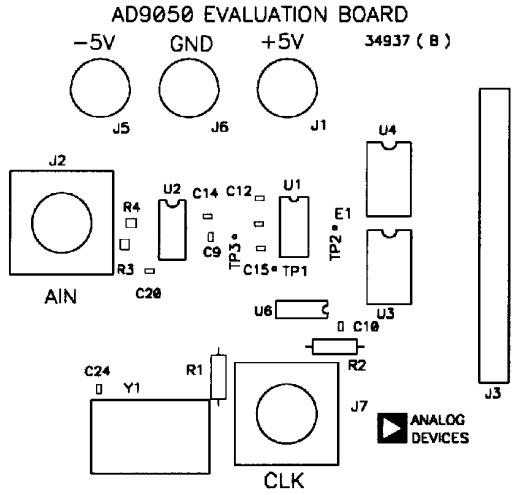


Figure 23. Silkscreen

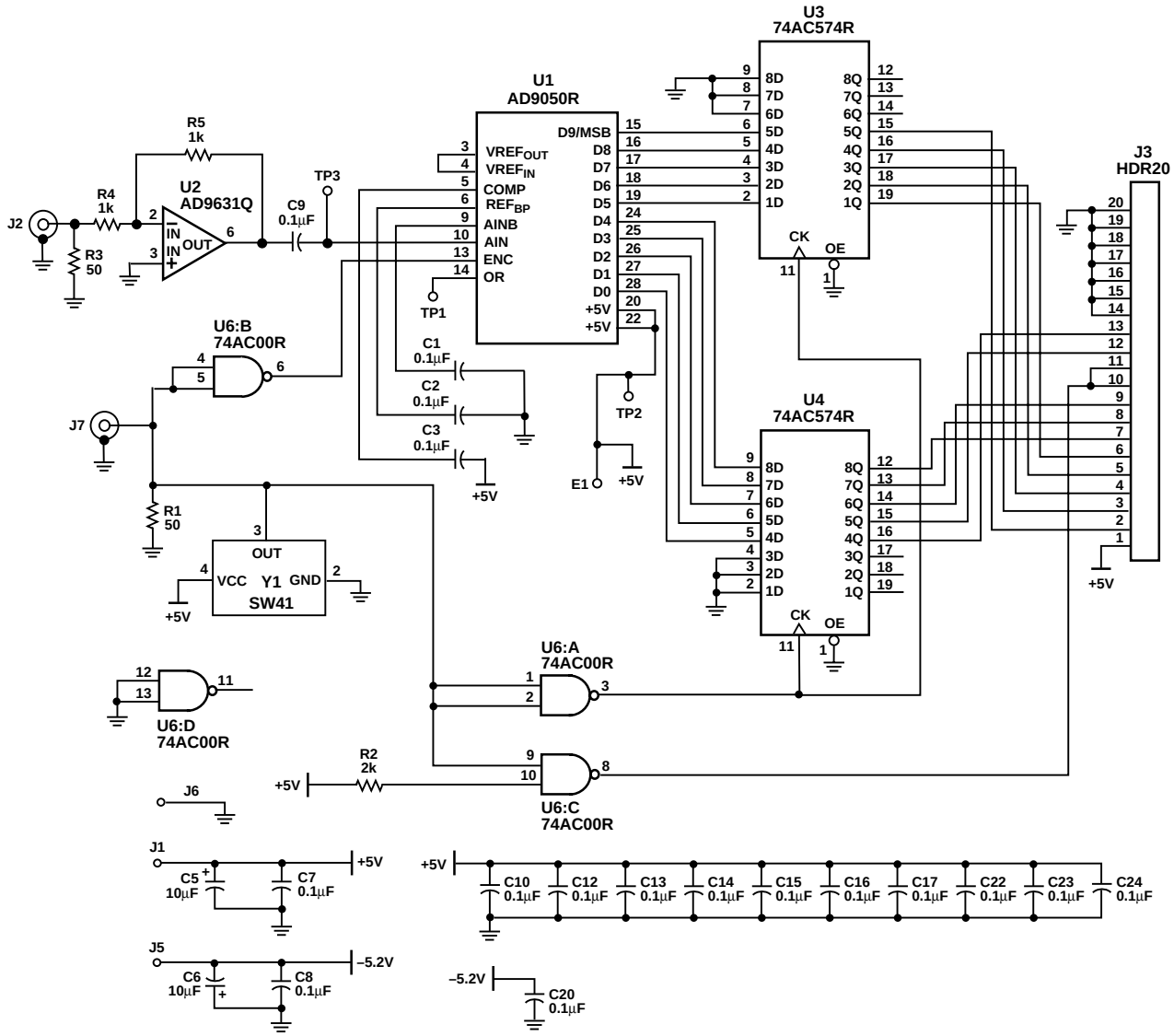
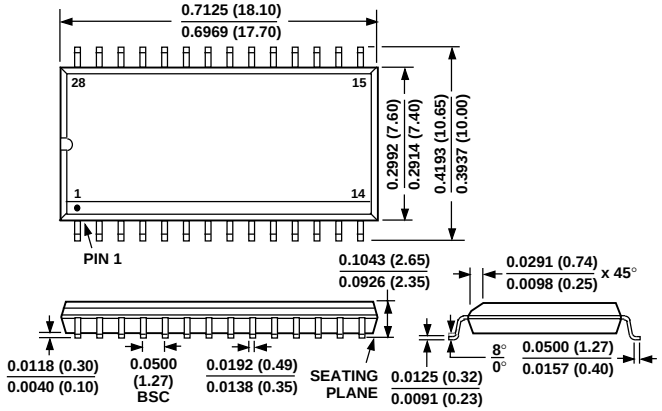


Figure 24. Evaluation Board Schematic

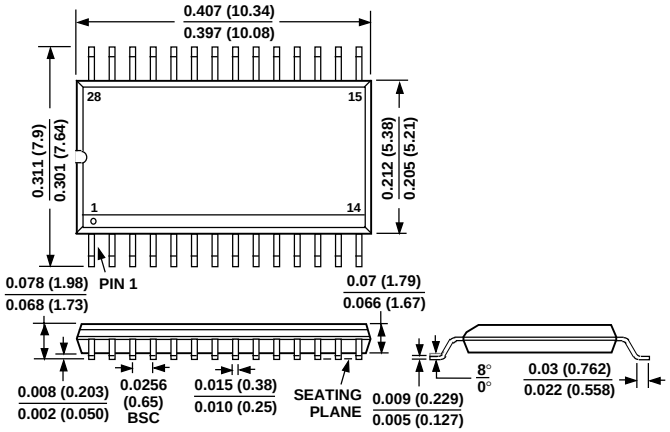
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead SOIC
(R-28)



28-Lead SSOP
(RS-28)



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