Sipex Corporation
SIGNAL PROCESSING EXCELLENCE

37kHz SAMPLING, 12-BIT A/D CONVERTER

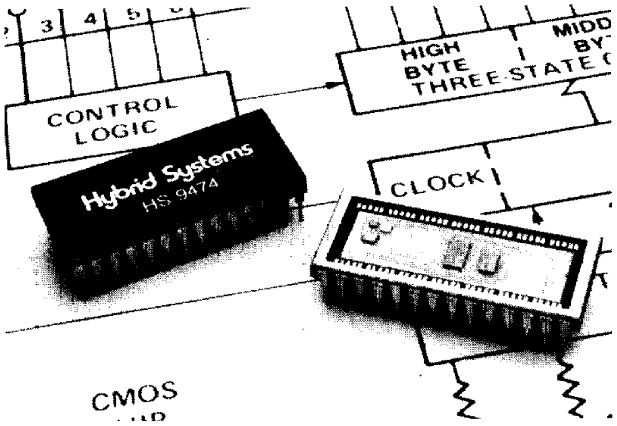
FEATURES

- Complete 12-bit A/D converter with reference, clock and three state outputs
- Internal sample-and-hold amplifier
- Internal hold capacitor
- Pin compatible with industry standard 574
- 37kHz throughput
- Low power: 390mW

DESCRIPTION

The HS9474 is a complete HS574 A/D converter with internal sample-hold amplifier. Requiring no external sample-hold connections, the HS9474 is pin for pin compatible with the industry standard 574. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. Incorporation of the sample-hold into the same circuit with the A/D converter reduces real estate, parts count, design time, and component interaction errors.

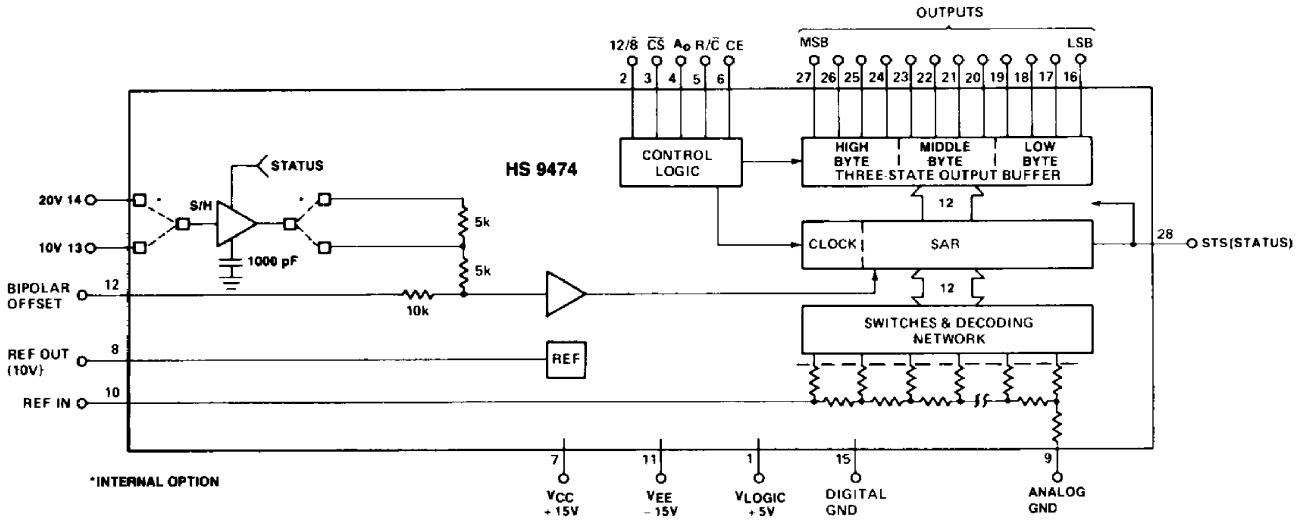
The sample-hold has a 7μsec acquisition time to 0.01% for a full 10V input change. A 1000 pF hold



capacitor is included in the circuit. Input voltage ranges available are ±5V or 0 to +10V for the -1 model and ±10V for the -2 model.

The HS9474 is offered in a hermetically-sealed ceramic package for use over a wide temperature range and for MIL-STD-883 Rev. C requirements.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

(Typical @ +25°C with V_{CC} = +15V, V_{EE} = −15V, V_{LOGIC} = +5V unless otherwise specified)

MODEL	HS 9474J	HS 9474K	HS 9474S	HS 9474T
RESOLUTION (max)	12 Bits	*	*	*
TYPE	Successive Approximation	*	*	*
ANALOG INPUTS				
Input Ranges		*	*	*
−1***	±5V, 0 to +10V	*	*	*
−2	±10V			
Input Impedance	$10^{10}\Omega$			
DIGITAL INPUTS				
Logic Inputs				
CE, $\overline{CS}$, R/$\overline{C}$, A_0, 12/$\overline{8}$		*	*	*
Logic 1	+2.4V min, +5.5V max	*	*	*
Logic 0	−0.5V min, +0.8V max	*	*	*
Current	±5μA max	*	*	*
Capacitance	5pF			
Minimum Start Pulse		*	*	*
CE-Positive	50nsec	*	*	*
$\overline{CS}$-Negative	50nsec	*	*	*
R/$\overline{C}$-Negative	50nsec			
DIGITAL OUTPUTS				
Logic Outputs				
DB_{11}-DB_0, STS		*	*	*
Logic 0	+0.4V max, I_{SINK} ≤1.6mA	*	*	*
Logic 1	+2.4V min, I_{SOURCE} ≤500μA	*	*	*
Leakage (High Z State)	±5μA max (Data Bits Only)	*	*	*
Capacitance	5pF			
Parallel Data				
Output Codes		*	*	*
Unipolar	Positive True Binary	*	*	*
Bipolar	Positive True Offset Binary			
REFERENCE				
Internal	10.00 ±0.1 Volts max	*	*	*
Output Current	1.5mA****	*	*	*
CONVERSION TIME	18μsec (25μsec max)	*	*	*
ACQUISITION TIME	7μsec (10μsec max)	*	*	*
ACCURACY				
Linearity (% of F.S.R. max)	±0.025	±0.012	±0.025	±0.012
Monotonicity (Bits)[2]				
No Missing Codes	11	12	11	12
Offset[3]		*	*	*
Unipolar (% of F.S.R. max)	±0.05			
Bipolar (% of F.S.R. max)	±0.25	±0.1	±0.25	±0.1
Gain[3, 4] (% to F.S.R. max)	±0.3	*	*	*
STABILITY				
Linearity (ppm/°C max)				
0°C to +70°C	±0.5	*	±0.5	**
−55°C to +125°C			±0.5	**
Unipolar Offset (ppm/°C max)				
0°C to +70°C	±10	±5	±10	±5
−55°C to +125°C				
Bipolar Offset (ppm/°C max)				
0°C to +70°C	±15	±10	±15	±10
−55°C to +125°C				
Gain (Scale Factor)(ppm/°C max)				
0°C to +70°C	±50	±27	±50	±25
−55°C to +125°C				
POWER SUPPLY				
V_{LOGIC}	+4.5 to +5.5 Volts @ 3mA max	*	*	*
V_{CC}	+13.5 to +16.5 Volts @ 12.5mA typ, 17mA max	*	*	*
V_{EE}	−13.5 to −16.5 Volts @ 8mA max	*	*	*
Power Dissipation	390mW max	*	*	*
Rejection[5]		*	*	*
V_{LOGIC}	±0.002%/%	*	*	*
V_{CC}, V_{EE}	±0.005%/%			
TEMPERATURE RANGE				
Operating	0°C to +70°C	*	−55°C to +125°C	
Storage	−25°C to +85°C	*	−65°C to +150°C	

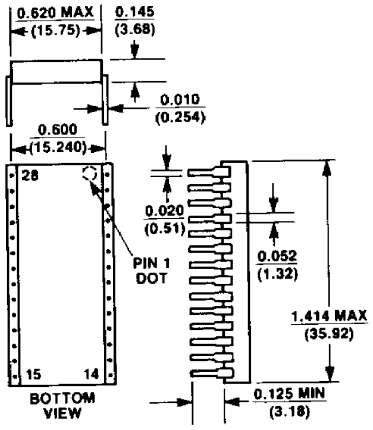
NOTES:

1. Conversion time shown for a complete 12 bit conversion. 2. T_{min} to T_{max}. 3. Externally adjustable to zero. See application information. 4. Connect 50Ω between REF OUT and REF IN initial gain and offset adjustable to zero. 5. Maximum change over rated supply range

*Specifications same as HS 9474J **Specifications same as HS 9474S

***Input range selected at factory ****Recommend buffer for external use.

PACKAGE OUTLINE



PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	V_{LOGIC}	28	STS
2	12/$\overline{8}$	27	DB_{11}(MSB)
3	$\overline{CS}$	26	DB_{10}
4	A_0	25	DB_9
5	R/$\overline{C}$	24	DB_8
6	CE	23	DB_7
7	V_{CC}	22	DB_6
8	REF OUT	21	DB_5
9	ANA GND(AC)	20	DB_4
10	REF IN	19	DB_3
11	V_{EE}	18	DB_2
12	BIP OFF	17	DB_1
13*	$10V_{IN}$ (−1)	16	DB_0(LSB)
14*	$20V_{IN}$ (−2)	15	DIGITAL GND

*Input not selected at factory will not be connected.

ABSOLUTE MAXIMUM RATINGS

V_{CC} to Digital Common ..... 0 to +16.5V
V_{EE} to Digital Common ..... 0 to −16.5V
V_{LOGIC} to Digital Common ..... 0 to +7V
Analog Common to Digital Common ..... ±1V
Control Inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... −0.5V to V_{LOGIC} +0.5V
Analog Inputs (REF IN, BIP OFF, V_{IN}) to Analog Common ..... ±16.5V
REF OUT ..... Indefinite short to common
Momentary short to V_{CC}
Power Dissipation 1000mW
Lead Temperature, Soldering ..... 300°C, 10sec

CONTROL FUNCTIONS

The HS 9474 contains all control functions necessary to provide for complete microprocessor interface and also 'stand alone' operation including continuous conversions. All control functions are defined in Table 1 and Table 2.

Function	Definition	Function
CE	Chip Enable	1. Typically used as clock synchronization with µP. 2. Must be high (1) for a conversion to start. 3. Must be high (1) to read data on the output. 4. ⌐ transition may be used to initiate conversion.
$\overline{CS}$	Chip Select	1. Typically the address pin when used with µP. 2. Must be low (0) for a conversion to start or read data at the output. 3. ¬ transition may be used to initiate conversion.
R/$\overline{C}$	Read/Convert	1. ¬ initiate conversion 2. ⌐ initiate read
A_0	Address	1. Selects conversion mode. 12 Bits if low (0). 8 Bits if high (1). 2. In read mode A_0 selects the output format. If low (0) then 8 MSB's (high and middle byte) or if high (1) then only low byte and trailing zeros.
12/$\overline{8}$	Output Format	1. Must be hard wired. 2. Normal 12 Bit format if high (1). 3. 8-Bit format as set by A_0 if low (0).

Table 1. Defining the Control Functions

CONTROL INPUTS					HS 9474 OPERATION
CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	
0	X	X	X	X	No Operation
X	1	X	X	X	No Operation
1	0	¬	X	0	Initiates 12-Bit Conversion
1	0	¬	X	1	Initiates 8-Bit Conversion
⌐	0	0	X	0	Initiates 12-Bit Conversion
⌐	0	0	X	1	Initiates 8-Bit Conversion
1	¬	0	X	0	Initiates 12-Bit Conversion
1	¬	0	X	1	Initiates 8-Bit Conversion
1	0	⌐	Pin 1	X	Enables 12-Bit Parallel Output
1	0	⌐	Pin 15	0	Enables 8 MSB's
1	0	⌐	Pin 15	1	Enables 4 LSB's and 4 Trailing Zeros

NOTES: 1. 1 indicates logic HIGH.
2. 0 indicates logic LOW.
3. X indicates don't care.
4. ⌐ indicates operation commences on low to high transition.
5. MSB → XXXX XXXX XXXX ← LSB
High Byte Middle Byte Low Byte
6. Not a common use of this function.
7. When using the HS 9474 in the 8-bit bus mode with 12-bit resolution, the high byte must be externally hard wired to the low byte.

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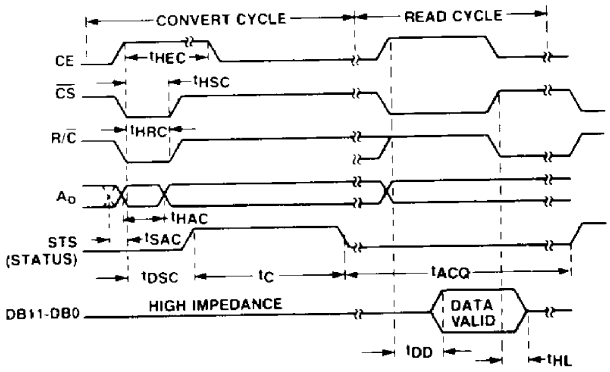
TIMING

The timing diagrams are shown in Fig. 1. Note that to start a conversion CS, CE, and R/C must have an overlap time of 50ns minimum. CS and R/C may be advanced or delayed if needed (by the application) but no specifications are given for this — only the coincidence of 50ns must be met. Typically R/C is used to initiate a conversion — however other lines may be used. See truth table (Table 2).

In the READ mode **note the access time t_{DD} is 75ns typ, 150ns max. This means that an entire conversion can be completed and read in 20 μs typ, 25 μs max** including setup, conversion time and access time.



CONVERT CYCLE

SYMBOL	PARAMETER	
t_{ACQ}	Acquisition Time	7 μs typ, 10 min
t_{HEC}	CE Pulse Width	50ns min
t_{HSC}	CS LOW during CE high	50ns min
t_{HRC}	R/C LOW during CE high	50ns min
t_{HAC}	A_0 valid during CE high	50ns min
t_{SAC}	Maximum A_0 delay from CE. Set up as shown (negative time wrt* CE) not needed	0ns max
t_{DSC}	STS delay from CE	200ns max
t_C	Conversion time	
	8 Bit cycle	13 μs typ, 19 μs max
	12 Bit cycle	20 μs typ, 25 μs max

CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, CS, R/C, as shown in Table 1. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be setup at least 50ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in Figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if A_0 changes state after a conversion begins, an additional Start Convert command will latch the new state of A_0 and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READ CYCLE

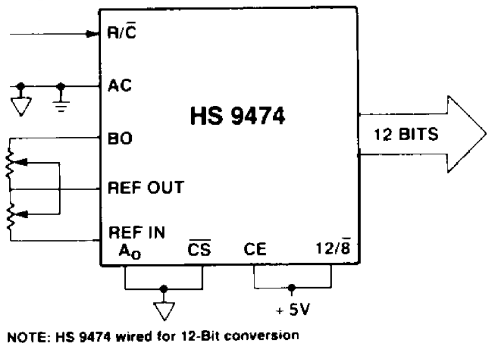
t_{DD}	Access time from CE high	75ns typ, 150ns max
t_{HL}	Output Float Delay	150ns max

*wrt = With Respect To.

Figure 1. HS 9474 Interface Timing

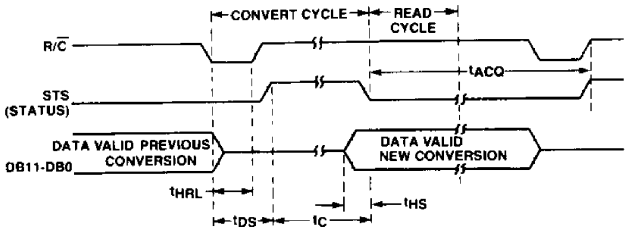
STAND-ALONE OPERATION

The HS 9474 can be used in a 'stand-alone' mode in systems having dedicated input ports. Connections and timing for this mode are shown in Fig. 2.



NOTE: HS 9474 wired for 12-Bit conversion

R/C NEGATIVE PULSE



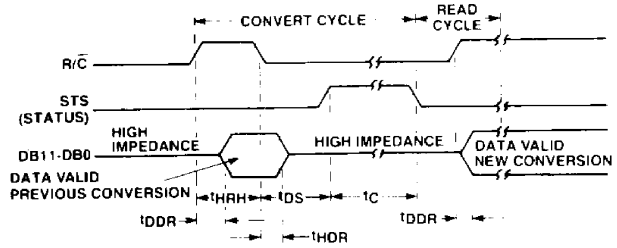
CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HRL}	Low R/C Pulse Width	50ns min
t_{DS}	STS Delay from R/C	200ns max
t_C	Conversion Time	25 μs max
t_{HS}	Data valid after STS low	70ns max
t_{ACQ}	Acquisition Time	7 μs typ
		10μs max

READ CYCLE

1. Data always in 'read' mode except during a conversion in which data lines revert to high impedance.
2. Output always valid after conversion is complete

R/C POSITIVE PULSE



CONVERT CYCLE

SYMBOL	PARAMETER	
t_{HDR}	Valid Data (Previous Conversion) after R/C low	25ns min
t_{HRH}	High R/C Pulse Width	150ns min
t_{DS}	STS Delay from R/C	200ns max
t_{DDR}	Data Access Time	150ns max
t_C	Conversion Time	25 μs max

READ CYCLE

1. Converter output remains in high impedance state after conversion (STS goes low) until R/C goes high (to 'read' data).

Figure 2. HS 9474 Stand-Alone Operation
Top: Using negative R/C pulse
Bottom: Using positive R/C pulse

CONTINUOUS CONVERSION

Requirements for self triggered-continuous conversions are popular applications for an analog to digital converter, see Fig. 3.

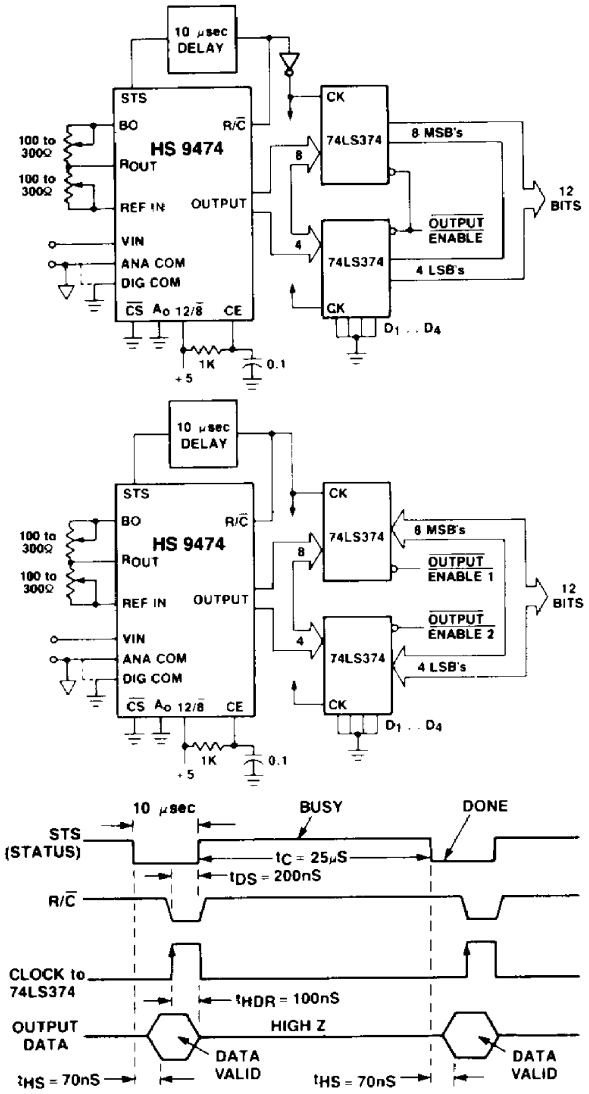


Figure 3. Continuous Conversion
Top: DATA BUS 12 Bits or greater
Bottom: DATA BUS 8 Bits

$\overline{CS}$ and A_0 are tied low (0) while 12/$\overline{8}$ is tied high (1) to select the converter and enable a 12-Bit conversion. Note A_0 is 'don't care' in the truth table.

CE is connected to a 1KΩ and 0.1μF integrator as shown, this ensures an initial conversion on power up. CE will see a rising edge which will initiate a conversion ($\overline{CS}$ = 0, R/$\overline{C}$ = 0). The RC network will then integrate the initial 1 at the output of the first inverter causing a delay in the R/$\overline{C}$ command. After the first conversion, continuous conversions are caused by delaying the STATUS (STS) into R/$\overline{C}$. After the conversion is complete the output data lines come out of tri-state approximately 70ns after STS goes low (DONE). Data will remain valid (from previous conversion) 100ns after the new R/$\overline{C}$ ⌐└ command which allows for the positive edge ┘‾ triggered data to be loaded into the external buffer (75LS374 or equivalent).

Using the R-C network as shown, 1.5μs is allowed between conversions. Shorter times can be used but a longer time will cause long rise and fall of the R/$\overline{C}$ line and the clock input to the buffer. The setup time for the latch shown is 20ns and the hold time is 0ns.

The user may access the octal latches asynchronously by means of the $\overline{OUTPUT\ ENABLE}$ (CONTROL OUTPUT) line. The data will always be valid,for a 12-bit conversion. Using this method, data will always be current and the STATUS bit need not be tested for valid data.

USING THE A_0 LINE

The state of the A_0 line at the start of a conversion places the HS 9474 in either a full 12-bit conversion or in an 8-bit 'short cycle' mode. During a READ at the end of a conversion the A_0 line is used to the format of the data as follows:

1. Prior to Conversion

	MODE
$A_0 = 1$	Short cycle 8-bit conversion
$A_0 = 0$	Full 12-bit conversion

2. After Conversion (READ)

$A_0 = 1$	Data = Low Byte (LSB) followed by zeros
$A_0 = 0$	Data = High Byte (MSB's) followed by middle and low byte.

In a μP application the A_0 line can be considered a pair of $\overline{WR}$ locations as follows:

1. Prior to Conversion (WRITE)

	MODE
$\overline{WR}$ = 0 in low address ($A_0 = 0$)	Full 12-bit conversion
$\overline{WR}$ = 0 in high address ($A_0 = 1$)	Short cycle 8-bit conversion

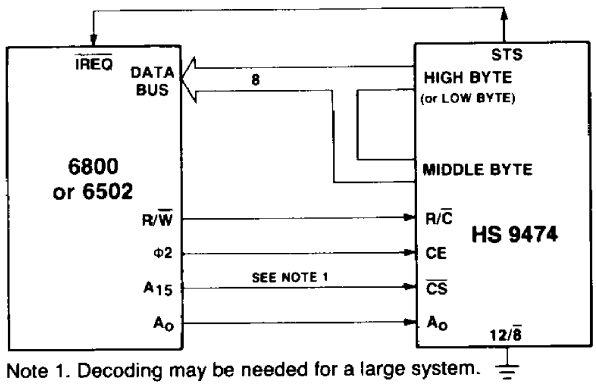
2. After Conversion (READ)

$\overline{WR}$ = 1 in either address ($A_0 = X$)	Full 12-bit word with 12/$\overline{8}$ = 1
$\overline{WR}$ = 1 in high address ($A_0 = 1$)	LSB's & zeros when 12/$\overline{8}$ = 0
$\overline{WR}$ = 1 in low address ($A_0 = 0$)	8 MSB's only when 12/$\overline{8}$ = 0

INTERFACING THE HS 9474 WITH 8-BIT MICROPROCESSORS

The HS 9474 which has 12-bit data can be used directly with popular 8-bit microprocessors. The data however, must be multiplexed by setting the output mode select 12/$\overline{8}$ pin to GND.

In the first case, a 6800 (or 6502) is used. See Figure 4.



Note 1. Decoding may be needed for a large system.

Figure 4. Interfacing the HS 9474 and a 6800 μP

The STATUS (STS) is tied directly to $\overline{IREQ}$ which is the interrupt line. When STS goes to 0 (at the end of a conversion) the 6800 may either service the interrupt or be timed for 25μs (since this $\overline{IREQ}$ is software maskable) the time required for a conversion.

Figure 5 shows the 8080A μP as interfaced with the HS 9474. In this case, a 8228 controller is shown with gates to generate needed signals.

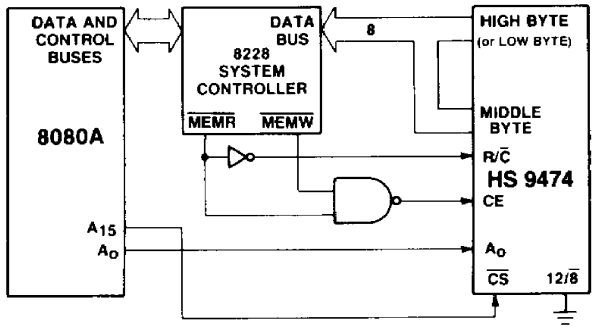


Figure 5. Interfacing the HS 9474 and 8080A μP

Figure 6 shows the HS 9474 connected with a 8048 μP. A single NAND gate is used to generate CE.

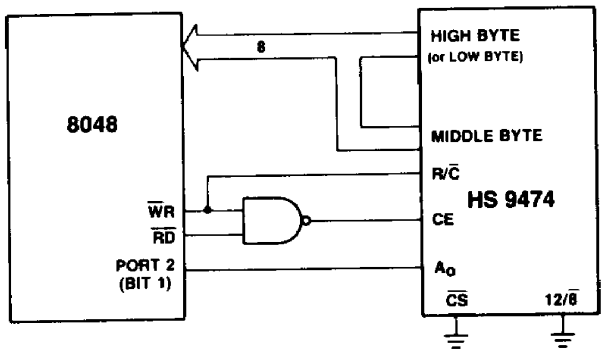


Figure 6. Interfacing the HS 9474 and a 8048 μP

A summary of μP types and connections is in Table 3.

MICRO-PROCESSOR	HS 9474 CONTROL INPUTS			
	CE	R/$\overline{C}$	$\overline{CS}$	A_0
8080 MEMORY MAPPED I/O	$\overline{(\overline{MEMW} \cdot \overline{MEMR})}$	$\overline{(MEMR)}$	DECODED ADDRESS	A_0
PROGRAMMED I/O	$\overline{(I/OW \cdot I/OR)}$	$\overline{(I/OR)}$		
6800	ϕ_2	R/$\overline{W}$	DECODED ADDRESS	A_0
6502	ϕ_2	R/$\overline{W}$	DECODED ADDRESS	A_0
Z80 MEMORY MAPPED I/O	$\overline{(\overline{RD} \cdot \overline{WR})}$	$\overline{(\overline{RD})}$	DECODED ADDRESS WITH MREQ	A_0
PROGRAMMED I/O	$\overline{(\overline{RD} \cdot \overline{WR})}$	$\overline{(\overline{RD})}$	DECODED ADDRESS WITH IOR	A_0
8048	$\overline{(\overline{RD} \cdot \overline{WR})}$	$\overline{(\overline{RD})}$	PORT 2_{0-3}*	PORT 2_{0-3}*

*Port 2, Lines 0-3 can be used as a 4-Bit address bus. System address decoding requirements vary from no hardware to a fully latched 12-Bit address, depending on system complexity.

Table 3. Summary of HS 9474 Control Inputs with Various Microprocessors

ENABLING DATA IN 8-BIT MODE

To operate the HS 9474 in a 12-bit conversion mode with an 8-bit data bus, use the basic configuration shown in Figure 7. The A_0 control can be connected to the least significant bit of the data bus in order to store the output data into two consecutive memory locations. When A_0 is pulled low, only the 8 MSB's are enabled. When A_0 is high, the 4 MSB's are disabled, bits 4 through 7 are forced to a zero and the 4 LSB's are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1. A_0 may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between two data bytes. This assures that the outputs which are strapped together in Figure 7 will never be enabled at the same time.

ZERO AND GAIN CONNECTIONS

The HS 9474 is normally used with external zero and gain calibration potentiometers. However, if maximum accuracy is not required, they may be omitted. If no trims are used, the gain calibration will be within approximately $\pm$2LSB zero offset error, and $\pm$12LSB maximum full scale error. See Figure 8 for connection with no trims. If gain and zero adjustment potentiometers are used, they should be connected as shown in Figure 9. The zero control has a range of about $\pm$20LSB, and the gain control has a range of about $\pm$13LSB.

Proper gain and zero calibration requires great care and the use of extremely sensitive and accurate instruments. The voltage source used as a signal input must be very stable. It also should be capable of being set to within 1/10LSB at both ends of its range.

The HS 9474's zero and gain adjustments are independent of each other if the zero (or offset) adjustment is made first.

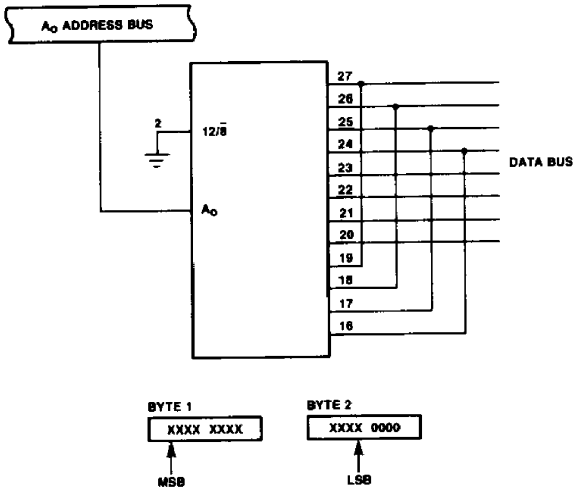
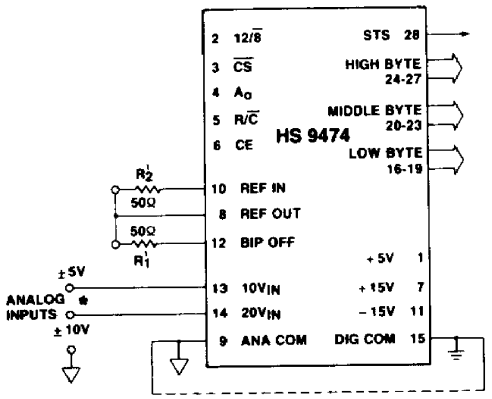
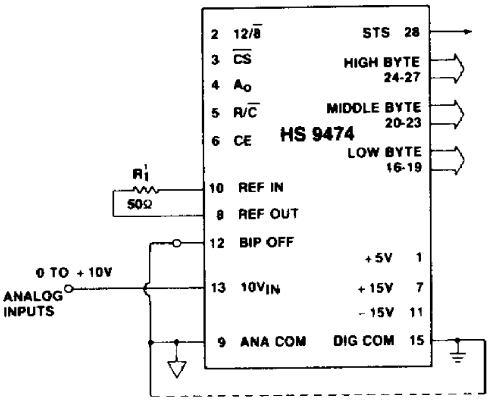


Figure 7. Enabling Data in 8-Bit Mode



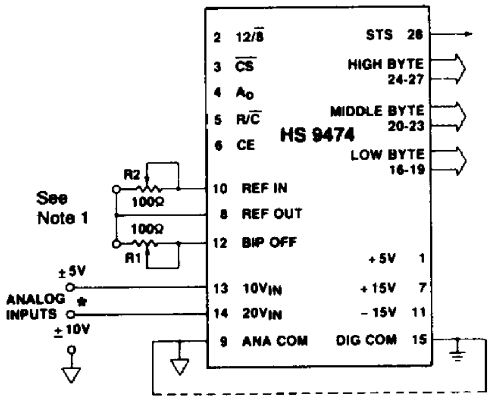
1. 50Ω ±1% metal film

Figure 8a. No Trim Biplor Input Connections



1. 50Ω ±1% metal film

Figure 8b. No Trim Unipolar Input Connections

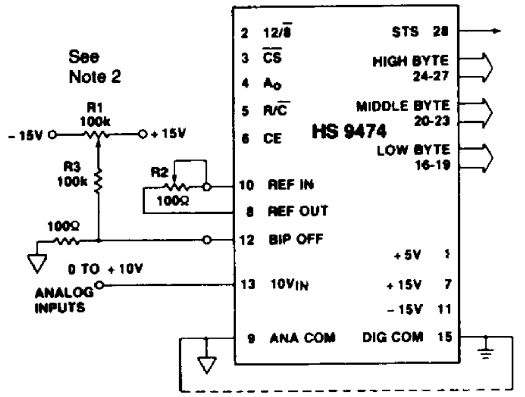


1. To increase adjustment range:
   a) Change R1 and R2 to 300 .
   b) Add series resistor 100Ω to ±5V input and 200Ω to ±10V input.

*Selected at factory.

**May be changd to 300Ω for greater adjustment capability.

Figure 9a. Bipolar Input Connections with Trim Adjustment



2. To increase adjustment range:
   a) Change R3 to 33kΩ, and R2 to 300
   b) Add series resistor 100Ω to ±5V input and 200Ω to ±10V input.

Figure 9b. Unipolar Input Connections with Trim Adjustment

ZERO ADJUSTMENT PROCEDURE

1. For unipolar ranges:
   a) Set input voltage precisely to +½LSB.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001.
2. For bipolar ranges:
   a) Set input voltage precisely to ½LSB above — F.S.
   b) Adjust zero control until converter is switching from 000000000000 to 000000000001

GAIN ADJUSTMENT PROCEDURE

1. Set input voltage precisely to ½LSB less than 'all bits on' value. Note that this is 1½LSB less than nominal full scale.
2. Adjust gain control until converter is switching from 111111111110 to 111111111111.

Table 4 summarizes the zero and gain adjustment procedure, and shows the proper input test voltages used in calibrating the HS 9474.

Table 4. Calibration Data

Input Voltage Range	Adjust-ment	Input Voltage	Adjust input to point where converter is just on the verge of switching between the two codes shown.[1]
-1 Model	ZERO	1.22mV	0000 0000 000Ø
0 to +10V	GAIN	9.9963V	1111 1111 111Ø
-1 Model	ZERO	-4.9988V	0000 0000 000Ø
±5V	GAIN	4.9963V	1111 1111 111Ø
-2 Model	ZERO	-9.9976V	0000 0000 000Ø
±10V	GAIN	9.9927V	1111 1111 111Ø

[1]Codes shown are natural binary for unipolar input ranges and offset binary for bipolar ranges.
Ø = a transition between logic "1" and logic "0".

POWER SUPPLY CONSIDERATION

Power supplies used for the HS 9474 should be selected for low noise operation. In particular they should be free of high frequency noise. Unstable output codes may result with noisy power sources. It is important to remember that 2.44mV is 1LSB for a 10 volt input.

Decoupling capacitors are recommended on all power supply pins located as close to the converter as possible. Suitable decoupling capacitors are 10 μF tantalum type in parallel with 0.1 μF disc ceramic type.

GROUNDING CONSIDERATIONS

The analog common at pin 9 is the ground reference point for the internal reference and is thus the high quality ground for the HS 9474; it should be connected directly to the analog reference point of the system. In order to achieve all of the high accuracy performance available from the HS 9474 in an environment of high digital noise content, it is recommended that the analog and digital commons be connected together at the package. In some situations, the digital common at pin 15 can be connected to the most convenient ground reference point; analog power return is preferred. If digital common contains high frequency noise beyond 200mV, this noise may feed through the converter, so that some caution will be required.

It is also important in the layout, to carefully consider the placement of digital lines. It is recommended that digital lines not be run directly under the 9474. For optimum system performance, if space permits, a ground plane is advised under the 9474. This should be connected to a digital ground. Finally, in packaging the assembled 9474, the designer should also try to minimize any capacitive coupling that might occur at the top to the device.

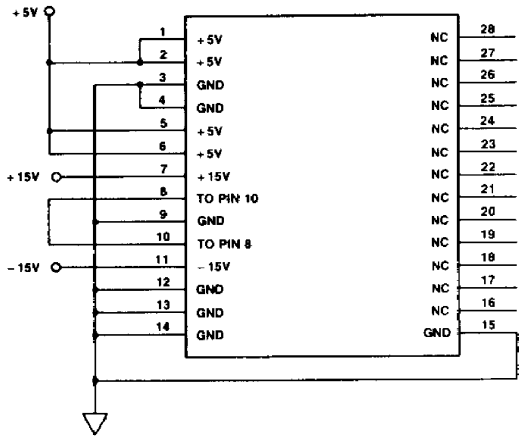


Figure 10. Burn-In Schematic

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ORDERING INFORMATION

MODEL NUMBER	RESOLUTION MONOTONICITY	INPUT RANGE(S)	TEMPERATURE RANGE	SCREENING
HS 9474J-1	11 Bits	±5V, 0 to +10V	0° to +70°C	
HS 9474J-2	11 Bits	±10V	0° to +70°C	
HS 9474K-1	12 Bits	±5V, 0 to +10V	0° to +70°C	
HS 9474K-2	12 Bits	±10V	0° to +70°C	
HS 9474S/B-1	11 Bits	±5V, 0 to +10V	−55°C to +125°C	883 Rev. C, Level B
HS 9474S/B-2	11 Bits	±10V	−55°C to +125°C	883 Rev. C, Level B
HS 9474T/B-1	12 Bits	±5V, 0 to +10V	−55°C to +125°C	883 Rev. C, Level B
HS 9474T/B-2	12 Bits	±10	−55°C to +125°C	883 Rev. C, Level B

Specifications subject to change without notice.