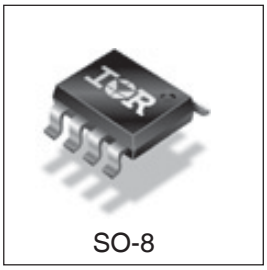
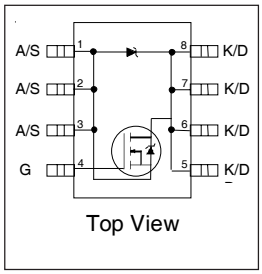
International
IOR Rectifier

# IRF7807VD1PbF-1

## FETKY™ MOSFET / SCHOTTKY DIODE

| | | |
|---|---|---|
| $V_{DS}$ | 30 | V |
| $R_{DS(on)\ max}$ (@$V_{GS}$ = 4.5V) | 25 | mΩ |
| $Q_{g\ (typical)}$ | 9.5 | nC |
| $Q_{SW\ (typical)}$ | 3.4 | nC |
| $Q_{OSS\ (typical)}$ | 12 | nC |
| $I_D$ (@$T_A$ = 25°C) | 8.3 | A |


SO-8



Top View

### Applications

- Co-Pack N-channel HEXFET® POWER MOSFET and Schottky Diode
- Ideal for Synchronous Rectifiers in DC-DC

| Features | ⇒ | Benefits |
|---|---|---|
| Industry-standard pinout SO-8 Package | | Multi-Vendor Compatibility |
| Compatible with Existing Surface Mount Techniques | | Easier Manufacturing |
| RoHS Compliant, Halogen-Free | | Environmentally Friendlier |
| MSL1, Industrial qualification | | Increased Reliability |

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| IRF7807VD1PbF-1 | SO-8 | Tube/Bulk | 95 | IRF7807VD1PbF-1 |
| | | Tape and Reel | 4000 | IRF7807VD1TRPbF-1 |

### Absolute Maximum Ratings

| Parameter | | Symbol | Max | Units |
|---|---|---|---|---|
| Drain-to-Source Voltage | | $V_{DS}$ | 30 | V |
| Gate-to-Source Voltage | | $V_{GS}$ | ±20 | |
| Continuous Output Current ($V_{GS}$ ≥ 4.5V) | 25°C | $I_D$ | 8.3 | A |
| | 70°C | | 6.6 | |
| Pulsed Drain Current ① | | $I_{DM}$ | 66 | |
| Power Dissipation ③ | 25°C | $P_D$ | 2.5 | W |
| | 70°C | | 1.6 | |
| Schottky and Body Diode Average Forward Current ④ | 25°C | $I_F$ (AV) | 3.5 | |
| | 70°C | | 2.2 | |
| Junction & Storage Temperature Range | | $T_J$ , $T_{STG}$ | -55 to 150 | °C |

### Thermal Resistance

| Parameter | Symbol | Typ | Max | Units |
|---|---|---|---|---|
| Maximum Junction-to-Ambient ③⑥ | $R_{\theta JA}$ | — | 50 | °C/W |
| Maximum Junction-to-Lead ⑥ | $R_{\theta JL}$ | — | 20 | |

## Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | 30 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 250µA |
| Static Drain-Source On-Resistance | $R_{DS(on)}$ | — | 17 | 25 | mΩ | $V_{GS}$ = 4.5V, $I_D$ = 7.0A ② |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1.0 | — | 3.0 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA |
| Drain-Source Leakage Current | $I_{DSS}$ | — | — | 100 | µA | $V_{DS}$ = 30V, $V_{GS}$ = 0V |
| | | — | — | 20 | µA | $V_{DS}$ = 24V, $V_{GS}$ = 0V |
| | | — | — | 2.0 | mA | $V_{DS}$ = 24V, $V_{GS}$ = 0V, $T_J$ = 100°C |
| Gate-Source Leakage Current | $I_{GSS}$ | — | — | ±100 | nA | $V_{GS}$ = ± 20V |
| Total Gate Charge* | $Q_G$ | — | 9.5 | 14 | nC | $V_{DS}$ = 4.5V<br>$I_D$ = 7.0A<br>$V_{DS}$ = 16V |
| Pre-Vth Gate-Source Charge | $Q_{GS1}$ | — | 2.3 | — | | |
| Post-Vth Gate-Source Charge | $Q_{GS2}$ | — | 1.0 | — | | |
| Gate-to-Drain Charge | $Q_{GD}$ | — | 2.4 | — | | |
| Switch Charge ($Q_{gs2}$ + $Q_{gd}$) | $Q_{SW}$ | — | 3.4 | 5.2 | | |
| Output Charge* | $Q_{OSS}$ | — | 12 | 16.8 | | $V_{DS}$ = 16V, $V_{GS}$ = 0 |
| Gate Resistance | $R_G$ | 0.9 | — | 2.8 | Ω | |
| Turn-On Delay Time | $t_{d(on)}$ | — | 6.3 | — | ns | $V_{DD}$ = 16V, $I_D$ = 7.0V<br>$V_{GS}$ = 5V, $R_G$ = 2Ω<br>Resistive Load |
| Rise Time | $t_r$ | — | 1.2 | — | | |
| Turn-Off Delay Time | $t_{d(off)}$ | — | 11 | — | | |
| Fall Time | $t_f$ | — | 2.2 | — | | |

## Diode Characteristics

| Parameter | Symbol | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| Diode Forward Voltage | $V_{SD}$ | — | — | 0.5 | V | $T_J$ = 25°C, $I_S$ = 1.0A ,$V_{GS}$ = 0V② |
| | | — | — | 0.39 | | T = 125°C, $I_S$ = 1.0A, $V_{GS}$ = OV② |
| Reverse Recovery Time ④ | $t_{rr}$ | — | 51 | — | ns | di/dt = 700A/µs<br>$V_{DD}$ = 16V, $V_{GS}$ = 0V, $I_D$ = 15A |
| Reverse Recovery Charge ④ | $Q_{rr}$ | — | 51 | — | nC | $T_J$ = 25°C, $I_S$ = 7.0A ,$V_{DS}$ = 16V<br>di/dt = 100A/µs |

**Notes:**

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 400 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board
④ 50% Duty Cycle, Rectangular
⑤ Typical values of $R_{DS}$(on) measured at $V_{GS}$ = 4.5V, $Q_G$, $Q_{SW}$ and $Q_{OSS}$ measured at $V_{GS}$ = 5.0V, $I_F$ = 7.0A.
⑥ $R_\theta$ is measured at $T_J$ approximately 90°C
* Device are 100% tested to these parameters.

## Power MOSFET Selection for DC/DC Converters

### Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms $Q_{gs2}$ and $Q_{oss}$ which are new to Power MOSFET data sheets.

$Q_{gs2}$ is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, $Q_{gs1}$ and $Q_{gs2}$, can be seen from Fig 1.

$Q_{gs2}$ indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached (t1) and the time the drain current rises to $I_{dmax}$ (t2) at which time the drain voltage begins to change. Minimizing $Q_{gs2}$ is a critical factor in reducing switching losses in Q1.

$Q_{oss}$ is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure 2 shows how $Q_{oss}$ is formed by the parallel combination of the voltage dependant (non-linear) capacitance's $C_{ds}$ and $C_{dg}$ when multiplied by the power supply input buss voltage.

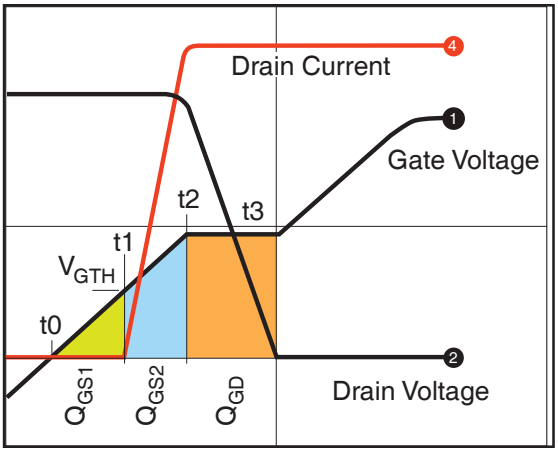



Figure 1: Typical MOSFET switching waveform

### Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge $Q_{oss}$ and reverse recovery charge $Q_{rr}$ both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and $V_{in}$. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of $Q_{gd}/Q_{gs1}$ must be minimized to reduce the potential for Cdv/dt turn on.

Spice model for IRF7807V can be downloaded in machine readable format at www.irf.com.

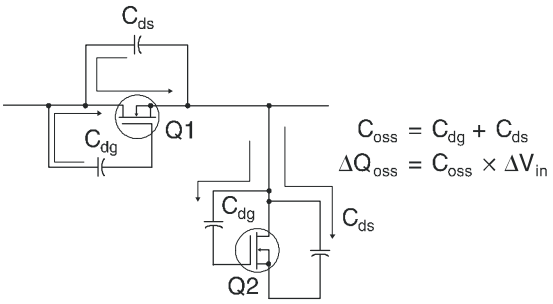



Figure 2: $Q_{oss}$ Characteristic

## Typical Mobile PC Application

The performance of these new devices has been tested in circuit and correlates well with performance predictions generated by the system models. An advantage of this new technology platform is that the MOSFETs it produces are suitable for both control FET and synchronous FET applications. This has been demonstrated with the 3.3V and 5V converters. (Fig 3 and Fig 4). In these applications the same MOSFET IRF7807V was used for both the control FET (Q1) and the synchronous FET (Q2). This provides a highly effective cost/performance solution.

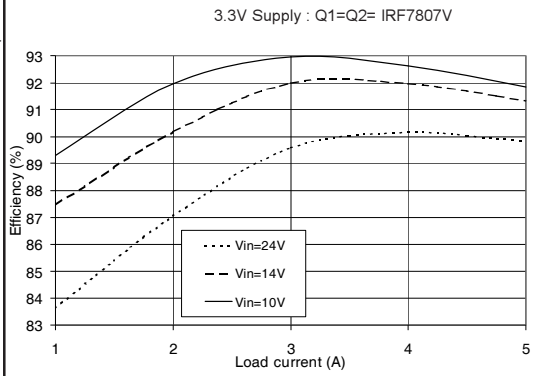



Figure 3

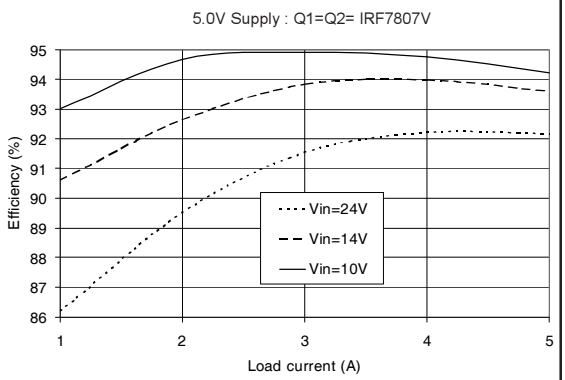



Figure 4

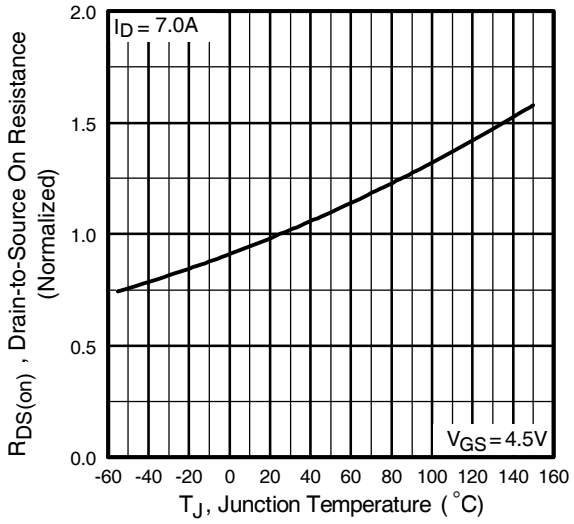



**Fig 5.** Normalized On-Resistance Vs. Temperature

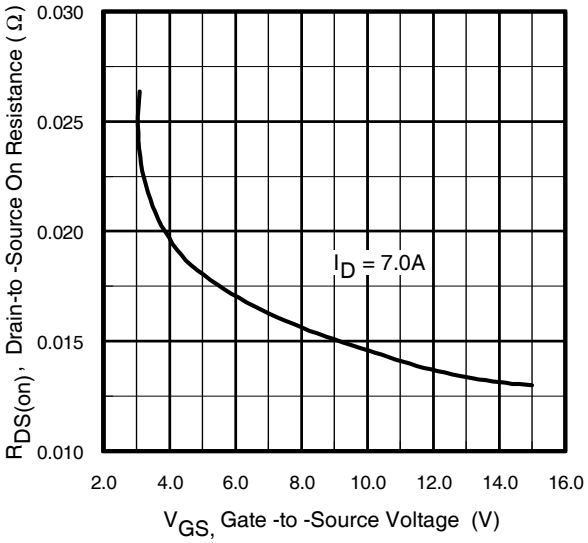



**Fig 7.** On-Resistance Vs. Gate Voltage

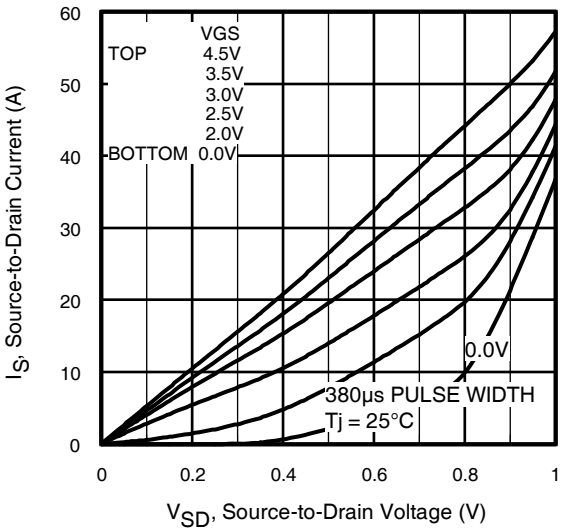



**Fig 7.** Typical Reverse Output Characteristics

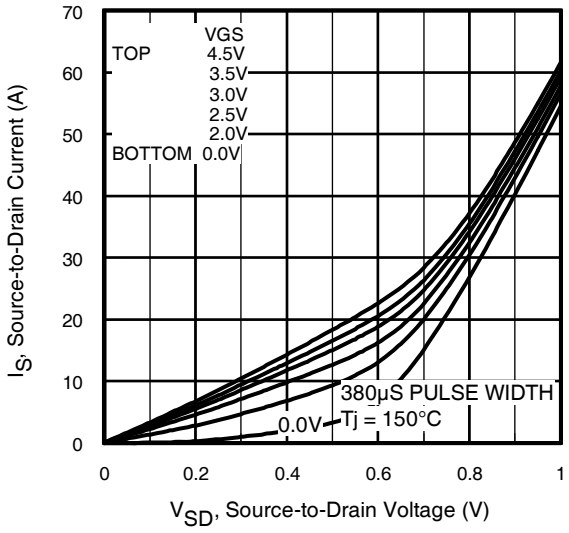



**Fig 8.** Typical Reverse Output Characteristics

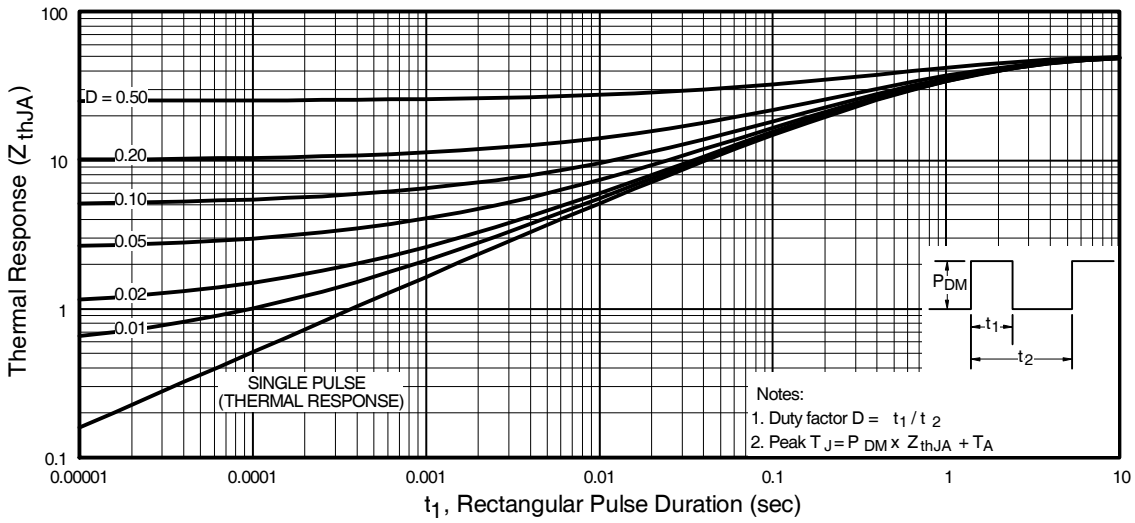



Figure 9. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

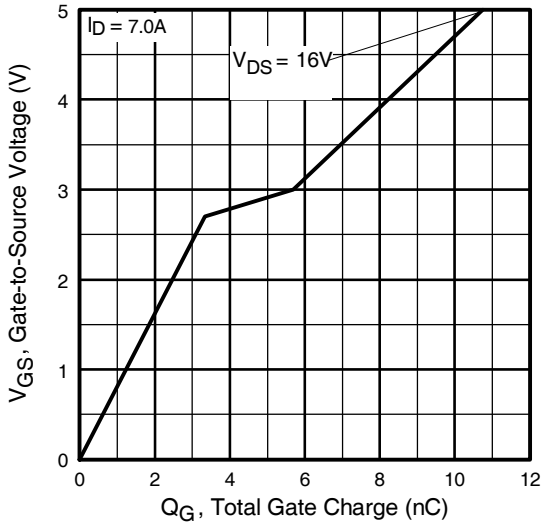



**Fig 10.** Typical Gate Charge Vs. Gate-to-Source Voltage

## MOSFET , Body Diode & Schottky Diode Characteristics

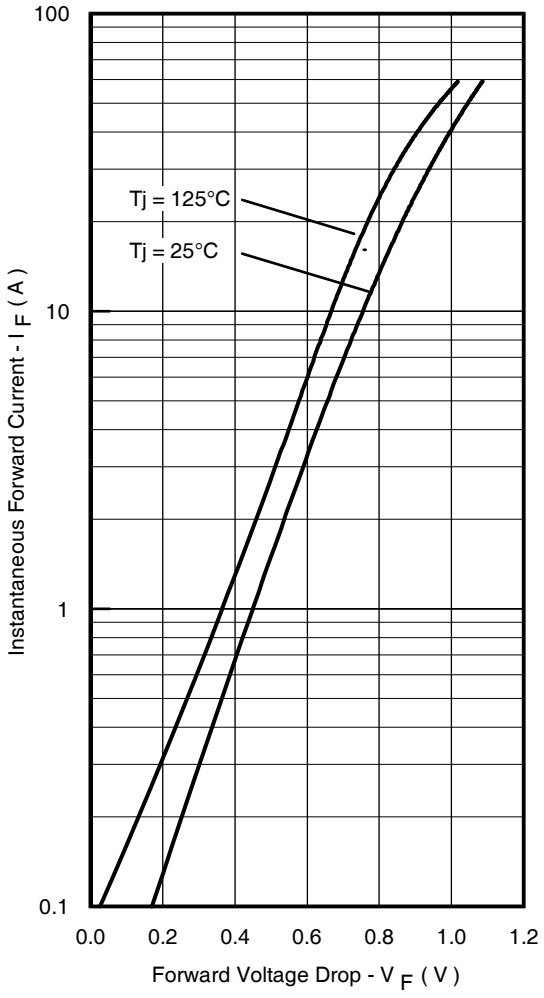



**Fig. 11** - Typical Forward Voltage Drop Characteristics

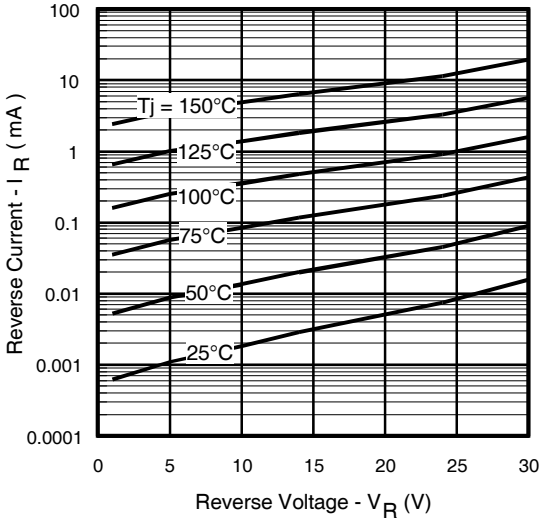
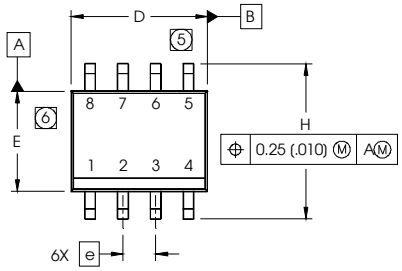


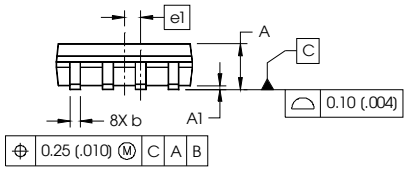

**Fig. 12** - Typical Values of Reverse Current Vs. Reverse Voltage

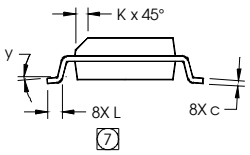
## SO-8 Package Outline(Mosfet & Fetky)

Dimensions are shown in milimeters (inches)

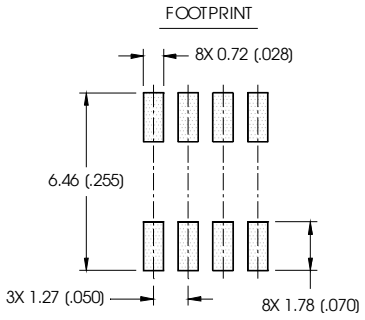



| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |



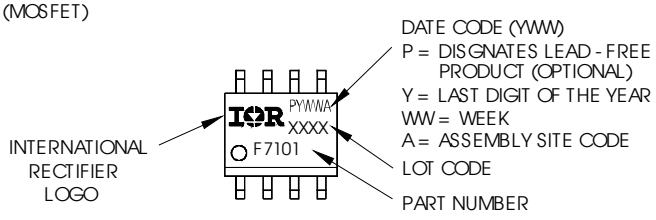




NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



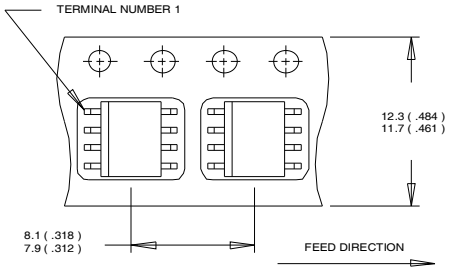

## SO-8 Part Marking Information (Lead - Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

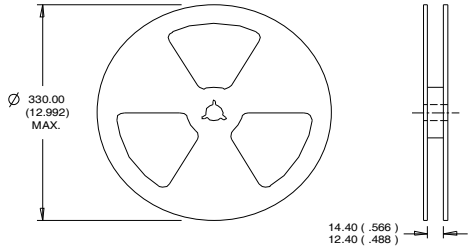



**Note: For the most current drawing please refer to IR website at http://www.irf.com/package/**

## SO-8 Tape and Reel (Dimensions are shown in milimeters (inches))




NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.




NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**Note: For the most current drawing please refer to IR website at http://www.irf.com/package/**

**Qualification information**†

| | | |
|---|---|---|
| Qualification level | Industrial (per JEDEC JESD47F†† guidelines) | |
| Moisture Sensitivity Level | SO-8 | MSL1 (per JEDEC J-STD-020D††) |
| RoHS compliant | Yes | |

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability
†† Applicable version of JEDEC standard at the time of product release

International
IOR Rectifier
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