

# 74ALVCH32973

## 16-bit bus transceiver and transparent D-type latch with 8 independent buffers

Rev. 3 — 17 January 2013

Product data sheet

### 1. General description

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The 74ALVCH32973 is a 16-bit bus transceiver and transparent D-type latch with 8 independent buffers with bus hold inputs and 3-state outputs. It features direction (1DIR, 2DIR), latch enable (1 $\overline{\text{LOE}}$ , 2 $\overline{\text{LOE}}$ ), transceiver output enable (1 $\overline{\text{TOE}}$ , 2 $\overline{\text{TOE}}$ ) and latch enable (1LE, 2LE) control inputs; four 8-bit transceiver ports (1An, 2An & 1Bn, 2Bn); two 8-bit D-type latch output ports (1Qn, 2Qn) and an 8-bit buffer with data inputs Dn and outputs Yn. The configuration of the control pins allows the device to be used as one 8-bit buffer, two 8-bit transceivers, and two 8-bit latches or one 8-bit buffer, one 16-bit transceiver and one 16-bit latch.

The 8-bit buffer functions independently of the control inputs. The direction of data transmission between A and B is controlled by nDIR and when n $\overline{\text{TOE}}$  is set HIGH the A and B ports will assume a HIGH-impedance OFF-state, they will be effectively isolated. When nLE is HIGH, data at the A inputs enter the latches. In this condition the latches are transparent, a Q output will change each time its corresponding A-input changes. When nLE is LOW the latches store the information that was present at the inputs a set-up time preceding the HIGH-to-LOW transition of nLE. A HIGH on n $\overline{\text{LOE}}$  causes the Q outputs to assume a high-impedance OFF-state. Operation of the n $\overline{\text{LOE}}$  input does not affect the state of the latches.

### 2. Features and benefits

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- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Current drive  $\pm 24$  mA at  $V_{\text{CC}} = 3.0$  V

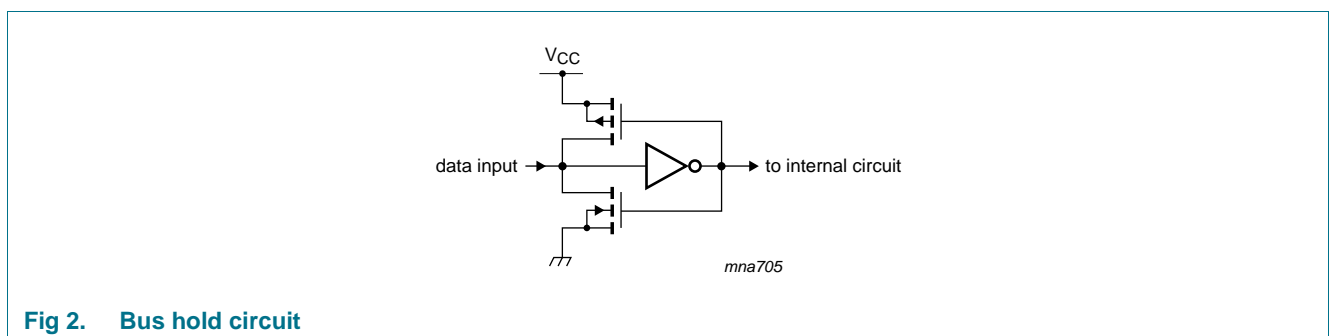
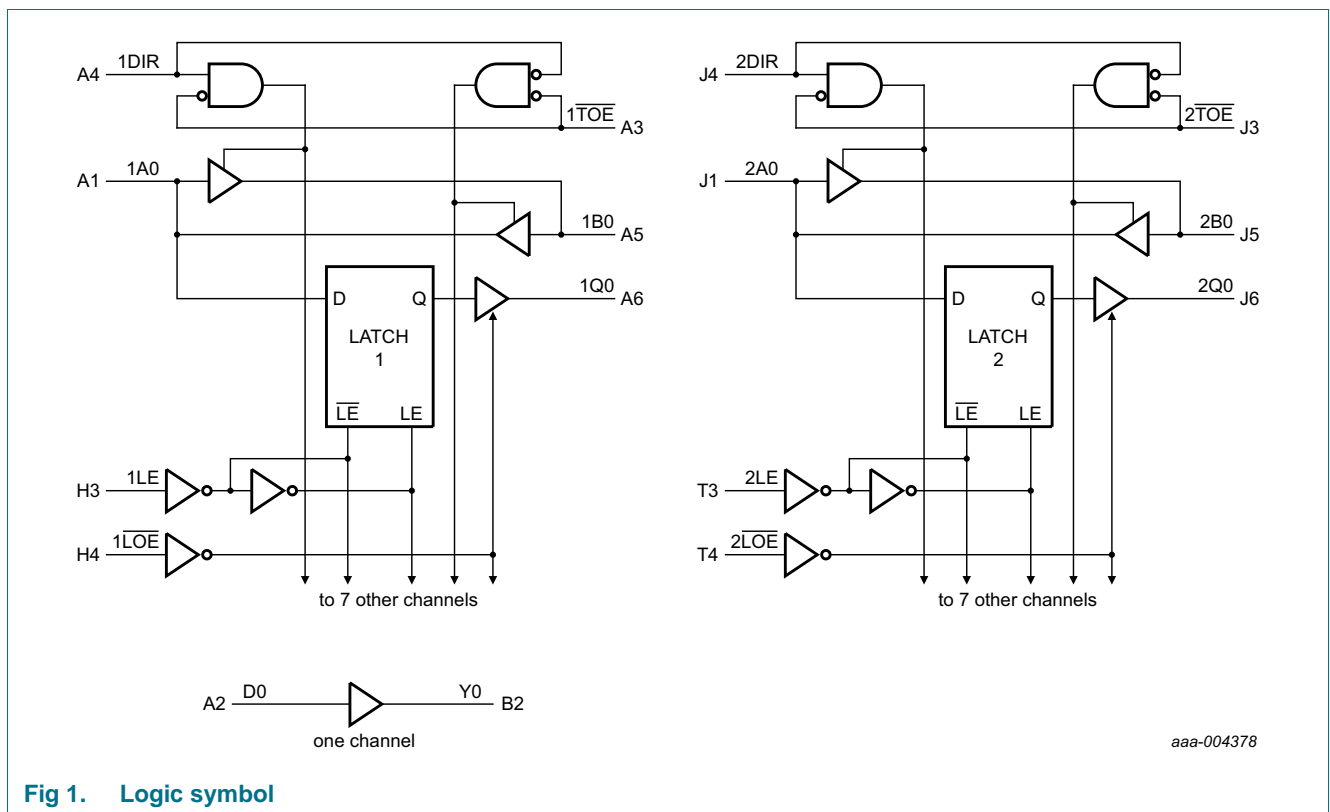


### 3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVCH32973EC	-40 °C to +85 °C	LFBGA96	plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 × 5.5 × 1.05 mm	SOT536-1

### 4. Functional diagram



## 5. Pinning information

### 5.1 Pinning

6	1Q0	1Q1	1Q2	1Q3	1Q4	1Q5	1Q6	1Q7	2Q0	2Q1	2Q2	2Q3	2Q4	2Q5	2Q6	2Q7
5	1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7	2B0	2B1	2B2	2B3	2B4	2B5	2B6	2B7
4	1DIR	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	1 $\overline{\text{LOE}}$	2DIR	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2 $\overline{\text{LOE}}$
3	1 $\overline{\text{TOE}}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	1LE	2 $\overline{\text{TOE}}$	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2LE
2	D0	Y0	D1	Y1	D2	Y2	D3	Y3	D4	Y4	D5	Y5	D6	Y6	D7	Y7
1	1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7	2A0	2A1	2A2	2A3	2A4	2A5	2A6	2A7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

aaa-004379

Fig 3. Pin configuration

### 5.2 Pin description

Table 2. Pin description

Symbol	Ball	Description
n $\overline{\text{TOE}}$ (n = 1 to 2)	A3, J3	transceiver output enable input (active LOW)
nDIR (n = 1 to 2)	A4, J4	direction control input (active HIGH)
nLE (n = 1 to 2)	H3, T3	latch enable input (active HIGH)
n $\overline{\text{LOE}}$ (n = 1 to 2)	H4, T4	latch output enable input (active LOW)
1A[0:7]	A1, B1, C1, D1, E1, F1, G1, H1	data input/output
D[0:7]	A2, C2, E2, G2, J2, L2, N2, R2	data input
1B[0:7]	A5, B5, C5, D5, E5, F5, G5, H5	data input/output
2B[0:7]	J5, K5, L5, M5, N5, P5, R5, T5	data input/output
Y[0:7]	B2, D2, F2, H2, K2, M2, P2, T2	data output
1Q[0:7]	A6, B6, C6, D6, E6, F6, G6, H6	data output
2A[0:7]	J1, K1, L1, M1, N1, P1, R1, T1	data input/output
2Q[0:7]	J6, K6, L6, M6, N6, P6, R6, T6	data output
GND	B3, B4, D3, D4, E3, E4, G3, G4, K3, K4, M3, M4, N3, N4, R3, R4	ground (0 V)
V <sub>CC</sub>	C3, C4, F3, F4, L3, L4, P3, P4	supply voltage

## 6. Functional description

### 6.1 Function table

Table 3. Function table<sup>[1]</sup>

Inputs			Internal latches	Outputs nQn	Operating mode
nLOE	nLE	nAn			
L	H	L	L	L	enable and read register (transparent mode)
L	H	H	H	H	
L	↓	l	L	L	latch and read register
L	↓	h	H	H	
L	L	X	no change	no change	hold mode
H	↓	l	L	Z	latch register and disable outputs
H	↓	h	H	Z	
H	H	L	L	Z	enable register and disable outputs
H	H	H	H	Z	
H	L	X	no change	Z	hold mode and disable outputs

- [1] H = HIGH voltage level;  
 L = LOW voltage level;  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;  
 ↓ = negative-going transition;  
 Z = high-impedance OFF-state;  
 X = don't care.

Table 4. Function table<sup>[1]</sup>

Inputs		Outputs		
nTOE	nDIR	nAn	nBn	
L	L	nAn = nBn	input	
L	H	input	nBn = nAn	
H	X	Z	Z	

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Table 5. Function table<sup>[1]</sup>

Input	Output
Dn	Yn
L	L
H	H

- [1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage	control inputs	[1] -0.5	+4.6	V
		data inputs	[1] -0.5	$V_{CC} + 0.5$	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage		[1] -0.5	$V_{CC} + 0.5$	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +85 °C	[2] -	1000	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 70 °C the value of  $P_{tot}$  derates linearly with 1.8 mW/K.

## 8. Recommended operating conditions

**Table 7. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage	maximum speed performance				
		$C_L = 30$ pF	2.3	-	2.7	V
		$C_L = 50$ pF	3.0	-	3.6	V
		low voltage applications	1.2	-	3.6	V
$V_I$	input voltage		0	-	$V_{CC}$	V
$V_O$	output voltage		0	-	$V_{CC}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.0 V	0	-	20	ns/V
		$V_{CC} = 3.0$ V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 8. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 1.8 V	0.7V <sub>CC</sub>	0.9	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	0	V
		V <sub>CC</sub> = 1.8 V	-	0.9	0.2V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.8 V to 3.6 V	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> - 0.4	V <sub>CC</sub> - 0.1	-	V
		I <sub>O</sub> = -6 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.17	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 2.7 V	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	-	V
		I <sub>O</sub> = -18 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	-	V
		I <sub>O</sub> = -24 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.8 V to 3.6 V	-	0	0.20	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 1.8 V	-	0.09	0.30	V
		I <sub>O</sub> = 6 mA; V <sub>CC</sub> = 2.3 V	-	0.07	0.20	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.3 V	-	0.15	0.40	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 2.7 V	-	0.14	0.40	V
		I <sub>O</sub> = 18 mA; V <sub>CC</sub> = 2.3 V	-	0.23	0.60	V
		I <sub>O</sub> = 24 mA; V <sub>CC</sub> = 3.0 V	-	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>CC</sub> = 1.8 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	5	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND				
		V <sub>CC</sub> = 1.8 V to 2.7 V	-	0.1	5	μA
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	0.1	10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A;				
		V <sub>CC</sub> = 1.8 V to 2.7 V	-	0.4	80	μA
		V <sub>CC</sub> = 2.7 V to 3.6 V	-	0.4	80	μA
ΔI <sub>CC</sub>	additional supply current	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A;				
		V <sub>CC</sub> = 2.7 V to 3.6 V				
		per control input	-	5	500	μA
	per data I/O input	-	150	750	μA	
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 0.7 V	45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 0.8 V	75	150	-	μA

**Table 8. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 2.3 V; V <sub>I</sub> = 1.7 V	-45	-	-	μA
		V <sub>CC</sub> = 3.0 V; V <sub>I</sub> = 2.0 V	-75	-175	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 3.6 V	500	-	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 3.6 V	-500	-	-	μA
C <sub>I</sub>	input capacitance		-	5.0	-	pF
C <sub>I/O</sub>	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

## 10. Dynamic characteristics

**Table 9. Dynamic characteristics**At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
t <sub>pd</sub>	propagation delay	nAn to nQn; see <a href="#">Figure 4</a>		<a href="#">[2]</a>			
		V <sub>CC</sub> = 1.2 V	-	7.0	-	ns	
		V <sub>CC</sub> = 1.8 V	1.1	3.4	5.7	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	1.0	2.2	3.9	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	3.8	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	<a href="#">[4]</a>	1.0	2.5	3.6	ns
		nLE to nQn; see <a href="#">Figure 5</a>		<a href="#">[2]</a>			
		V <sub>CC</sub> = 1.2 V	-	8.2	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	3.7	5.9	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	1.0	2.4	3.8	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.7	4.3	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	<a href="#">[4]</a>	0.8	2.6	4.1	ns
		nAn to nBn or nBn to nAn; see <a href="#">Figure 6</a>		<a href="#">[2]</a>			
		V <sub>CC</sub> = 1.2 V	-	5.9	-	ns	
		V <sub>CC</sub> = 1.8 V	1.4	3.0	4.3	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	1.0	2.0	3.8	ns
		V <sub>CC</sub> = 2.7 V	1.0	2.3	3.7	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	<a href="#">[4]</a>	1.0	2.2	3.4	ns
Dn to Yn; see <a href="#">Figure 7</a>		<a href="#">[2]</a>					
V <sub>CC</sub> = 1.2 V	-	4.6	-	ns			
V <sub>CC</sub> = 1.8 V	1.1	2.4	5.1	ns			
V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	0.7	1.7	3.7	ns		
V <sub>CC</sub> = 2.7 V	1.0	2.1	3.6	ns			
V <sub>CC</sub> = 3.0 V to 3.6 V	<a href="#">[4]</a>	0.9	1.8	3.1	ns		

**Table 9. Dynamic characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
t <sub>en</sub>	enable time	n $\overline{\text{LOE}}$ to nQn; see <a href="#">Figure 8</a>					
			[2]				
		V <sub>CC</sub> = 1.2 V	-	9.5	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	4.6	7.3	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	3.0	5.2	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.3	4.9	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	2.7	4.3	ns
		n $\overline{\text{TOE}}$ to nAn or nBn; see <a href="#">Figure 8</a>					
			[2]				
		V <sub>CC</sub> = 1.2 V	-	10.0	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	4.7	7.6	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	3.2	5.7	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.3	5.4	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	2.7	4.4	ns
		nDIR to nAn or nBn; see <a href="#">Figure 8</a>					
			[2]				
		V <sub>CC</sub> = 1.2 V	-	7.0	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	3.5	7.6	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	2.7	5.2	ns
		V <sub>CC</sub> = 2.7 V	1.0	4.2	6.0	ns	
V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	3.4	5.0	ns		
t <sub>dis</sub>	disable time	n $\overline{\text{LOE}}$ to nQn; see <a href="#">Figure 8</a>					
			[2]				
		V <sub>CC</sub> = 1.2 V	-	6.7	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	3.5	5.6	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	2.2	4.1	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.4	4.7	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	3.1	4.2	ns
		n $\overline{\text{TOE}}$ to nAn or nBn; see <a href="#">Figure 8</a>					
			[2]				
		V <sub>CC</sub> = 1.2 V	-	7.0	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	3.6	7.6	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	2.6	5.2	ns
		V <sub>CC</sub> = 2.7 V	1.0	3.5	4.6	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	3.2	4.3	ns
		nDIR to nAn or nBn; see <a href="#">Figure 8</a>					
			[2]				
		V <sub>CC</sub> = 1.2 V	-	7.2	-	ns	
		V <sub>CC</sub> = 1.8 V	1.5	3.7	7.6	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	[3]	1.0	2.7	5.2	ns
		V <sub>CC</sub> = 2.7 V	1.0	4.0	6.0	ns	
V <sub>CC</sub> = 3.0 V to 3.6 V	[4]	1.0	3.2	5.0	ns		



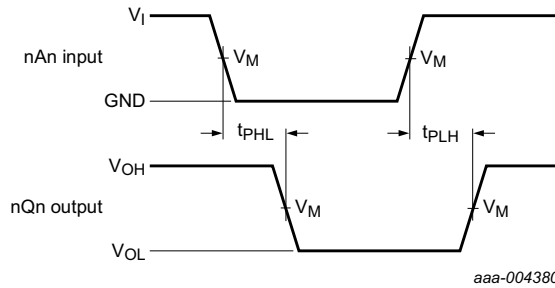
**Table 9. Dynamic characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit [Figure 10](#).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit	
t <sub>w</sub>	pulse width	nLE HIGH; see <a href="#">Figure 5</a>					
		V <sub>CC</sub> = 1.8 V	3.5	1.0	-	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	3.0	1.0	-	ns
		V <sub>CC</sub> = 2.7 V		3.0	1.0	-	ns
t <sub>su</sub>	set-up time	nAn to nLE; see <a href="#">Figure 9</a>					
		V <sub>CC</sub> = 1.8 V	1.1	-0.1	-	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	1.1	-0.1	-	ns
		V <sub>CC</sub> = 2.7 V		1.1	-0.1	-	ns
t <sub>h</sub>	hold time	nAn to nLE; see <a href="#">Figure 9</a>					
		V <sub>CC</sub> = 1.8 V	1.3	0.1	-	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	<a href="#">[3]</a>	1.6	0.2	-	ns
		V <sub>CC</sub> = 2.7 V		1.6	0.4	-	ns
C <sub>PD</sub>	power dissipation capacitance	per latch or buffer; V <sub>I</sub> = GND to V <sub>CC</sub> ; V <sub>CC</sub> = 1.2 V to 3.6 V	<a href="#">[5]</a>				
		Q outputs enabled; A and B ports isolated; f <sub>i(nAn)</sub> = 10 MHz; f <sub>i(nLE)</sub> = 20 MHz; f <sub>i(nQn)</sub> = 10 MHz		-	26	-	pF
		A outputs enabled; Q output disabled; f <sub>i(nAn)</sub> = 10 MHz; f <sub>i(nBn)</sub> = 10 MHz		-	16	-	pF
		B outputs enabled; Q output disabled; f <sub>i(nAn)</sub> = 10 MHz; f <sub>i(nBn)</sub> = 10 MHz		-	16	-	pF
		Y outputs enabled; A and B parts isolated; Q output disabled; f <sub>i(Dn)</sub> = 10 MHz; f <sub>i(Yn)</sub> = 10 MHz		-	12	-	pF
		all outputs disabled; one nLE input and one nAn input switching; f <sub>i(nAn)</sub> = 10 MHz; f <sub>i(nLE)</sub> = 20 MHz; f <sub>i(nQn)</sub> = 0 MHz		-	18	-	pF
		Q outputs disabled; A and B ports isolated; one nLE input switching; f <sub>i(nAn)</sub> = 0 MHz; f <sub>i(nLE)</sub> = 20 MHz; f <sub>i(nQn)</sub> = 0 MHz		-	6	-	pF

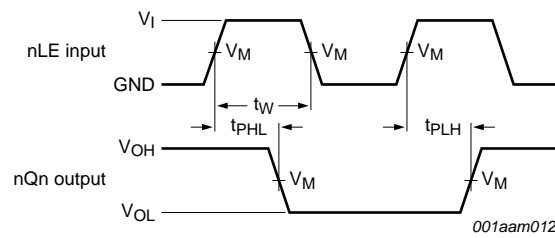
- [1] All typical values are measured at T<sub>amb</sub> = 25 °C.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
t<sub>en</sub> is the same as t<sub>pZL</sub> and t<sub>pZH</sub>.  
t<sub>dis</sub> is the same as t<sub>pLZ</sub> and t<sub>pHZ</sub>.
- [3] Typical values are measured at V<sub>CC</sub> = 2.5 V.
- [4] Typical values are measured at V<sub>CC</sub> = 3.3 V.
- [5] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> × N + Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz;  
C<sub>L</sub> = output load capacitance in pF;  
V<sub>CC</sub> = supply voltage in Volts;  
N = number of inputs switching;  
Σ(C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

11. Waveforms



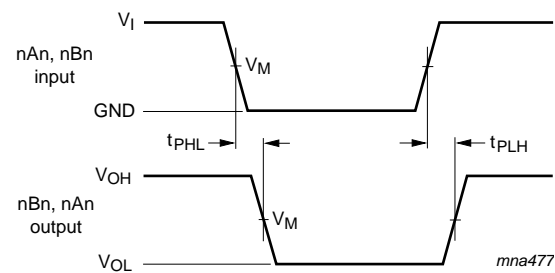
Measurement points are given in [Table 10](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig 4. Propagation delay, input (nAn) to data output (nQn)**



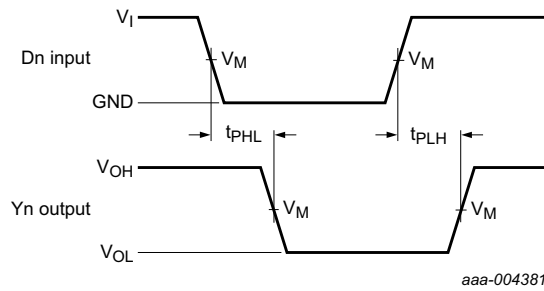
Measurement points are given in [Table 10](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig 5. Propagation delay, latch enable input (nLE) to data output (nQn), and pulse width**



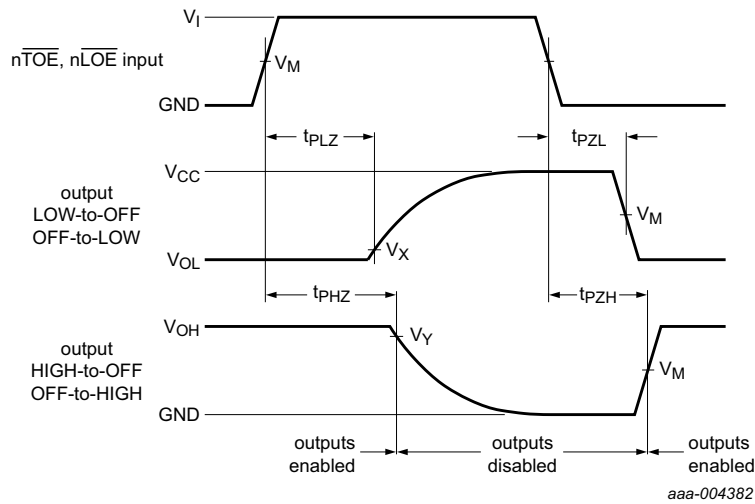
Measurement points are given in [Table 10](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig 6. Propagation delay, input (nAn, nBn) to data output (nBn, nAn)**



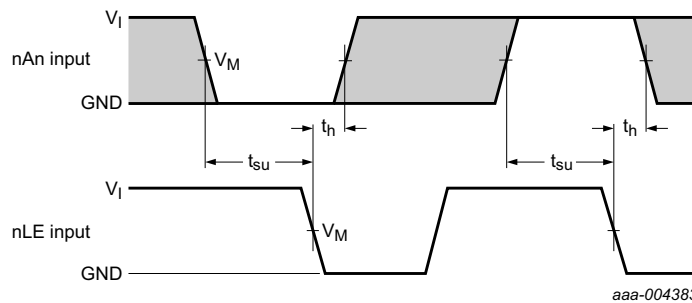
Measurement points are given in [Table 10](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig 7. Propagation delay, input (Dn) to data output (Yn)**



Measurement points are given in [Table 10](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output levels that occur with the output load.

**Fig 8. 3-state enable and disable times**



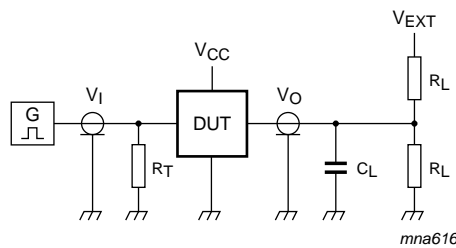
Measurement points are given in [Table 10](#).  
 The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 9. Data setup and hold times for input (nAn) to input (nLE)**

Table 10. Measurement points

Supply voltage	Input		Output		
V <sub>CC</sub>	V <sub>I</sub>	V <sub>M</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>
2.3 V to 2.7 V and < 2.3 V	V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 0.15 V	V <sub>OH</sub> - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V <sub>OL</sub> + 0.3 V	V <sub>OH</sub> - 0.3 V

## 12. Test information



Test data is given in [Table 11](#).

Definitions for test circuit:

R<sub>L</sub> = Load resistance.

C<sub>L</sub> = Load capacitance including jig and probe capacitance.

R<sub>T</sub> = Termination resistance should be equal to output impedance Z<sub>o</sub> of the pulse generator.

V<sub>EXT</sub> = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 11. Test data

Supply voltage	Input		Load		V <sub>EXT</sub>		
V <sub>CC</sub>	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	R <sub>L</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	t <sub>PLZ</sub> , t <sub>PZL</sub>	t <sub>PHZ</sub> , t <sub>PZH</sub>
2.3 V to 2.7 V and < 2.3 V	V <sub>CC</sub>	≤ 2.0 ns	30 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V <sub>CC</sub>	GND

13. Package outline

LFBGA96: plastic low profile fine-pitch ball grid array package; 96 balls; body 13.5 x 5.5 x 1.05 mm SOT536-1

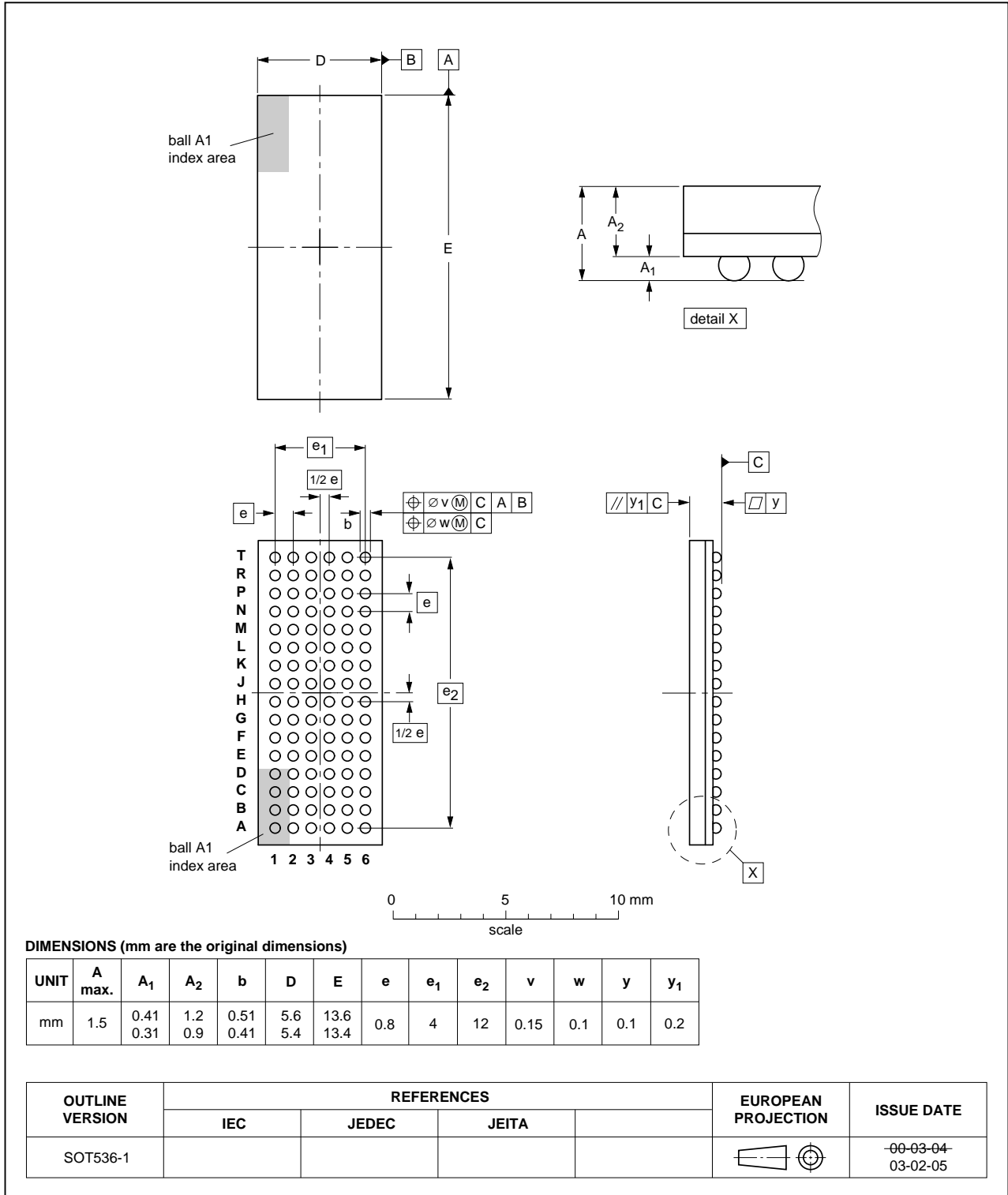


Fig 11. Package outline SOT536-1 (LFBGA96)

## 14. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH32973 v.3	20130117	Product data sheet	-	74ALVCH32973 v.2
Modifications:	• Table note of function table updated (LOW-to-HIGH changed into HIGH-to-LOW).			
74ALVCH32973 v.2	20121108	Product data sheet	-	74ALVCH32973 v.1
Modifications:	• Function table updated.			
74ALVCH32973 v.1	20120822	Product data sheet	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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